Table 11: AC Parameters (Die)

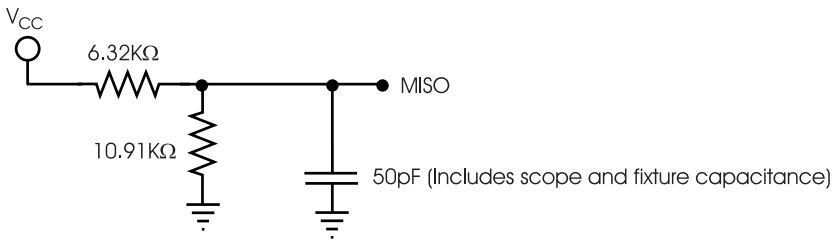
Symbol	Characteristic	Min(2)	Typ(1)	Max(2)	Units	Conditions
THD	Total Harmonic Distortion		1	2	%	@ 1 KHz
V_{IN}	ANA IN Input Voltage			32	mV	Peak-to-Peak(4) (7) (8)

1. *Typical values: T_A = 25°C and 3.0 V.*
2. *All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cut off depends upon the value of external capacitors (see Pin Descriptions).*
4. *Single-ended input mode. In the differential input mode, V_{IN} maximum for ANA IN+ and ANA IN– is 16 mV peak-to-peak.*
5. *For greater stability, an external clock can be utilized (see Pin Descriptions).*
6. *Filter specification applies to the antialiasing filter and to the smoothing filter.*
7. *The typical output voltage will be approximately 570 mV peak-to-peak with V_{IN} at 32 mV peak-to-peak.*
8. *For optimal signal quality, this maximum limit is recommended.*
9. *When a record command is sent, T_{RAC} = T_{RAC} + T_{RACLO} on the first row addressed.*

Table 12: SPI AC Parameters[1]

Symbol	Characteristics	Min	Max	Units	Conditions
T_{SSS}	$\overline{SS}$ Setup Time	500		nsec	
T_{SSH}	$\overline{SS}$ Hold Time	500		nsec	
T_{DIS}	Data in Setup Time	200		nsec	
T_{DIH}	Data in Hold Time	200		nsec	
T_{PD}	Output Delay		500	nsec	
T_{DF}(2)	Output Delay to hiZ		500	nsec	
T_{SSmin}	$\overline{SS}$ HIGH	1		µsec	
T_{SCKhi}	SCLK High Time	400		nsec	
T_{SCKlow}	SCLK Low Time	400		nsec	
F_0	CLK Frequency		1,000	KHz	

1. *Typical values: T_A= 25°C and 3.0 V. Timing measured at 50 percent of the V_{CC} level.*
2. *Tristate test condition.*



TIMING DIAGRAMS

Figure 5: Timing Diagram

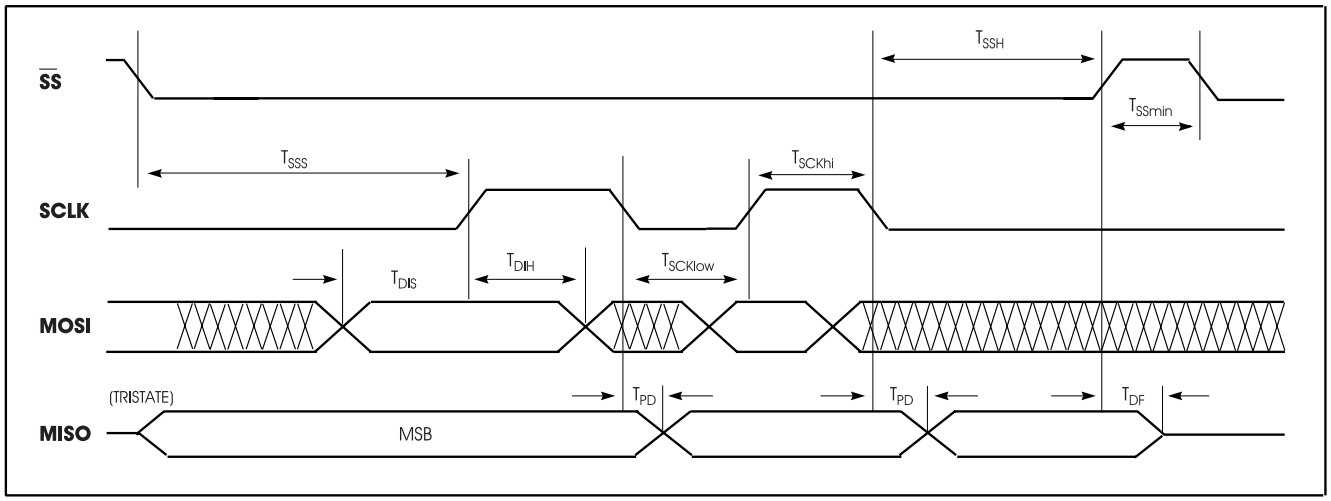


Figure 6: 8-Bit Command Format

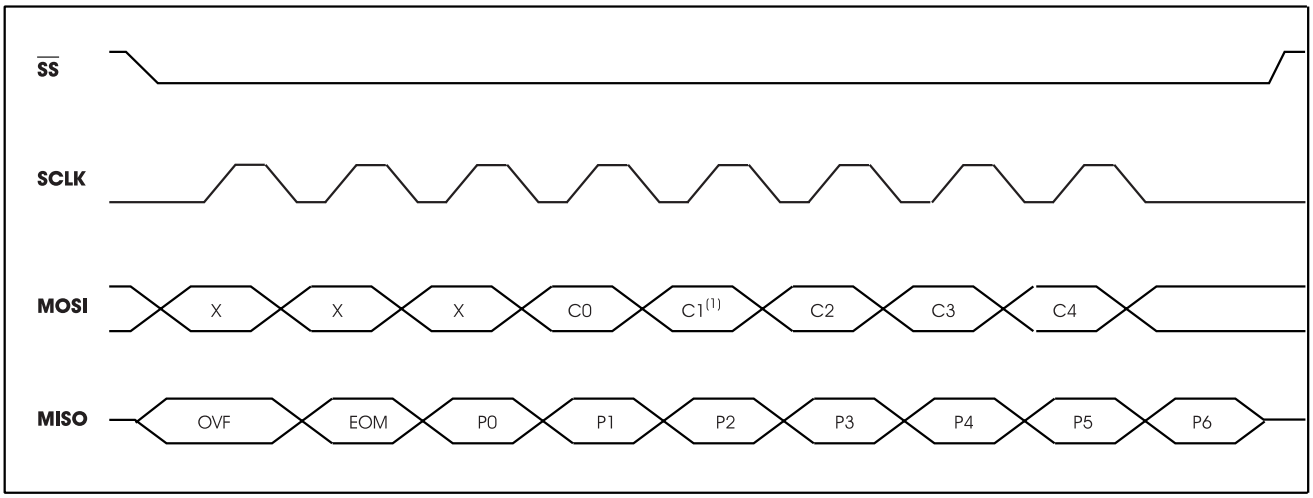


Figure 7: 24-Bit Command Format

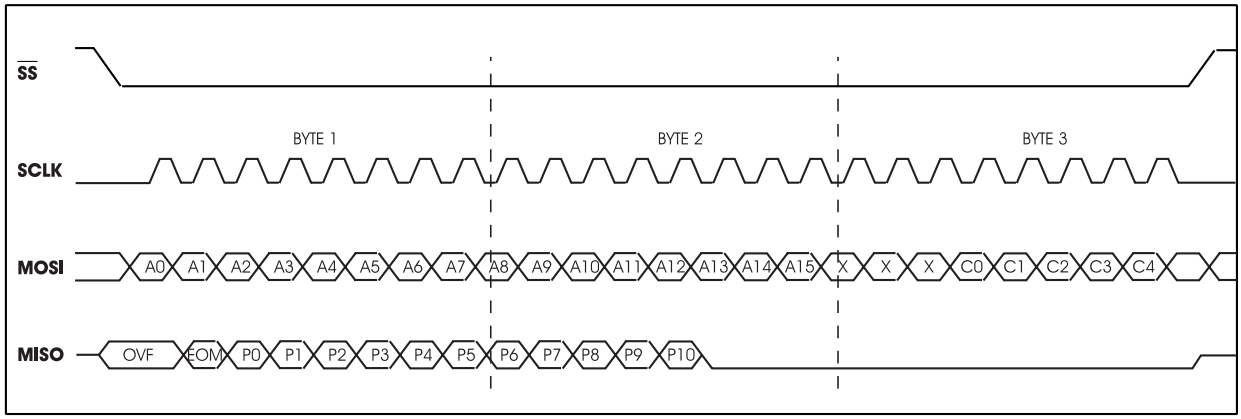


Figure 8: Playback/Record and Stop Cycle

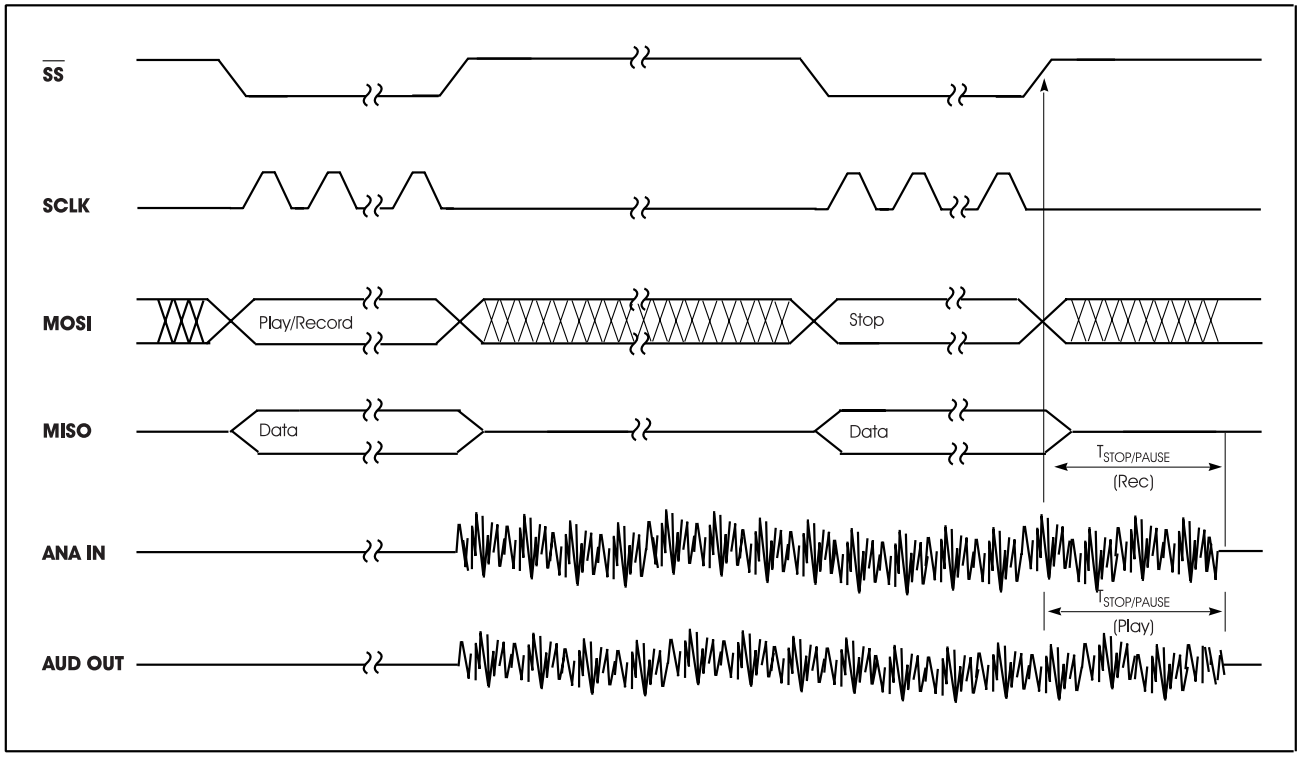
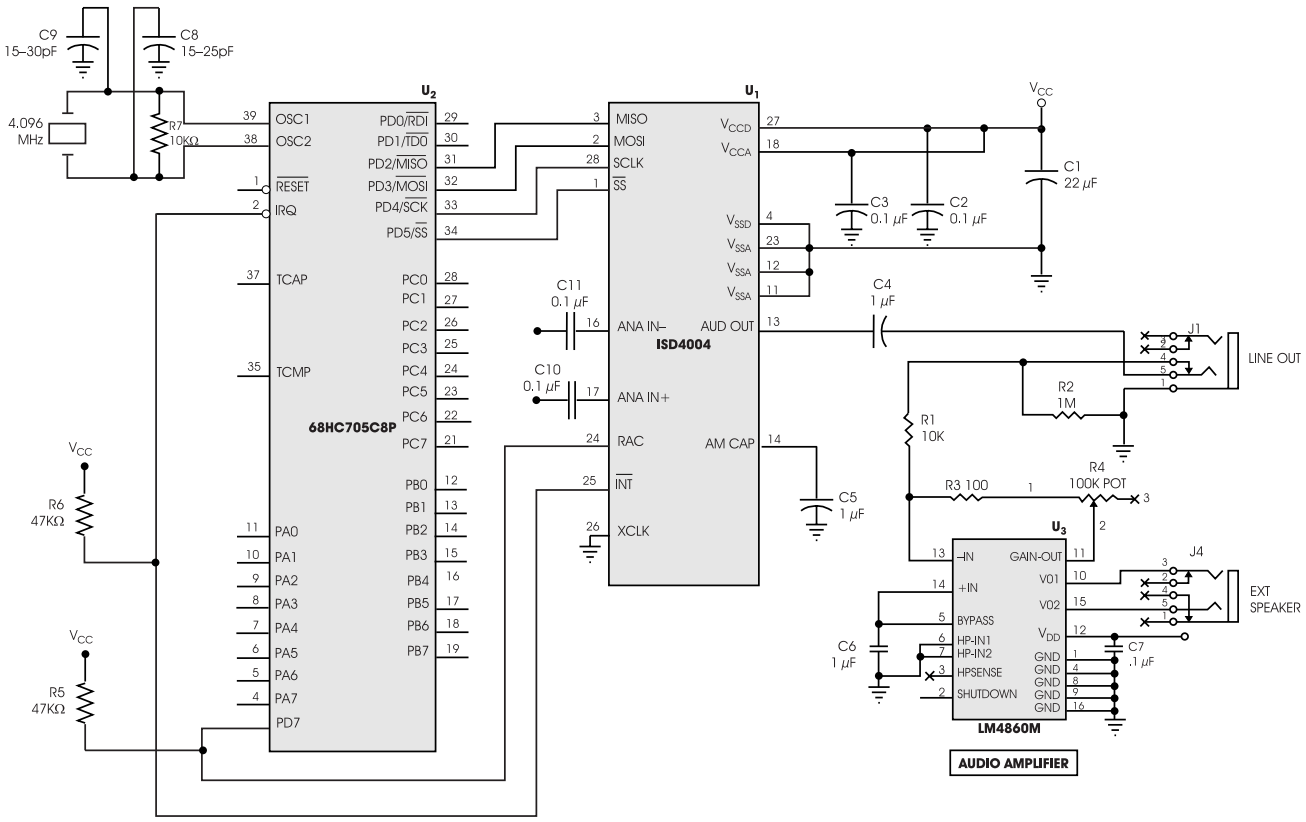
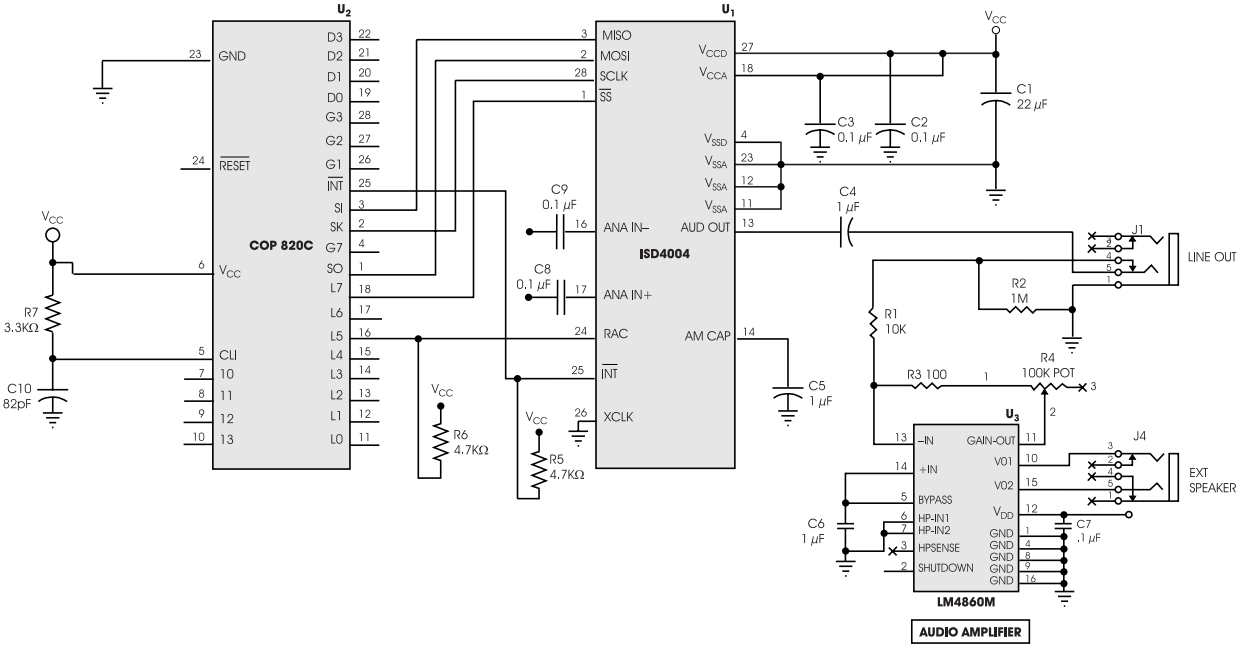


Figure 9: Application Example Using SPI(1)



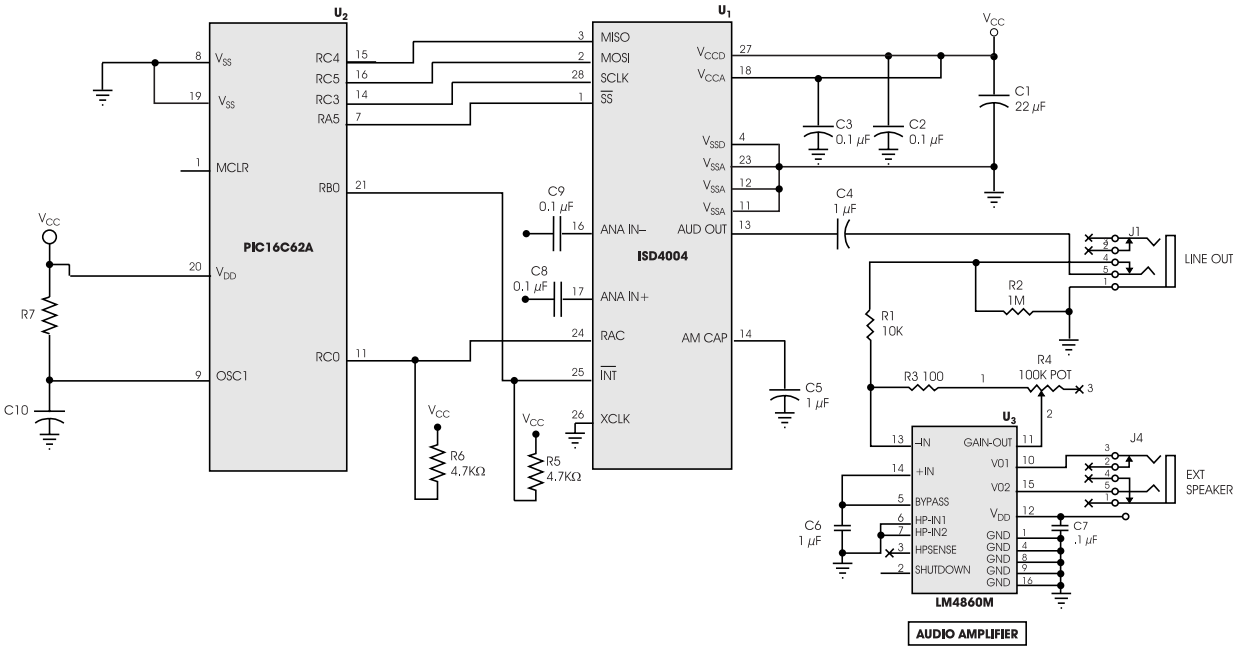
1. *This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.*
2. *Please make sure the bypass capacitor, C2 is as close as possible to the package.*

Figure 10: Application Example Using Microwire(1)



1. *This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.*
2. *Please make sure the bypass capacitor, C2 is as close as possible to the package.*

Figure 11: Application Example Using SPI Port on Microcontroller(1)



1. *This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.*
2. *Please make sure the bypass capacitor, C2 is as close as possible to the package.*

DEVICE PHYSICAL DIMENSIONS

Figure 12: 28-Lead 8x13.4 mm Plastic Thin Small Outline Package (TSOP) Type I (E)

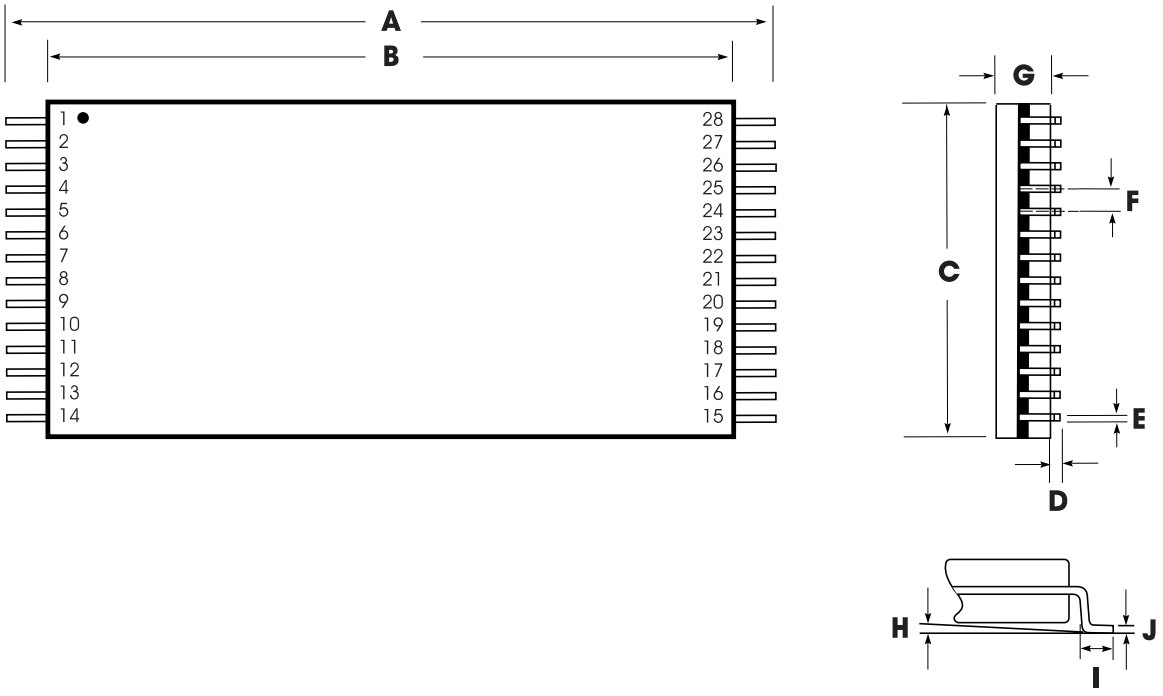


Table 13: Plastic Thin Small Outline Package (TSOP) Type I (E) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.520	0.528	0.535	13.20	13.40	13.60
B	0.461	0.465	0.469	11.70	11.80	11.90
C	0.311	0.315	0.319	7.90	8.00	8.10
D	0.002		0.006	0.05		0.15
E	0.007	0.009	0.011	0.17	0.22	0.27
F		0.0217			0.55	
G	0.037	0.039	0.041	0.95	1.00	1.05
H	0°	3°	6°	0°	3°	6°
I	0.020	0.022	0.028	0.50	0.55	0.70
J	0.004		0.008	0.10		0.21

NOTE: *Lead coplanarity to be within 0.004 inches.*

Figure 13: 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP) (P)

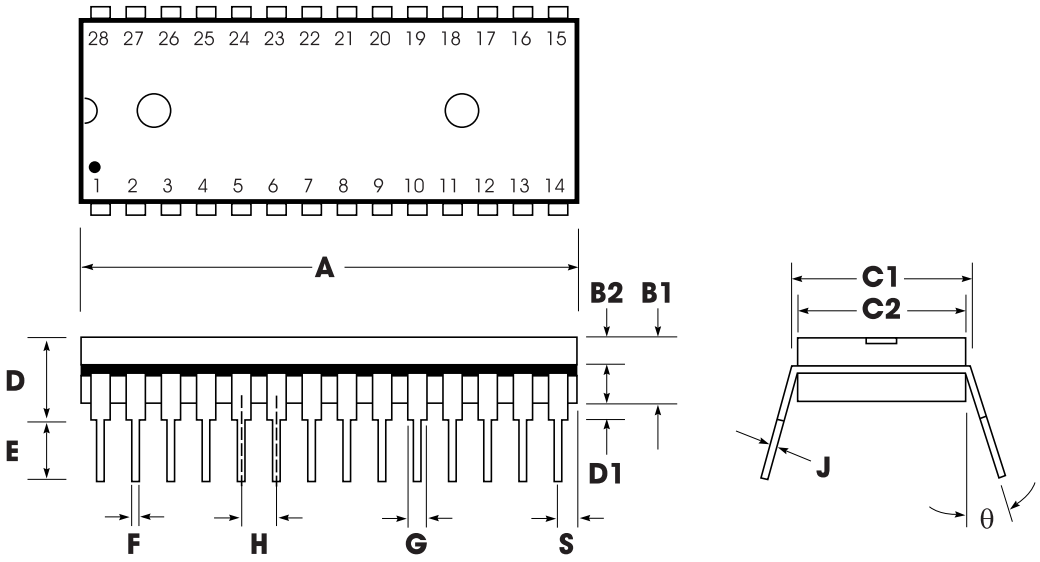


Table 14: Plastic Dual Inline Package (PDIP) (P) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.65
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
q	0°		15°	0°		15°

Figure 14: 28-Lead 0.300-Inch Plastic Small Outline Integrated Circuit (SOIC) (S)

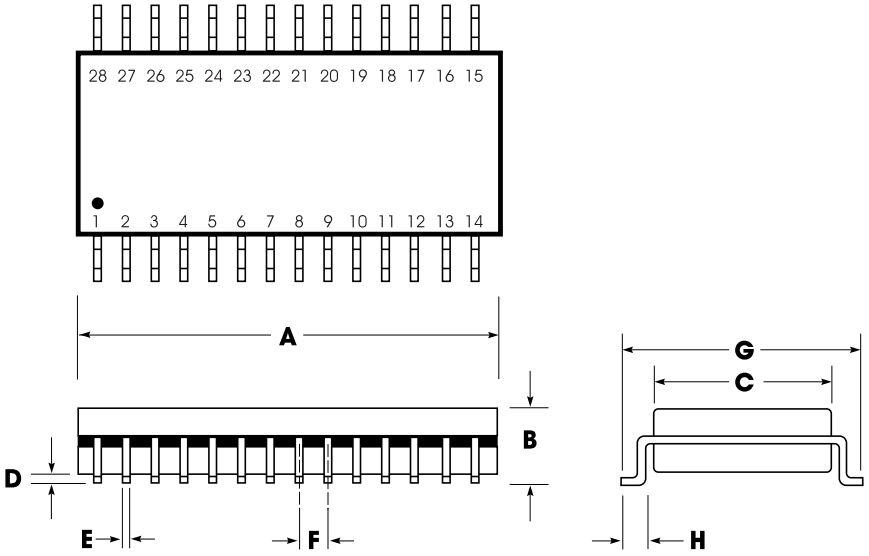


Table 15: Plastic Small Outline Integrated Circuit (SOIC) (S) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.701	0.706	0.711	17.81	17.93	18.06
B	0.097	0.101	0.104	2.46	2.56	2.64
C	0.292	0.296	0.299	7.42	7.52	7.59
D	0.005	0.009	0.0115	0.127	0.22	0.29
E	0.014	0.016	0.019	0.35	0.41	0.48
F		0.050			1.27	
G	0.400	0.406	0.410	10.16	10.31	10.41
H	0.024	0.032	0.040	0.61	0.81	1.02

NOTE: *Lead coplanarity to be within 0.004 inches.*

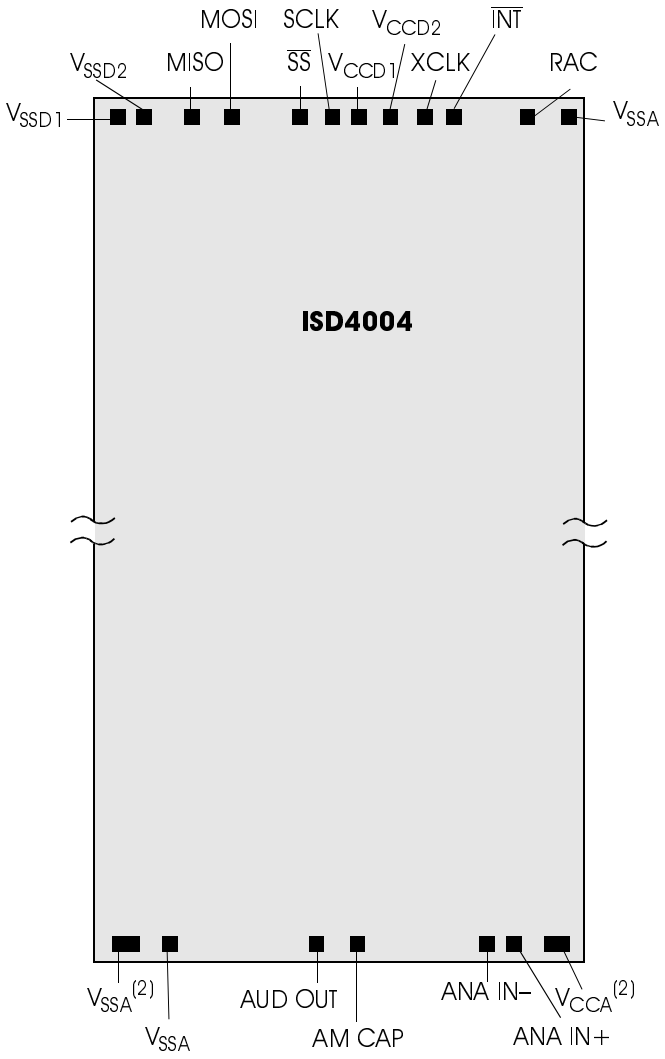
Figure 15: ISD4004 Series Bonding Physical Layout[1] (Unpackaged Die)

ISD4004 Series

I. Die Dimensions
X: 4230 microns
Y: 9780 microns

II. Die Thickness[3]
11.5 ±0.5 mils

III. Pad Opening (min)
90 x 90 microns
3.5 x 3.5 mils



1. *The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.*
2. *Double bond recommended.*
3. *This figure reflects the current die thickness. Please contact ISD as this thickness may change in the future.*

Table 16: ISD4004 Series Device Pin/Pad Designations, with Respect to Die Center (µm)

Pin	Pin Name	X Axis	Y Axis
V_{SSA}	V_{SS} Analog Power Supply	–1898.1	–4622.4
V_{SSA}	V_{SS} Analog Power Supply	–1599.9	–4622.4
AUD OUT	Audio Output	281.9	–4622.4
AM CAP	AutoMute	577.3	–4622.4
ANA IN –	Inverting Analog Input	1449.4	–4622.4
ANA IN +	Noninverting Analog Input	1603.5	–4622.4
V_{CCA}[1]	V_{CC} Analog Power Supply	1898.7	–4622.4
V_{SSA}	V_{SS} Analog Power Supply	1885.2	–4622.4
RAC	Row Address Clock	1483.8	4623.7
INT	Interrupt	794.8	4623.7
XCLK	External Clock Input	564.8	4623.7
V_{CCD2}	V_{CC} Digital Power Supply	387.9	4623.7
V_{CCD1}	V_{CC} Digital Power Supply	169.5	4623.7
SCLK	Slave Clock	–14.7	4623.7
SS	Slave Select	–198.1	4623.7
MOSI	Master Out Slave In	–1063.7	4623.7
MISO	Master In Slave Out	–1325.6	4623.7
V_{SSD1}	V_{SS} Digital Power Supply	–1655.3	4623.7
V_{SSD2}	V_{SS} Digital Power Supply	–1836.9	4623.7

1. *Double bond recommended.*

ORDERING INFORMATION

Product Number Descriptor Key

ISD4004– _ _ _ _ _

Product Family
ISD4000 Family

Product Series
04 = Fourth Series (8–16 min)

Duration:
08M=8 minutes
10M=10 minutes
12M=12 minutes
16M=16 minutes

Special Temperature Field:
Blank= Commercial Packaged (0°C to +70°C)
or Commercial Die (0°C to +50°C)
D = Extended (–20°C to +70°C)
I = Industrial (–40°C to +85°C)

Package Type:
E = 28-Lead 8x13.4mm Plastic Thin Small Outline Package (TSOP) Type 1
P = 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP)
S = 28-Lead 0.300-Inch Plastic Small Outline Package (SOIC)
X = Die

When ordering ISD4004 series devices, please refer to the following valid part numbers.

Part Number	Part Number	Part Number	Part Number
ISD4004-08ME	ISD4004-10ME	ISD4004-12ME	ISD4004-16ME
ISD4004-08MED	ISD4004-10MED	ISD4004-12MED	ISD4004-16MED
ISD4004-08MEI	ISD4004-10MEI	ISD4004-12MEI	ISD4004-16MEI
ISD4004-08MP	ISD4004-10MP	ISD4004-12MP	ISD4004-16MP
ISD4004-08MS	ISD4004-10MS	ISD4004-12MS	ISD4004-16MS
ISD4004-08MSI	ISD4004-10MSI	ISD4004-12MSI	ISD4004-16MSI
ISD4004-08MX	ISD4004-10MX	ISD4004-12MX	ISD4004-16MX

For the latest product information, access ISD's worldwide website at http://www.isd.com.

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