**Table 11: AC Parameters** (Die)

| Symbol | Characteristic | | Min(2) | Typ(1) | Max(2) | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $F_S$ | Sampling Frequency | ISD4003-04M | | 8.0 | | KHz | (5) |
| | | ISD4003-05M | | 6.4 | | KHz | (5) |
| | | ISD4003-06M | | 5.3 | | KHz | (5) |
| | | ISD4003-08M | | 4.0 | | KHz | (5) |
| $F_{CF}$ | Filter Pass Band | ISD4003-04M | | 3.4 | | KHz | 3dB Roll-Off Point (3) (6) |
| | | ISD4003-05M | | 2.7 | | KHz | 3dB Roll-Off Point (3) (6) |
| | | ISD4003-06M | | 2.3 | | KHz | 3dB Roll-Off Point (3) (6) |
| | | ISD4003-08M | | 1.7 | | KHz | 3dB Roll-Off Point (3) (6) |
| $T_{REC}$ | Record Duration | ISD4003-04M | | 4 | | min | (5) |
| | | ISD4003-05M | | 5 | | min | (5) |
| | | ISD4003-06M | | 6 | | min | (5) |
| | | ISD4003-08M | | 8 | | min | (5) |
| $T_{PLAY}$ | Playback Duration | ISD4003-04M | | 4 | | min | (5) |
| | | ISD4003-05M | | 5 | | min | (5) |
| | | ISD4003-06M | | 6 | | min | (5) |
| | | ISD4003-08M | | 8 | | min | (5) |
| $T_{PUD}$ | Power-Up Delay | ISD4003-04M | | 25 | | msec | |
| | | ISD4003-05M | | 31.25 | | msec | |
| | | ISD4003-06M | | 37.5 | | msec | |
| | | ISD4003-08M | | 50 | | msec | |
| $T_{STOP}$ or $T_{PAUSE}$ | Stop or Pause in Record or Play | ISD4003-04M | | 50 | | msec | |
| | | ISD4003-05M | | 62.5 | | msec | |
| | | ISD4003-06M | | 75 | | msec | |
| | | ISD4003-08M | | 100 | | msec | |
| $T_{RAC}$ | RAC Clock Period | ISD4003-04M | | 200 | | msec | (9) |
| | | ISD4003-05M | | 250 | | msec | (9) |
| | | ISD4003-06M | | 300 | | msec | (9) |
| | | ISD4003-08M | | 400 | | msec | (9) |
| $T_{RACLO}$ | RAC Clock Low Time | ISD4003-04M | | 25 | | msec | |
| | | ISD4003-05M | | 31.25 | | msec | |
| | | ISD4003-06M | | 37.5 | | msec | |
| | | ISD4003-08M | | 50 | | msec | |
| $T_{RACM}$ | RAC Clock Period in Message Cueing Mode | ISD4003-04M | | 125 | | µsec | |
| | | ISD4003-05M | | 156.3 | | µsec | |
| | | ISD4003-06M | | 187.5 | | µsec | |
| | | ISD4003-08M | | 250 | | µsec | |
| $T_{RACML}$ | RAC Clock Low Time in Message Cueing Mode | ISD4003-04M | | 15.63 | | µsec | |
| | | ISD4003-05M | | 19.53 | | µsec | |
| | | ISD4003-06M | | 23.44 | | µsec | |
| | | ISD4003-08M | | 31.25 | | µsec | |

## Table 11: AC Parameters (Die)

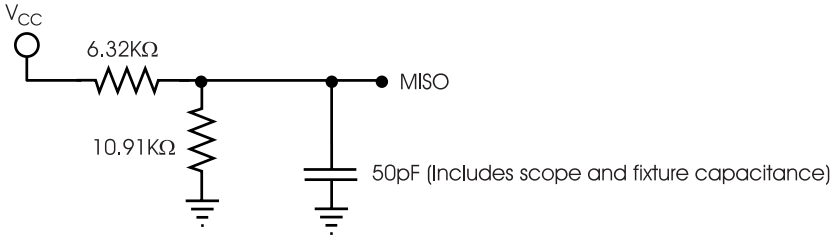
| Symbol | Characteristic | Min(2) | Typ(1) | Max(2) | Units | Conditions |
|---|---|---|---|---|---|---|
| THD | Total Harmonic Distortion | | 1 | 2 | % | @ 1 KHz |
| $V_{IN}$ | ANA IN Input Voltage | | | 32 | mV | Peak-to-Peak[4,7,8] |

1. *Typical values: $T_A$ = 25°C and 3.0 V.*
2. *All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cut off depends upon the value of external capacitors (see Pin Descriptions).*
4. *Single-ended input mode. In the differential input mode, $V_{IN}$ maximum for ANA IN+ and ANA IN– is 16 mV peak-to-peak.*
5. *Sampling Frequency and Duration can vary as much as ±2.25 percent over the commercial temperature and voltage ranges. For greater stability, an external clock can be utilized (see Pin Descriptions).*
6. *Filter specification applies to the antialiasing filter and to the smoothing filter.*
7. *The typical output voltage will be approximately 570 mV peak-to-peak with $V_{IN}$ at 32 mV peak-to-peak.*
8. *For optimal signal quality, this maximum limit is recommended.*
9. *When a record command is sent, $T_{RAC} = T_{RAC} + T_{RACLO}$ on the first row addressed.*

## Table 12: SPI AC Parameters[1]

| Symbol | Characteristics | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $T_{SSS}$ | $\overline{SS}$ Setup Time | 500 | | nsec | |
| $T_{SSH}$ | $\overline{SS}$ Hold Time | 500 | | nsec | |
| $T_{DIS}$ | Data in Setup Time | 200 | | nsec | |
| $T_{DIH}$ | Data in Hold Time | 200 | | nsec | |
| $T_{PD}$ | Output Delay | | 500 | nsec | |
| $T_{DF}$(2) | Output Delay to hiZ | | 500 | nsec | |
| $T_{SSmin}$ | $\overline{SS}$ HIGH | 1 | | µsec | |
| $T_{SCKhi}$ | SCLK High Time | 400 | | nsec | |
| $T_{SCKlow}$ | SCLK Low Time | 400 | | nsec | |
| $F_0$ | CLK Frequency | | 1,000 | KHz | |

1. *Typical values: $T_A$= 25°C and 3.0 V. Timing measured at 50 percent of the $V_{CC}$ level.*
2. *Tristate test condition.*



# TIMING DIAGRAMS

**Figure 6: Timing Diagram**

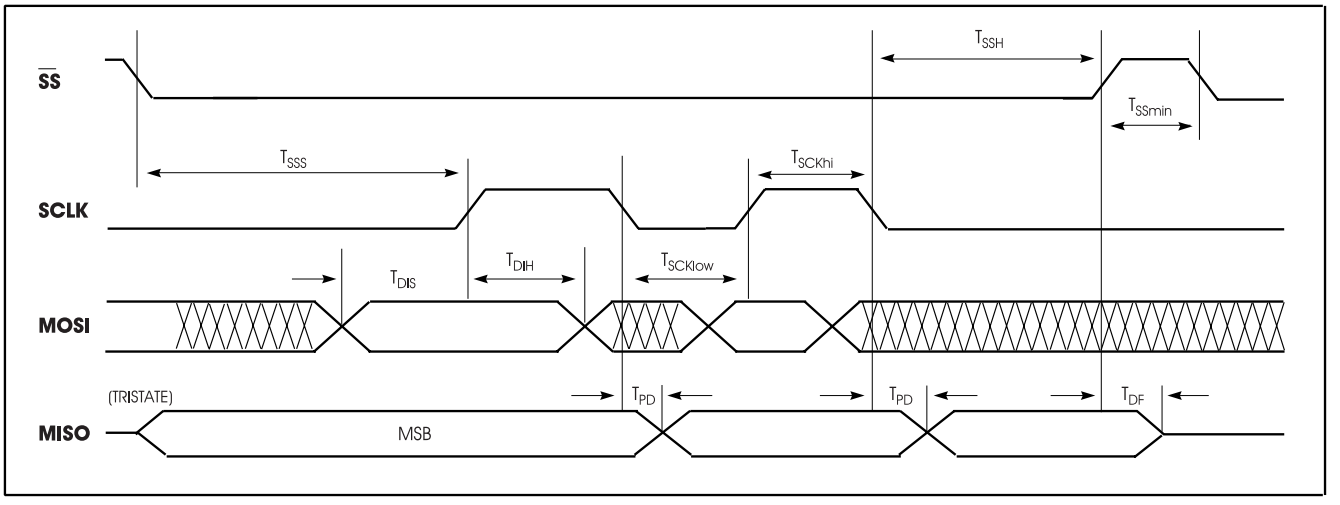



**Figure 7: 8-Bit Command Format**

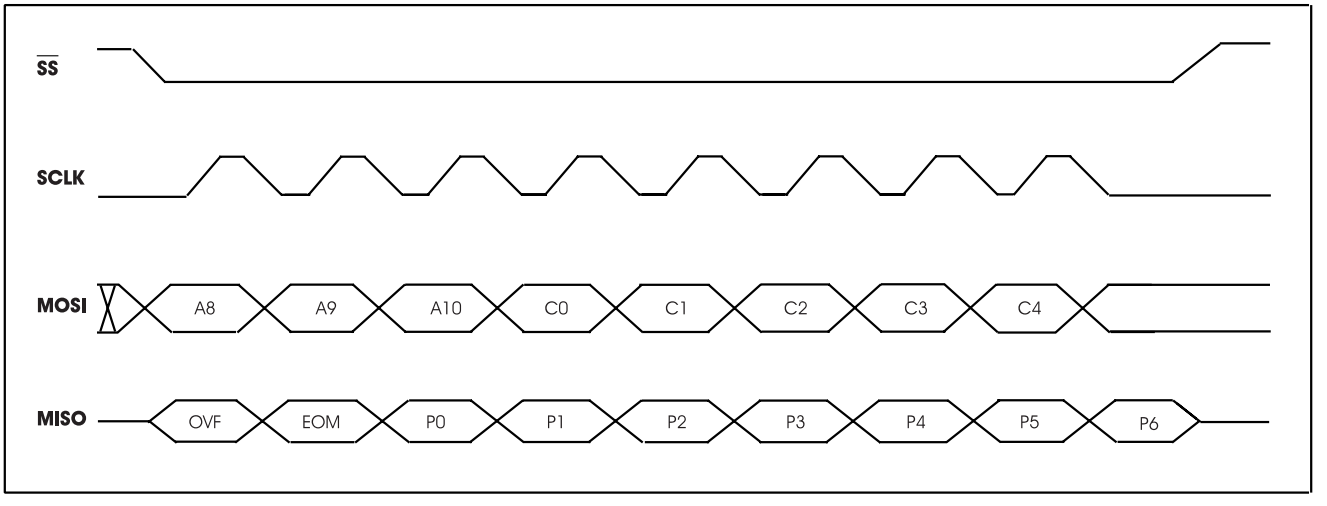


**Figure 8: 16-Bit Command Format**

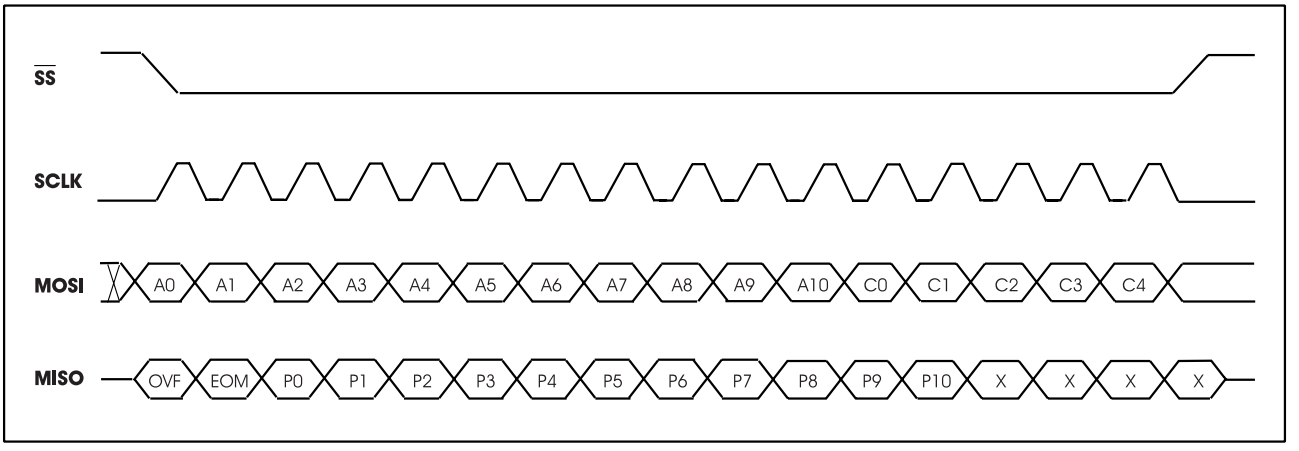
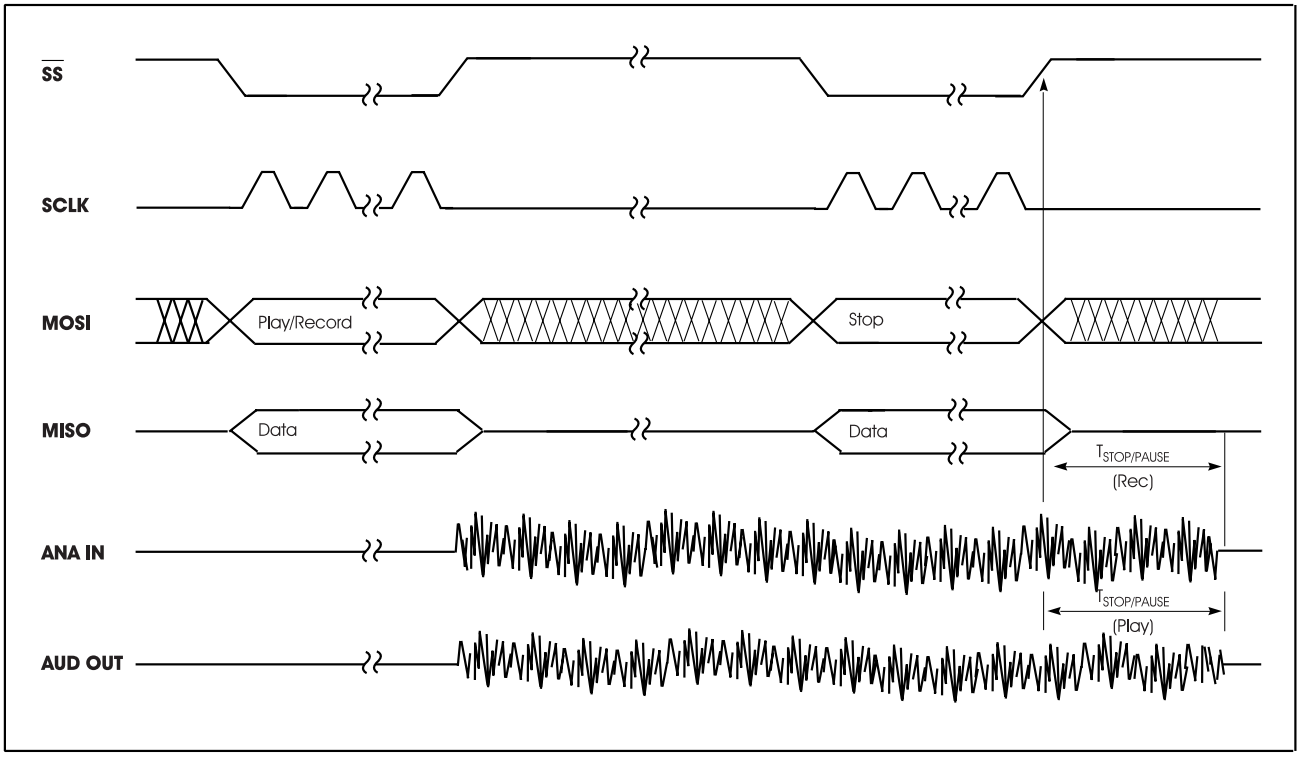
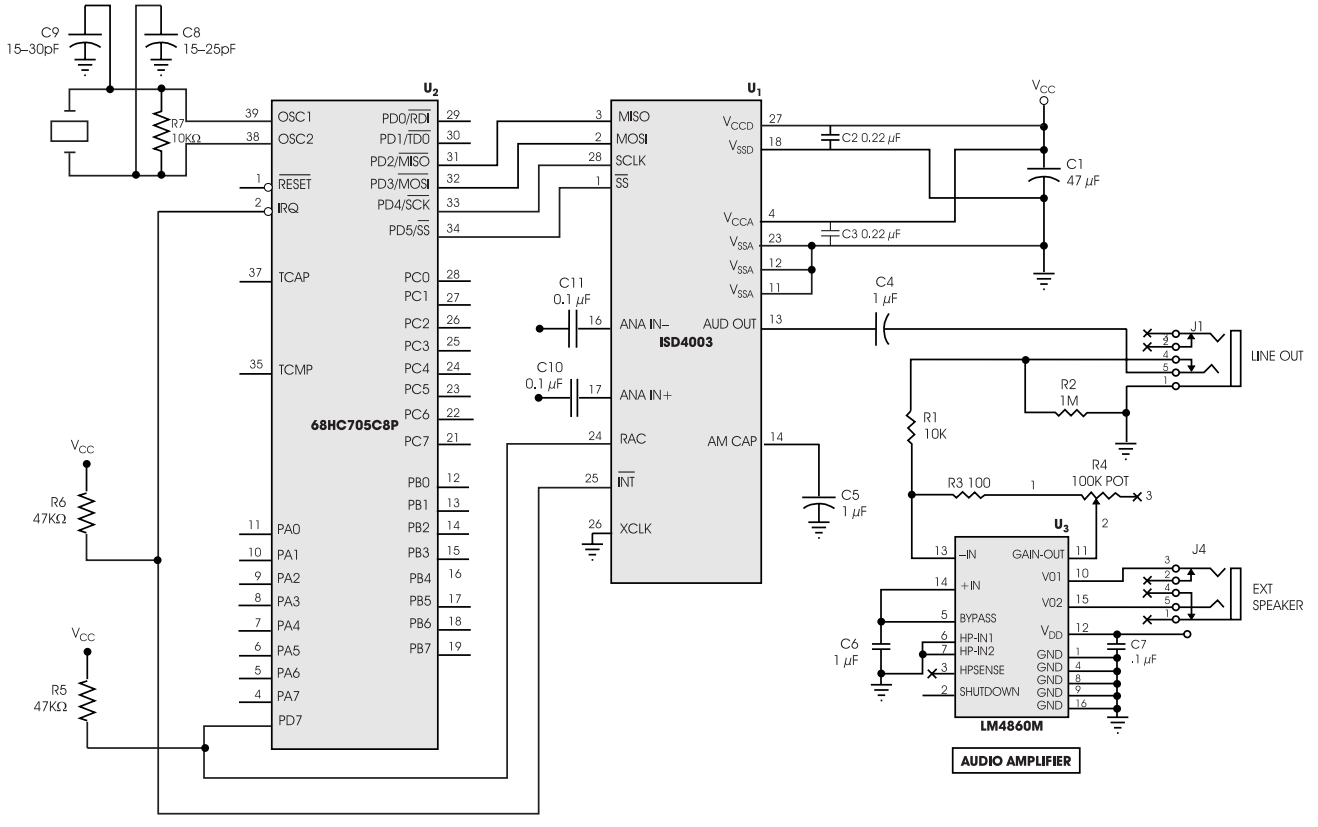



**Figure 9: Playback/Record and Stop Cycle**

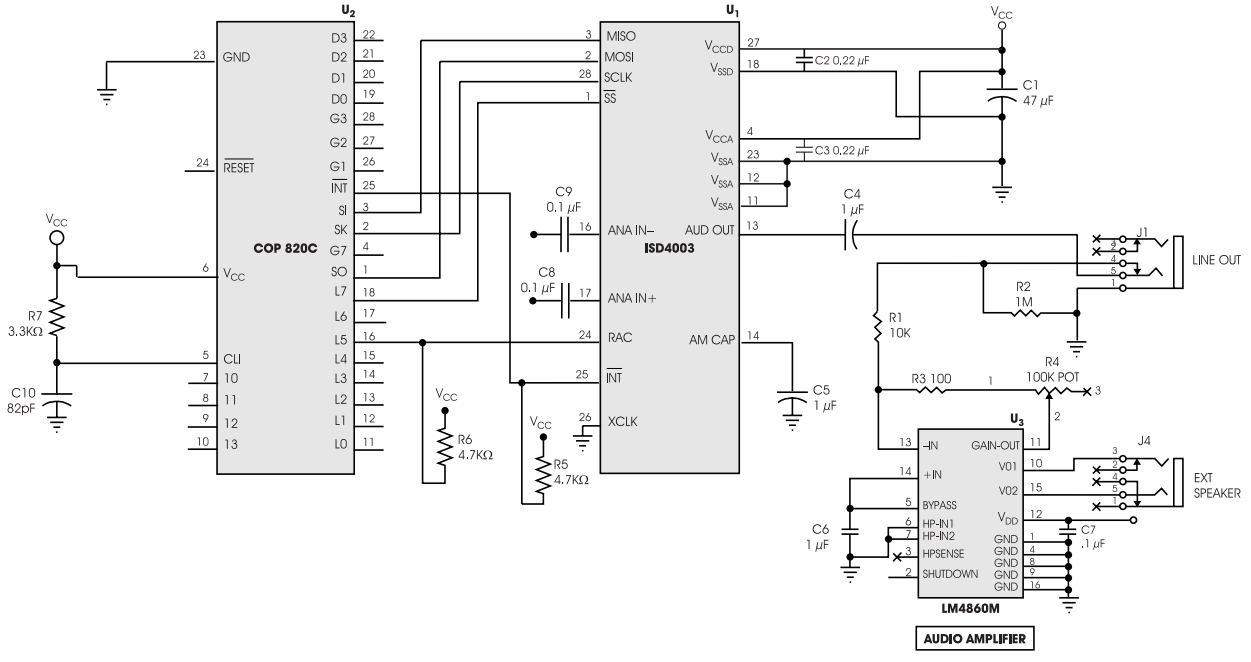


## Figure 10: Application Example Using SPI(1)



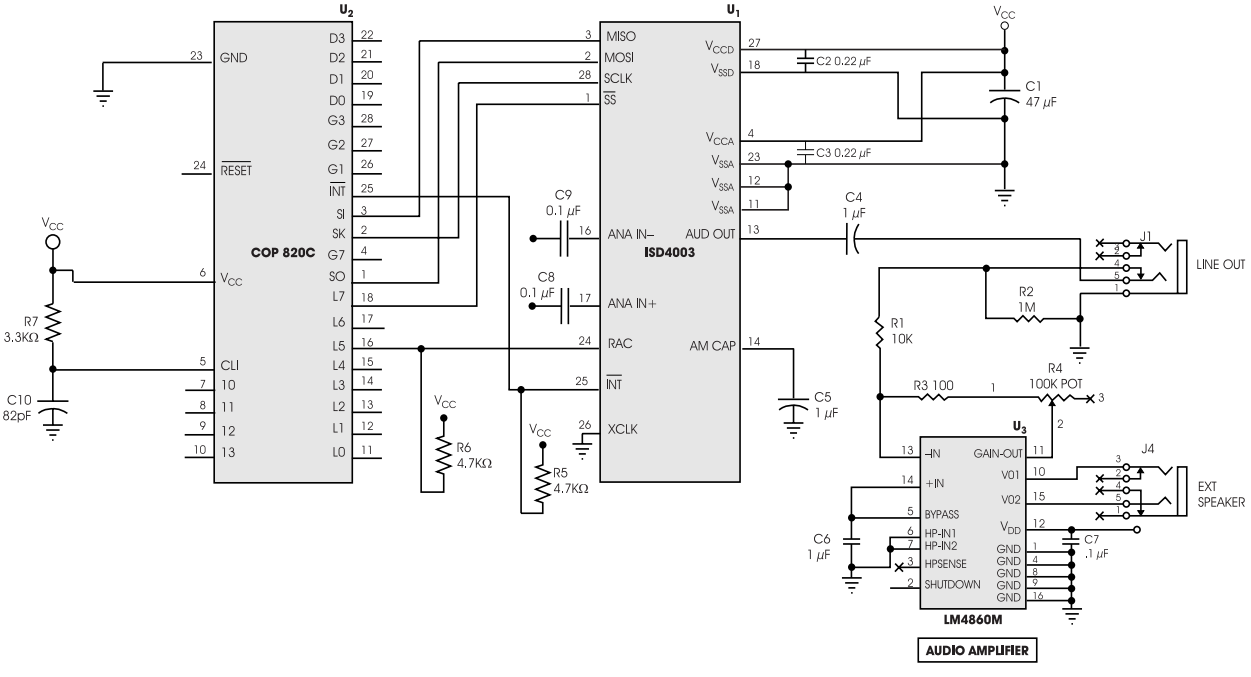

1. *This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.*
2. *Please make sure the bypass capacitor, C2 is as close as possible to the package.*

## Figure 11: Application Example Using Microwire(1)



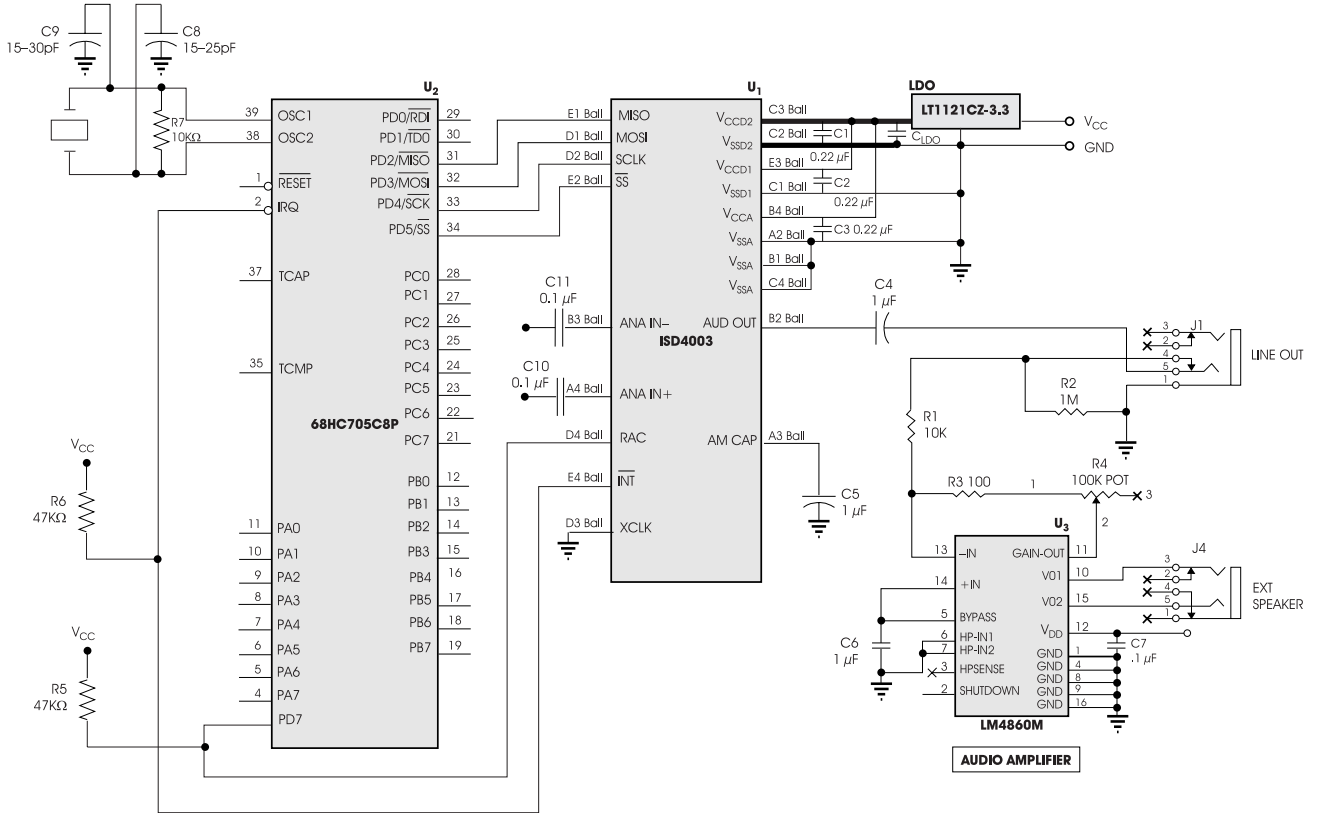

1. *This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.*
2. *Please make sure the bypass capacitor, C2 is as close as possible to the package.*

## Figure 12: Application Example Using SPI Port on Microcontroller(1)




1. *This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.*
2. *Please make sure the bypass capacitor, C2 is as close as possible to the package.*

## Figure 13: Application Example Using SPI with a Chip Scale Packaged Device




1. *This application example is for illustration purposes only. ISD makes no representation or warranty that such application will be suitable for production.*
2. *Please make sure all bypass capacitors are as close as possible to the package.*
3. *Ground plane must be used to connect all $V_{SSA}$ pins together. If a ground plane is not available then a short and low impedance path is necessary.*
4. *Route ANA IN+ and ANA IN– away from $V_{CCD}$ and $V_{SSD}$ return paths.*
5. *Biasing for electret microphone must come from $V_{CCA}$ and $V_{SSA}$.*
6. *AMCAP must return to $V_{SSA}$.*
7. *Traces from $V_{CCD2}$ to the LDO (Low Dropout regulator) and from $V_{SSD2}$ to the LDO ground should be as thick as possible. The distance between these two traces should be as short as possible.*

# DEVICE PHYSICAL DIMENSIONS

**Figure 14: 28-Lead 8x13.4 mm Plastic Thin Small Outline Package (TSOP) Type I (E)**

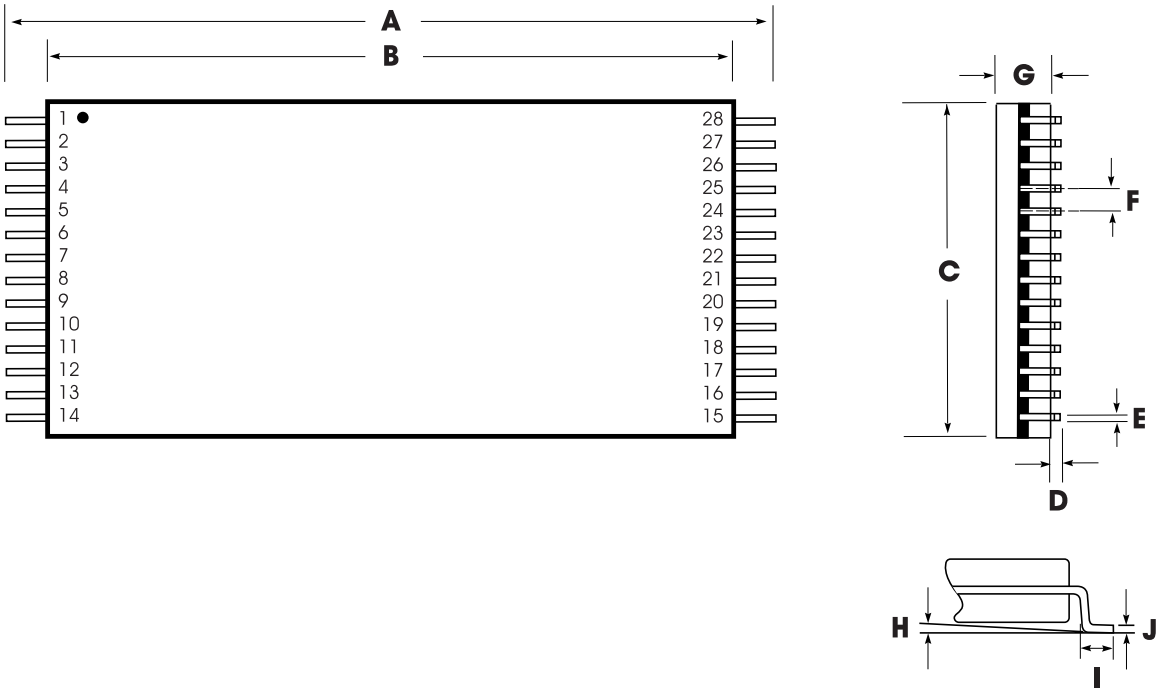



**Table 13: Plastic Thin Small Outline Package (TSOP) Type I (E) Dimensions**

| | INCHES | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.520 | 0.528 | 0.535 | 13.20 | 13.40 | 13.60 |
| B | 0.461 | 0.465 | 0.469 | 11.70 | 11.80 | 11.90 |
| C | 0.311 | 0.315 | 0.319 | 7.90 | 8.00 | 8.10 |
| D | 0.002 | | 0.006 | 0.05 | | 0.15 |
| E | 0.007 | 0.009 | 0.011 | 0.17 | 0.22 | 0.27 |
| F | | 0.0217 | | | 0.55 | |
| G | 0.037 | 0.039 | 0.041 | 0.95 | 1.00 | 1.05 |
| H | 0° | 3° | 6° | 0° | 3° | 6° |
| I | 0.020 | 0.022 | 0.028 | 0.50 | 0.55 | 0.70 |
| J | 0.004 | | 0.008 | 0.10 | | 0.21 |

***NOTE:*** *Lead coplanarity to be within 0.004 inches.*

**Figure 15: 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP) (P)**

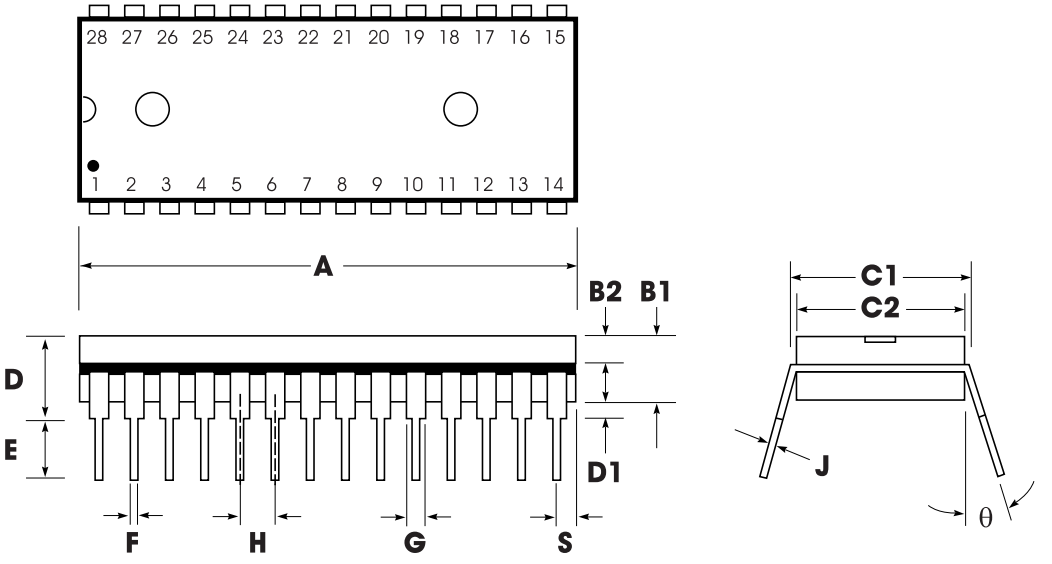



**Table 14: Plastic Dual Inline Package (PDIP) (P) Dimensions**

| | INCHES | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 1.445 | 1.450 | 1.455 | 36.70 | 36.83 | 36.96 |
| B1 | | 0.150 | | | 3.81 | |
| B2 | 0.065 | 0.070 | 0.075 | 1.65 | 1.78 | 1.91 |
| C1 | 0.600 | | 0.625 | 15.24 | | 15.88 |
| C2 | 0.530 | 0.540 | 0.550 | 13.46 | 13.72 | 13.97 |
| D | | | 0.19 | | | 4.83 |
| D1 | 0.015 | | | 0.38 | | |
| E | 0.125 | | 0.135 | 3.18 | | 3.43 |
| F | 0.015 | 0.018 | 0.022 | 0.38 | 0.46 | 0.56 |
| G | 0.055 | 0.060 | 0.065 | 1.40 | 1.52 | 1.65 |
| H | | 0.100 | | | 2.54 | |
| J | 0.008 | 0.010 | 0.012 | 0.20 | 0.25 | 0.30 |
| S | 0.070 | 0.075 | 0.080 | 1.78 | 1.91 | 2.03 |
| q | 0° | | 15° | 0° | | 15° |

**Figure 16: 28-Lead 0.300-Inch Plastic Small Outline Integrated Circuit (SOIC) (S)**

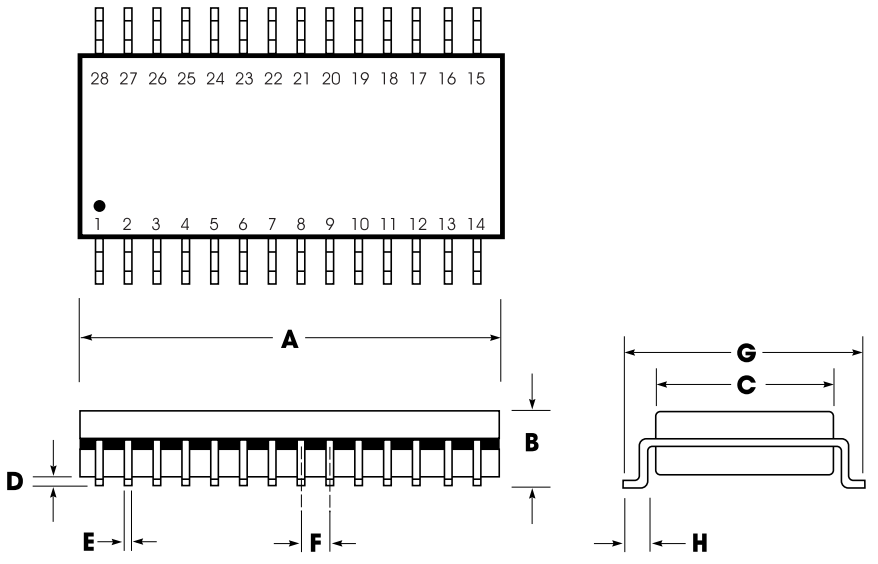



**Table 15: Plastic Small Outline Integrated Circuit (SOIC) (S) Dimensions**

| | INCHES | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.701 | 0.706 | 0.711 | 17.81 | 17.93 | 18.06 |
| B | 0.097 | 0.101 | 0.104 | 2.46 | 2.56 | 2.64 |
| C | 0.292 | 0.296 | 0.299 | 7.42 | 7.52 | 7.59 |
| D | 0.005 | 0.009 | 0.0115 | 0.127 | 0.22 | 0.29 |
| E | 0.014 | 0.016 | 0.019 | 0.35 | 0.41 | 0.48 |
| F | | 0.050 | | | 1.27 | |
| G | 0.400 | 0.406 | 0.410 | 10.16 | 10.31 | 10.41 |
| H | 0.024 | 0.032 | 0.040 | 0.61 | 0.81 | 1.02 |

***NOTE:*** *Lead coplanarity to be within 0.004 inches.*

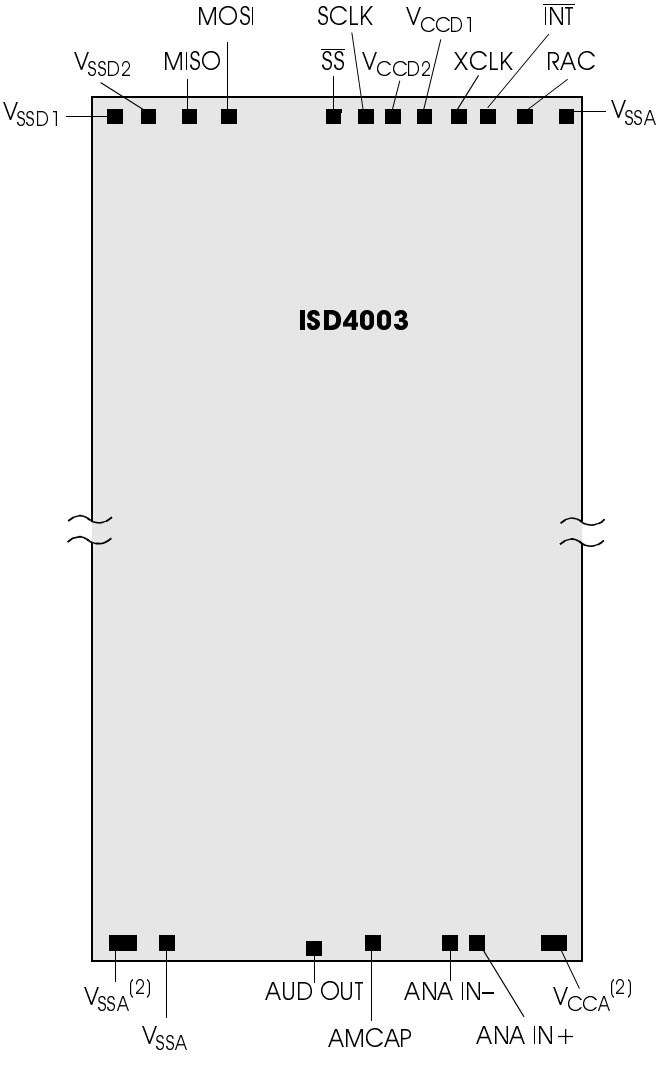
**Figure 17: ISD4003 Series Bonding Physical Layout[1]** (Unpackaged Die)

**ISD4003 Series**

**I.** Die Dimensions
X: 166.6 ±1 mils
Y: 274.9 ±1 mils

**II.** Die Thickness
11.5 ±0.5 mils

**III.** Pad Opening (min)
90 x 90 microns
3.5 x 3.5 mils



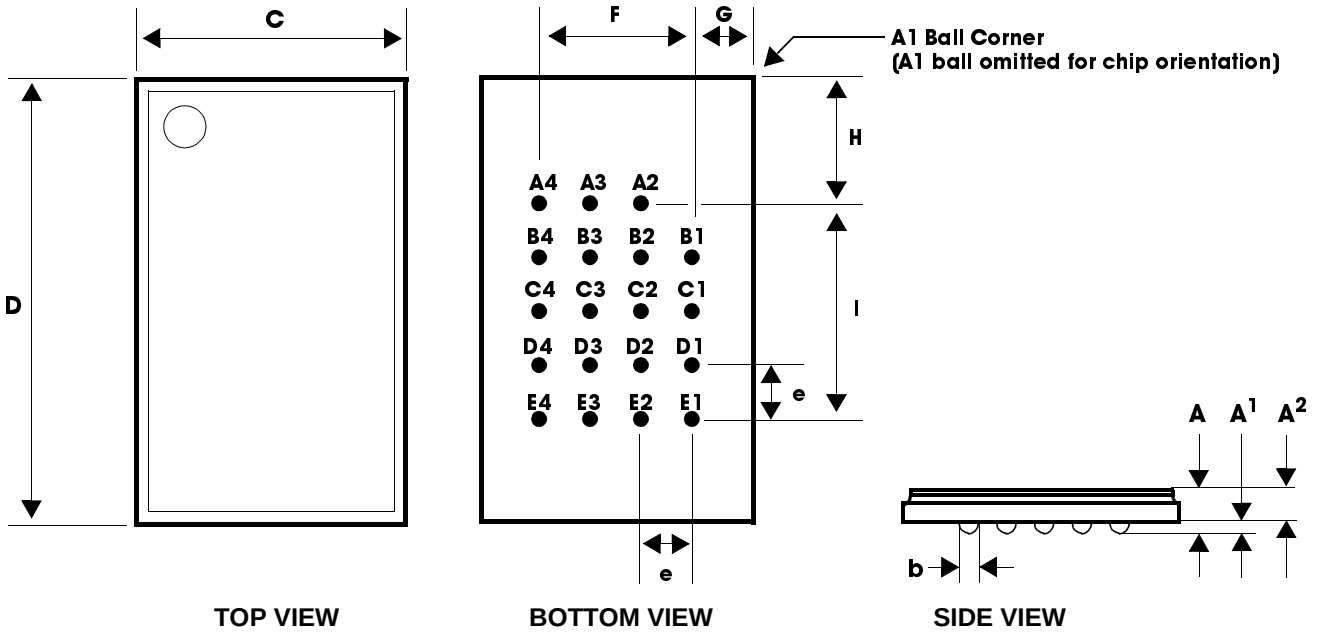

1. *The backside of die is internally connected to $V_{SS}$. It **MUST NOT** be connected to any other potential or damage may occur.*
2. *Double bond recommended.*
3. *This figure reflects the current die thickness. Please contact ISD as this thickness may change in the future.*

**Table 16: ISD4003 Series Device Pin/Pad Designations, with Respect to Die Center (µm)**

| Pin | Pin Name | X Axis | Y Axis |
|---|---|---|---|
| $V_{SSA}$ | $V_{SS}$ Analog Power Supply | –1898.1 | –3272.4 |
| $V_{SSA}$ | $V_{SS}$ Analog Power Supply | –1599.9 | –3272.4 |
| AUD OUT | Audio Output | 281.9 | –3272.4 |
| AMCAP | AutoMute | 577.3 | –3272.4 |
| ANA IN – | Inverting Analog Input | 1449.3 | –3272.4 |
| ANA IN + | Noninverting Analog Input | 1603.5 | –3272.4 |
| $V_{CCA}$[1] | $V_{CC}$ Analog Power Supply | 1898.7 | –3272.4 |
| $V_{SSA}$ | $V_{SS}$ Analog Power Supply | 1885.2 | 3273.7 |
| RAC | Row Address Clock | 1483.8 | 3273.7 |
| INT | Interrupt | 794.8 | 3273.7 |
| XCLK | External Clock Input | 564.8 | 3273.7 |
| $V_{CCD2}$ | $V_{CC}$ Digital Power Supply | 384.9 | 3273.7 |
| $V_{CCD1}$ | $V_{CC}$ Digital Power Supply | 169.5 | 3273.7 |
| SCLK | Slave Clock | –14.7 | 3273.7 |
| SS | Slave Select | –198.1 | 3273.7 |
| MOSI | Master Out Slave In | –1063.7 | 3273.7 |
| MISO | Master In Slave Out | –1325.6 | 3273.7 |
| $V_{SSD1}$ | $V_{SS}$ Digital Power Supply | –1665.3 | 3273.7 |
| $V_{SSD2}$ | $V_{SS}$ Digital Power Supply | –1836.9 | 3273.7 |

***1.*** *Double bond recommended.*

## Figure 18: ISD4003 Chip Scale Package (CSP) (Z)




## Table 17: CSP Dimensions

| Symbol | Min. | Nom. | Max. |
|---|---|---|---|
| A | — | — | 0.85 |
| $A^1$ | 0.15 | — | — |
| $A^2$ | — | 0.55 | — |
| b | 0.30 | 0.35 | 0.40 |
| C | — | 4.70 | — |
| D | — | 7.45 | — |
| e | | 0.75 | |
| F | — | 2.25 | — |
| G | — | 1.22 | — |
| H | — | 2.22 | — |
| I | — | 3.00 | — |

| Name | Ball Location | TSOP Pin # |
|---|---|---|
| $V_{SSA}$ | A2 | 18 |
| AMCAP | A3 | 22 |
| ANAIN+ | A4 | 25 |
| $V_{SSA}$ | B1 | 17 |
| AUDOUT | B2 | 20 |
| ANAIN– | B3 | 24 |
| $V_{CCA}$ | B4 | 26 |
| $V_{SSD1}$ | C1 | 12 |
| $V_{SSD2}$ | C2 | N/A |
| $V_{CCD2}$ | C3 | N/A |
| $V_{SSA}$ | C4 | 1 |
| MOSI | D1 | 10 |
| SCLK | D2 | 8 |
| XCLK | D3 | 6 |
| RAC | D4 | 2 |
| MISO | E1 | 11 |
| SS | E2 | 9 |
| $V_{CCD1}$ | E3 | 7 |
| INT | E4 | 5 |

# ORDERING INFORMATION

## *Product Number Descriptor Key*

**ISD4003–** _ _ _ _ _

**Product Family**
ISD4000 Family

**Product Series**
03 = Third Series (4–8 min)

**Duration:**
04M = 4 minutes
05M = 5 minutes
06M = 6 minutes
08M = 8 minutes

**Special Temperature Field:**
**Blank** = Commercial Packaged (0°C to +70°C)
or Commercial Die (0°C to +50°C)
**D** = Extended (–20°C to +70°C)
**I** = Industrial (–40°C to +85°C)

**Package Type:**
**E** = 28-Lead 8x13.4mm Plastic Thin Small Outline Package (TSOP) Type 1
**P** = 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP)
**S** = 28-Lead 0.300-Inch Plastic Small Outline Package (SOIC)
**X** = Die
**Z** = Chip Scale Package (CSP)

When ordering ISD4003 series devices, please refer to the following valid part numbers.

| Part Number | Part Number | Part Number | Part Number |
|---|---|---|---|
| ISD4003-04ME | ISD4003-05ME | ISD4003-06ME | ISD4003-08ME |
| ISD4003-04MED | ISD4003-05MED | ISD4003-06MED | ISD4003-08MED |
| ISD4003-04MEI | ISD4003-05MEI | ISD4003-06MEI | ISD4003-08MEI |
| ISD4003-04MP | ISD4003-05MP | ISD4003-06MP | ISD4003-08MP |
| ISD4003-04MS | ISD4003-05MS | ISD4003-06MS | ISD4003-08MS |
| ISD4003-04MSI | ISD4003-05MSI | ISD4003-06MSI | ISD4003-08MSI |
| ISD4003-04MX | ISD4003-05MX | ISD4003-06MX | ISD4003-08MX |
| ISD4003-04MZ | ISD4003-05MZ | ISD4003-06MZ | ISD4003-08MZ |
| ISD4003-04MZD | ISD4003-05MZD | ISD4003-06MZD | ISD4003-08MZD |
| ISD4003-04MZI | ISD4003-05MZI | ISD4003-06MZI | ISD4003-08MZI |

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