FEDS5424331-01

OKI Semiconductor

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MSM5424331

222,720-Word × 24-Bit Field Memory

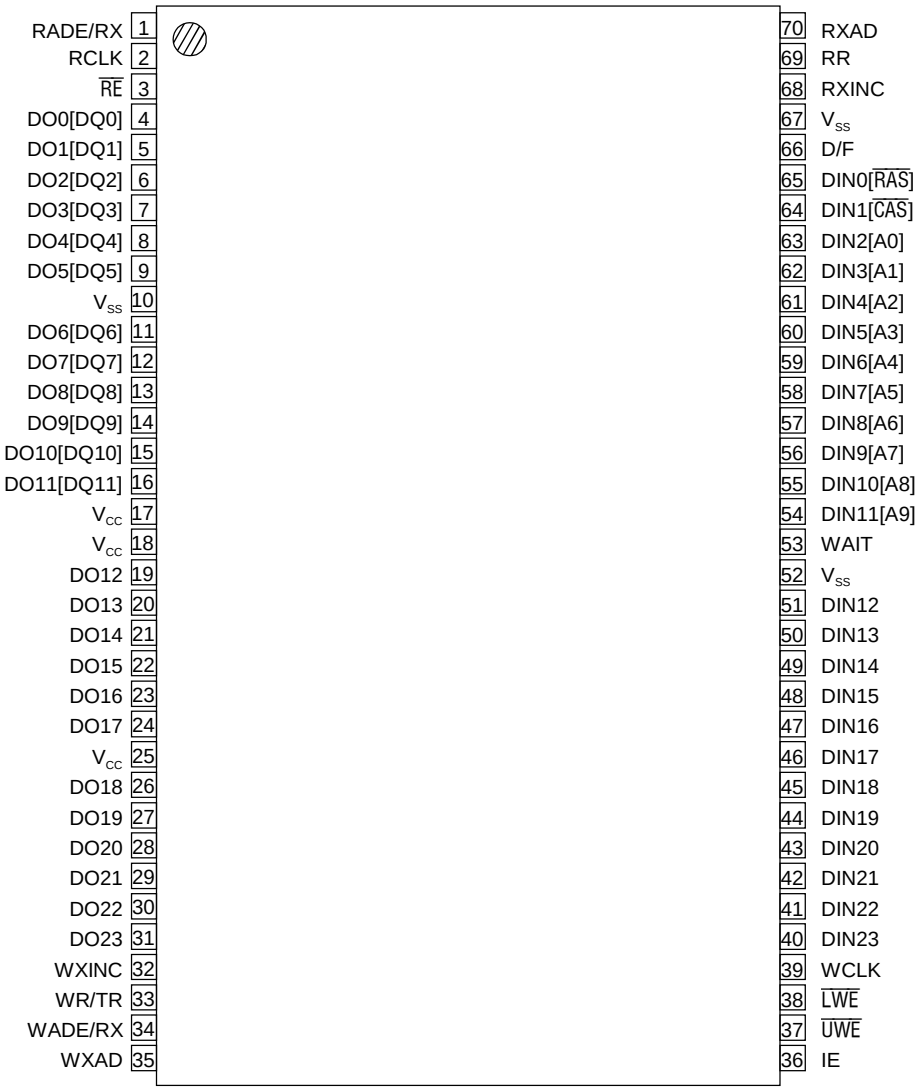
GENERAL DESCRIPTION

The MSM5424331 is an image data processing field memory organized as 222,720 (768 pixels by 290 lines) by 24 bits that can switch between the FIFO mode where the MSM5424331 is used as an ordinary field memory and a block access mode where the MSM5424331 can easily exchange data with personal computer and the like.
Serial writing in and serial reading from the MSM5424331 are performed line by line. In the FIFO mode, any line can be selected by specifying their addresses by the Serial Address input. In the Block Access mode, any line or word address (10 bits) can be set by entering the address through the address multiplexer.
As the MSM5424331 in the Block Access mode can be controlled by $\overline{RAS}$ and $\overline{CAS}$ signals, it can easily interface to the MPU.
The MSM5424331 contains dynamic memory cells. In the FIFO mode, the memory cells are automatically refreshed by the self refresh control circuit, but in the Block Access mode, the memory cells must be refreshed by the $\overline{CAS}$ before $\overline{RAS}$ Refresh function.
The MSM5424331 is not designed for high end use in such applications as medical systems, professional graphics systems which require long term picture storage, data storage systems and others.

FEATURES

- Switching between FIFO and Block Access modes by the D/F pin
  FIFO mode: Serial write/read operation by line-by-line accessing
  Block Access mode: Fast write/read operation on an 8-word basis by the $\overline{RAS}$ and $\overline{CAS}$ control
- Organization of 768 × 290 × 24 bits
  FIFO mode: Input × 12 or × 24 controlled by $\overline{L/UWE}$
  Output × 24
  Block Access mode: Input × 12 (Two 768 × 290 × 12-bit banks are controlled by $\overline{L/UWE}$.)
  Output × 12 (Two 768 × 290 × 12-bit banks are controlled by A9.)
- Asynchronous operation
  Input and output asynchronous operation enabled only in the FIFO mode Single write or read operation in the Block Access mode
- Serial Read and Write Cycle times (in both the FIFO mode and the Block Access mode)
  Cycle time: 60 ns
  Access time: 50 ns
- Operating supply voltage: 2.8 to 3.3 V
- Refresh
  FIFO mode: Self refresh
  Block Access mode: by the $\overline{CAS}$ before $\overline{RAS}$ refresh function (290 cycles/8 ms)
- Address input
  FIFO mode: Setting random line address by the serial address input
  Block Access mode: Setting random address in the address multiplexer by the $\overline{RAS}$ and $\overline{CAS}$ control
- Selectable serial address input setting or various address resetting in the FIFO mode
- Package:
  70-pin 400 mil plastic TSOP (Type 2) (TSOP(2)70-P-400-0.50-K) (Product: MSM5424331TS-AK)

PIN CONFIGURATION (TOP VIEW)

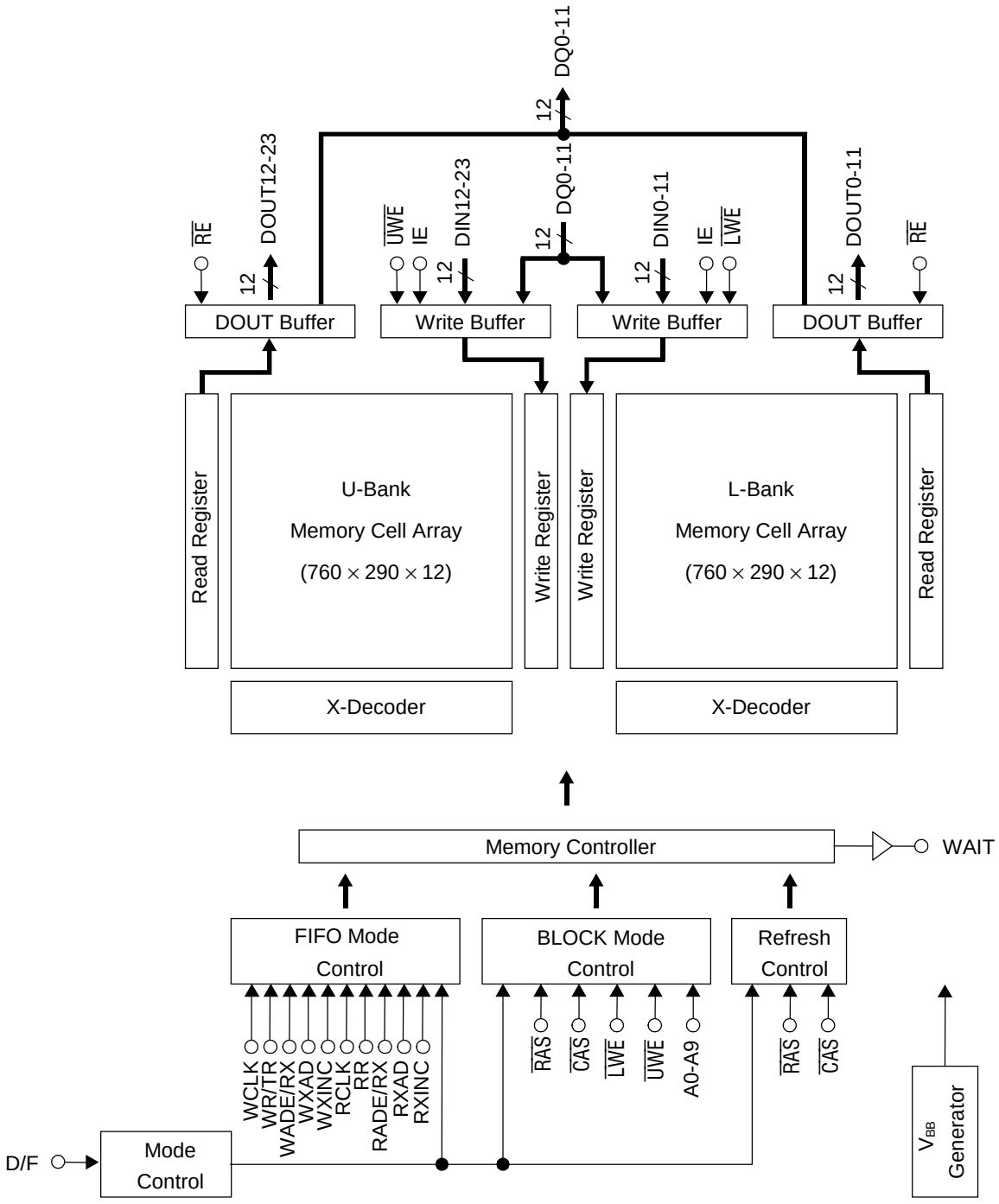


70-Pin Plastic TSOP (2)
(K Type)

Pin Name		FIFO Mode		Block Mode
FIFO Mode	Block Mode	Address Setting Cycle	Serial Read/Write Cycle	
RCLK		Read X Serial Address Strobe	Serial Read Clock	—
$\overline{RE}$	$\overline{RE}$	—	Read Enable	Read Enable
DO0 - 11	DQ0 - 11	—	Data Output	Data Input/Output
DO12 - 23		—	Data Output	—
RR		Read Address Reset Mode Enable	—	—
RXINC		Read X Address Increment	—	—
RADE/RX		Read X Address Input Enable Read X Address Reset	—	—
RXAD		Read X Serial Address Data	—	—
WCLK		Write X Serial Address Strobe	Serial Write Clock	—
$\overline{LWE}$	$\overline{LWE}$	—	Write Enable	Write Enable
$\overline{UWE}$	$\overline{UWE}$	—	Write Enable	Write Enable
IE		—	Input Enable	—
DIN0	$\overline{RAS}$	—	Data Input	X Address Strobe
DIN1	$\overline{CAS}$	—	Data Input	Y Address Strobe
DIN2 - 11	A0 - A9	—	Data Input	Address Input
DIN12 - 23		—	Data Input	—
WR/TR		Write Address Reset Mode Enable	Write Data Transfer	—
WXINC		Write X Address Increment	—	—
WADE/RX		Write X Address Input Enable Write X Address Reset	—	—
WXAD		Write X Serial Address Data	—	—
	WAIT	—	—	External Synchronous Signal
D/F	D/F	Mode Change (D/F = L)		Mode Change (D/F = H)
V_{CC}		Power Supply Voltage (3.0 V)		
V_{SS}		Ground (0 V)		

Note: Same power supply voltage level must be provided to every V_{CC} pin.
Same ground voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



PIN FUNCTION

Read Related

D/F
This signal switches between the FIFO mode and the Block Access mode. The FIFO mode is selected when this signal is low "L" and the Block Access mode is selected when this signal is high "H".

RCLK: Read Clock
RCLK is the read control clock input in the FIFO mode. Synchronized with RCLK's rising edge, serial read access from read ports is executed when $\overline{RE}$ is low.
The internal counter for the serial read address is incremented automatically on the rising edge of RCLK. In a read address set cycle, all the read address bits which were input from RXAD pin are stored into internal address registers synchronized with RCLK. In this address set cycle, RADE/RX must be held high and RR must be held low.
In the read address reset cycle, various read address reset modes can be set synchronously with RCLK. These reset cycles work to replace complicated serial address control which requires many RCLK clocks with a simple reset cycle control requiring only a single RCLK cycle. It greatly facilitates memory access.
In the Block Access mode, the RCLK signal is ignored.

$\overline{RE}$: Read Enable
$\overline{RE}$ is a read enable clock input in the FIFO mode. $\overline{RE}$ enables or disables both internal read address pointers and data-out buffers. When $\overline{RE}$ is low, the internal read address pointer is incremented synchronously with RCLK. When $\overline{RE}$ is high, even if the RCLK is input, the internal read address pointer is not incremented.
The output pins are enabled in the read cycle of the Block Access mode when this pin ($\overline{RE}$) is low "L".

RR: Read Reset
RR is a read reset control input in the FIFO mode. Read address reset modes are defined when RR level is high according to the "FUNCTION TABLE for read".
In the Block Access mode, the RR signal is ignored.

RXINC: Read X Address Increment
RXINC is a read X address (or line address) increment control input in the FIFO mode. In the read address reset cycle, defined by RR high, the X address (or line address) is incremented by 1 when RXINC is pulled high with RADE/RX low.
In the Block Access mode, the RXINC signal is ignored.

RADE/RX: Read Address Enable/Read X Address Reset Logic Function
RADE/RX is a dual function control input in the FIFO mode. RADE, one of the two functions of RADE/RX, is a read address enable input. In the read address set cycle, X address (or line address) input from the RXAD pin is latched into internal read X address register synchronously with RCLK.
RX, the second function of RADE/RX, works as an element to set read X address (or line address) reset mode. In an address reset mode cycle, defined by RR high, read X address is set to 0 when RADE/RX is pulled high with RXINC low.
In the Block Access mode, the RADE/RX signal is ignored.

RXAD: Read X Address
RXAD is a read X address (or line address) input in the FIFO mode. RXAD specifies the line address. 10 bits of read X address data are input serially from RXAD.
The bits of an address are fetched starting from the higher order bits. The most significant bit (A9) is ignored.
In the Block Access mode, the RXAD signal is ignored.

DO0-11 (DQ0-11), DO12-23: Data-Outs
In the FIFO mode, these pins are used as serial outputs.
In the Block Access mode, pins DO0 to DO11 (DQ0 to DQ11) are used as input and output pins.

Write Related

WCLK: Write Clock
WCLK is a write control clock input in the FIFO mode. Synchronized with WCLK's rising edge, serial write access into write ports is executed when $\overline{\text{LWE}}$ or $\overline{\text{UWE}}$ is low.
According to WCLK clocks, the internal counter for the serial address is incremented automatically.
In a write address set cycle, all the write addresses which were input from WXAD are stored into internal address registers synchronously with WCLK. In this address set cycle, WADE/RX must be held high and WR/TR must be held low.
In the write address reset cycle, various write address reset modes can be set synchronously with WCLK. These reset cycles replace complicated serial address control with simple reset cycle control which requires only one WCLK cycle. It greatly facilitates memory access.
In the Block Access mode, the WCLK signal is ignored.

$\overline{\text{LWE}}$: Write Enable
$\overline{\text{LWE}}$ is a write enable clock input in the FIFO mode. $\overline{\text{LWE}}$ enables or disables both internal write address pointers and data-in buffers. When $\overline{\text{LWE}}$ is low, the internal write address pointer is incremented synchronously with WCLK. When $\overline{\text{LWE}}$ is high, even if WCLK is input, the internal write address pointer is not incremented.
In the Block Access mode, writing in the L-bank is performed when $\overline{\text{LWE}}$ goes low at the falling edge of DIN0 ($\overline{\text{RAS}}$).

$\overline{\text{UWE}}$: Write Enable
$\overline{\text{UWE}}$ is a write enable clock input in the FIFO mode. $\overline{\text{UWE}}$ enables or disables both internal write address pointers and data-in buffers. When $\overline{\text{UWE}}$ is low, the internal write address pointer is incremented synchronously with WCLK. When $\overline{\text{UWE}}$ is high, even if WCLK is input, the internal write address pointer is not incremented.
In the Block Access mode, writing in the U-bank is performed when $\overline{\text{UWE}}$ goes low at the falling edge of DIN0 ($\overline{\text{RAS}}$).

DIN0 ($\overline{\text{RAS}}$): Data-In
DIN0 is serial data-in in the FIFO mode.
In the Block Access mode, this pin serves as $\overline{\text{RAS}}$. On the falling edge of this signal, the 10-bit row address (A0 to A9) is fetched.

DIN1 ($\overline{\text{CAS}}$): Data-In
DIN1 is serial data-in in the FIFO mode.
In the Block Access mode, this pin serves as $\overline{\text{CAS}}$. On the falling edge of this signal, the 10-bit column address (A0 to A9) is fetched. This column address becomes a start address in the Block Access mode. When DIN1 ($\overline{\text{CAS}}$) is toggled while DIN0 ($\overline{\text{RAS}}$) remains low, the read/write operation in the Block Access mode is enabled.

DIN2-11 (A0-A9): Data-Ins
DIN2-11 are serial data-ins in the FIFO mode.
In the Block Access mode, these pins serve as a row or column address input (A0 to A9). These pins fetch a row address when DIN0 ($\overline{\text{RAS}}$) is active or a column address when DIN1 ($\overline{\text{CAS}}$) is active.

DIN12-23: Data-Ins
DIN12-23 are serial data-ins in the FIFO mode.

WR/TR: Write Reset/Write Transfer
WR/TR is a write reset control input in the FIFO mode. Write address reset modes are defined when WR/TR level is high according to the "FUNCTION TABLE for write".
When the write operation on a line is terminated, be sure to perform a write transfer operation by WR/TR in order to store the written data in the write register to corresponding memory cells.
In the Block Access mode, the WR/TR signal is ignored.

WXINC: Write X Address Increment
WXINC is a write X address (or line address) increment control input in the FIFO mode. In the write address reset cycle, defined by WR/TR high, the write X address (or line address) is incremented by 1 when WXINC is pulled high with WADE/RX low.
In the Block Access mode, the WXINC signal is ignored.

WADE/RX: Write Address Enable/Write X Address Reset Logic Function
WADE/RX is a dual functional control input in the FIFO mode. WADE, one of the two functions of WADE/RX, is a write address enable input. In the write address set cycle, X address (or line address) input from the WXAD pin is latched into internal write X address register synchronously with WCLK.
RX, the second function of WADE/RX, works as an element to set write X address (or line address) reset mode. In the write address reset cycle, defined by WR/TR high, the write X address is set to 0 when WADE/RX is pulled high with WXINC low.
In the Block Access mode, the WADE/RX signal is ignored.

WXAD: Write X Address
WXAD is a write X address (or line address) input in the FIFO mode. WXAD specifies line address. 10 bits (0 to 9) of write X address data are input serially from WXAD. The bits of an address is fetched starting from the higher order bits. The most significant bit (A9) is ignored.
In the Block Access mode, the WXAD signal is ignored.

IE: Input Enable
IE is an input enable in the FIFO mode which controls the write operation. When IE is high, the input operation is enabled. When IE is low, the write operation is masked. When $\overline{\text{LWE}}$ and $\overline{\text{UWE}}$ signals are low, and IE low, the internal serial write address pointer is incremented on the rising edge of WCLK without actual write operations. This function facilitates picture in picture function in a TV system.
In the Block Access mode, the IE signal is ignored.

WAIT:
This output pin enables interface to the MPU in the Block Access mode.
To cause the MSM5424331 to operate in the Block Access mode, set the D/F pin high and afterward set $\overline{\text{RAS}}$ low. The output of the WAIT pin goes low while a row or column address is set. Perform the actual read or write operation in the Block Access mode after the output of the WAIT pin goes high again.

OPERATION MODE

FIFO Mode
The FIFO mode is set when the D/F pin is set low.

1. Write

1.1 Write operation

Before the write operation begins, X address (or line address) must be input to set the initial bit address for the following serial write access. When $\overline{LWE}$ or $\overline{UWE}$ is low, a set of serial write data on DIN0-11 or DIN12-23 is written into write registers attached to the DRAM memory arrays temporarily on the rising edge of WCLK. The $\overline{LWE}$ pin controls the write operation of DIN0 to DIN11 (12 bits) and the $\overline{UWE}$ pin controls the write operation of DIN12 to DIN23 (12 bits).

Following 24-bit-width serial input data is written into the memory locations in the write register designated by an internal write address pointer which is advanced by WCLK. This enables continuous serial write on a line. When write clock WCLK and read clock RCLK are tied together and are controlled by a common clock or CLK, more than two MSM5424331 can be cascaded directly without any delay devices between the MSM5424331 because the read timing is delayed by one CLK cycle to the write timing. When the write operation on a line is terminated, be sure to perform a write transfer operation by WR/TR in order to store the written data in the write registers to the corresponding memory cells in the DRAM memory arrays.

1.2 Write address pointer increment operation

The write address pointer is incremented synchronously with WCLK when $\overline{LWE}$ or $\overline{UWE}$ is low.

Relationship between the $\overline{LWE}$, $\overline{UWE}$, and IE input levels, Write Address pointer, and data input status

WCLK Rise			Internal Write Address Pointer	Data Input
$\overline{LWE}$	$\overline{UWE}$	IE		
L	L	H	Increments both L- and U-banks.	Inputted
L	H	H	Increments the L-bank only.	
H	L	H	Increments the U-bank only.	
L	L	L	Increments both L- and U-banks.	Not Inputted
L	H	L	Increments the L-bank only.	
H	L	L	Increments the U-bank only.	
H	H	—	Stopped	

When $\overline{LWE}$ or $\overline{UWE}$ is low and IE is high, the write operation is enabled.

If IE level goes low while WCLK is active, the write operation is halted but the write address pointer will continue to advance. That is, IE enables a write mask function. When $\overline{LWE}$ or $\overline{UWE}$ goes high, the write address pointer stops without WCLK.

2. Read

2.1 Read operation

Before the read operation begins, the X address (or line address) must be input for setting initial bit address for the following serial read access.

When $\overline{RE}$ is low, a set of serial 24-bit-width read data on DO0-11, DO12-23 pins is read from read registers attached to DRAM memory arrays on the rising edge of RCLK.

Each access time is specified by the rising edges of RCLK.

2.2 Read address pointer increment operation

The read address pointer is incremented synchronized with RCLK when $\overline{RE}$ level is low.

The output data will be undefined when the read address pointer is incremented above the last address of one line.

3. Initial Address Setting (Write/Read Independent)

Any read operations are prohibited in the read initial address set period. Similarly, any write operations are prohibited in the write initial address set period. Note that read initial address set and write initial address set can occur independently. Similarly, read access can be achieved independently from write initial address set period and write access can be achieved independently from read initial address set cycles.

3.1 Write address setting

WADE/RX enables initial read address inputs. When WADE/RX is high, 10 bits of serial X address (or line address) are input from higher order bits from WXAD.

The operations above enable selection of specific lines randomly and enables the start of serial write access synchronized with write clock WCLK. Address for each line must be input between each line access. In other words, MSM5424331's write is achieved in a "line by line" manner. Any write operations are prohibited in the initial write address set periods.

Serial write input enable time t_{SWE} must be kept for starting a serial write just after the initial write address set period. The most significant bit (A9) is ignored.

3.2 Read address setting

RADE/RX enables initial read address inputs.

When RADE/RX is high, 10 bits of serial X address (or line address) are input from higher order bits from RXAD.

The operations above enable selection of specific lines randomly and enables the start of serial read access synchronized with read clocks, RCLK. Address for each line must be input between each line access. In other words, MSM5424331's read operation is achieved in "line by line" manner.

Any read operations are prohibited in the initial read address set periods. Serial read operations are prohibited while RADE/RX is high. Serial read port enable time t_{SRE} must be kept for starting a serial read just after the initial read address set period. The most significant bit (A9) is ignored.

4. Initial Address Reset Modes (Write/Read Independent)

The initial address reset modes replace complicated read or write initial address settings with simple reset cycles. Initial address reset modes are selected by RR high during read and WR/TR high during write. As in normal read or write address settings, any read operations are prohibited in the read address reset cycles. Similarly, any write operations are prohibited in the initial write address reset cycles. Note that read initial address reset and write initial address reset can occur independently.

Similarly, read access can be achieved independently from write initial address reset cycles and write access can be achieved independently from read initial address reset cycles.

Input addresses are stored into address registers which are connected with address counter which controls address pointer operation. In the serial access operation, the input address into the address registers are kept. Serial write data input enable time t_{SWE} and serial read port read enable time t_{SRE} must be kept for starting serial read or write just after the initial read or write address reset cycles.

Refer to the "FUNCTION TABLE" shown later.

4.1 Line hold operation (read only)

By the "Line hold operation" logic which is composed by a combination of control inputs' level, access is executed starting from the first word on the current line.

4.2 Original address reset operation

By the "Original address reset" logic, the address counter is set to (0,0). After the reset mode, serial access starts from the address (0,0) .

The address counter is reset by this reset mode but the address register, which stored input address in the previous address reset cycle or address set cycle, is not reset. The non-initialized address can be used as a preset address in "address jump reset" mode.

4.3 Line increment operation

By the "Line increment operation" logic, the X address counter is incremented by one from the current X address. That is, serial access from the Y = (0) on the next line is enabled.

4.4 Address jump operation

By the "Address jump operation" logic, a jump may be caused to the initialized line address.

Note: During one reset setting cycle, a plurality of resets cannot be set.

Block Access Mode

The Block Access mode is configured when the D/F pin is set high.

1. Write Operation

The MSM5424331 fetches a 10-bit row address form lines A0 to A9 at the falling edge of the DIN0 ($\overline{RAS}$) pin and a 10-bit column address (10 bits long) from the lines at the falling edge of the DIN1 ($\overline{CAS}$) pin. With this operation, a head address can be set arbitrarily.

For a write operation, the $\overline{LWE}$ or $\overline{UWE}$ pin must be set low at the falling edge of DIN0 ($\overline{RAS}$). The actual fetching of write data is performed at the falling edge of DIN1 ($\overline{CAS}$) after t_{CASB}. The write data is entered from I/O pins DQ0 to DQ11. The write data is written in the L-bank at the falling edge of DIN0 ($\overline{RAS}$) when $\overline{LWE}$ is low and $\overline{UWE}$ is high or in the U-bank when $\overline{LWE}$ is high and $\overline{UWE}$ is low. When both $\overline{LWE}$ and $\overline{UWE}$ are both low, data is written in either the L- or U-bank (which is undefined).

Data storage in the memory cell is executed at the rising edge of DIN0 ($\overline{RAS}$) after the block write operation is completed.

When changing a write operation in the FIFO mode to a write operation in the Block Access mode, it is required to monitor on the WAIT pin whether self refresh in the FIFO mode is completed. Perform the block write operation after the output of the WAIT pin is high.

The block read operation and FIFO operation are disabled during a block write operation.

2. Read Operation

The MSM5424331 fetches a 10-bit row address from lines A0 to A9 at the falling edge of the DIN0 ($\overline{RAS}$) pin and a 10-bit column address from the lines at the falling edge of the DIN1 ($\overline{CAS}$) pin. With this operation, a head address can be set randomly.

For a read operation, the $\overline{LWE}$ or $\overline{UWE}$ pin must be set high at the falling edge of DIN0 ($\overline{RAS}$). Read data is fetches at the falling edge of DIN1 ($\overline{CAS}$) after t_{CASB}. The $\overline{RE}$ pin should be set low at the falling edge of DIN1 ($\overline{CAS}$).

The read data is output from DQ0 to DQ11 I/O pins. The L- or U-bank from which data is read is selected by the status of the "A9" bit of the row address. Data is read from the L-bank when the "A9" bit is "0" or from the U-bank when the "A9" bit is "1". When changing a read operation in the FIFO mode to a read operation in the Block Access mode, it is required to monitor on the WAIT pin whether self refresh in the FIFO mode is completed. Perform the block read operation after the output of the WAIT pin is high.

The block write operation and FIFO operation are disabled during a block read operation.

Refresh

1. FIFO Mode

   In the FIFO mode, the MSM5424331 performs self refresh.

2. Block Access Mode

   In the Block Access mode, self refresh is disabled. Use the $\overline{CAS}$ before $\overline{RAS}$ refresh function to refresh.

   Addressing from A0 to A9 pins is not required because refresh addresses are automatically given by the built-in refresh counter.

Power On

Power must be applied to RCLK, WCLK, and IE input signals to pull them "Low", and to $\overline{RE}$, $\overline{LWE}$, $\overline{UWE}$, DIN0 ($\overline{RAS}$), and DIN1 ($\overline{CAS}$) input signals to pull them "High" before or when the V_{CC} supply is turned on.

After power-up, the device is designed to begin proper operation in at least 200 μs after V_{CC} has reached the specified voltage (2.8 V). After 200 μs, a minimum of one line dummy write operation and read operation is required according to the address setting mode, because the read and write address pointers are not valid after power-up. After that, an operation can be started in the FIFO or Block Access mode.

New Data Read Access in the FIFO Mode

In order to read out "new data", the delay between the beginning of a write address setting cycle and read address setting cycle must be at least two lines.

Old Data Read Access in the FIFO Mode

In order to read out "old data", the delay between the beginning of a write address setting cycle and read address setting cycle must be more than 0 but less than a half line.

FUNCTION TABLE

1. Write (D/F = "L")

Mode	No.	Description of Operation	WR/TR	WXINC	WADE/RX	Internal Address Pointer
Write Transfer	1	Write Transfer	H	L	L	
Address Reset Mode	2	Reset	H	L	H	X address cleared to (0, 0)
	3	Line Increment	H	H	L	X address Increment to (Xn + 1, 0)
	4	Address Jump	H	H	H	X address jump to (Xi, 0)
Address Setting Mode	5	First Address Setting	L	L	H	X address set

Note: For write, Line hold is not provided.

2. Read (D/F = "L")

Mode	No	Description of Operation	RR	RXINC	RADE/RX	Internal Address Pointer
Address Reset Mode	1	Line Hold	H	L	L	X address hold to (Xn, 0)
	2	Reset	H	L	H	X address cleared to (0, 0)
	3	Line Increment	H	H	L	X address increment to (Xn + 1, 0)
	4	Address Jump	H	H	H	X address jump to (Xi, 0)
Address Setting Mode	5	First Address Setting	L	L	H	X address set

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating
Pin Voltage	V_T	Ta = 25°C, with respect to V_{SS}	–0.5 to 4.2 V
Short Circuit Output Current	I_{OS}	Ta = 25°C	50 mA
Power Dissipation	P_D	Ta = 25°C	1 W
Operating Temperature	T_{opr}	—	0 to 70°C
Storage Temperature	T_{stg}	—	–55 to 150°C

Recommended Operating Conditions

(Ta = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	2.8	3.0	3.3	V
Power Supply Voltage	V_{SS}	0	0	0	V
“H” Input Voltage	V_{IH}	2.1	V_{CC}	V_{CC} + 0.3	V
“L” Input Voltage	V_{IL}	–0.5	0	0.8	V

DC Characteristics

(V_{CC} = 2.8 to 3.3 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
“H” Output Voltage	V_{OH}	I_{OH} = –0.1 mA	2.2	—	V
“L” Output Voltage	V_{OL}	I_{OL} = 0.1 mA	—	0.6	V
Input Leakage Current	I_{LI}	$0 < V_I < V_{CC}$ Other input voltage 0 V	–10	10	µA
Output Leakage Current	I_{LO}	$0 < V_O < V_{CC}$	–10	10	µA
Power Supply Current (During Operation)	I_{CC1}	60 ns cycle	—	90	mA
Power Supply Current (During Standby)	I_{CC2}	Input pin = V_{IL}/V_{IH}	—	5	mA

Capacitance

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance	C_I	7	pF
Output Capacitance	C_O	7	pF

AC Characteristics (1/3)
FIFO Mode

Measurement Conditions: (V_{CC} = 2.8 to 3.3 V, Ta = 0 to 70°C)

Parameter	Symbol	Min.	Max.	Unit
WCLK Cycle Time	t_{WCLK}	60	—	ns
WCLK "H" Pulse Width	t_{WWCLH}	28	—	ns
WCLK "L" Pulse Width	t_{WWCLL}	28	—	ns
Serial Write Address Input Active Set-up Time	t_{WAS}	5	—	ns
Serial Write Address Input Active Hold Time	t_{WAH}	7	—	ns
Serial Write Address Input Inactive Hold Time	t_{WADH}	7	—	ns
Serial Write Address Input Inactive Set-up Time	t_{WADS}	7		ns
Write Transfer Instruction Set-up Time	t_{WTRS}	5	—	ns
Write Transfer Instruction Hold Time	t_{WTRH}	7	—	ns
Write Transfer Instruction Inactive Hold Time	t_{WTDH}	7	—	ns
Write Transfer Instruction Inactive Set-up Time	t_{WTDS}	7	—	ns
Serial Write X Address Set-up Time	t_{WXAS}	5	—	ns
Serial Write X Address Hold Time	t_{WXAH}	7	—	ns
Serial Write Data Input Enable Time	t_{SWE}	1500	—	ns
Write Instruction Set-up Time	t_{WES}	5	—	ns
Write Instruction Hold Time	t_{WEH}	7	—	ns
Write Instruction Inactive Hold Time	t_{WEDH}	7	—	ns
Write Instruction Inactive Set-up Time	t_{WEDS}	7	—	ns
Input Data Set-up Time	t_{DS}	5	—	ns
Input Data Hold Time	t_{DH}	12	—	ns
WR/TR-WCLK Active Set-up Time	t_{WRS}	5	—	ns
WR/TR-WCLK Active Hold Time	t_{WRH}	7	—	ns
WR/TR-WCLK Inactive Hold Time	t_{WRDH}	7	—	ns
WR/TR-WCLK Inactive Set-up Time	t_{WRDS}	7	—	ns
WXINC-WCLK Active Set-up Time	t_{WINS}	5	—	ns
WXINC-WCLK Active Hold Time	t_{WINH}	7	—	ns
WXINC-WCLK Inactive Hold Time	t_{WINDH}	7	—	ns
WXINC-WCLK Inactive Set-up Time	t_{WINDS}	7	—	ns
WADE/RX-WCLK Active Set-up Time	t_{WRXS}	5	—	ns
WADE/RX-WCLK Active Hold Time	t_{WRXH}	7	—	ns
WADE/RX-WCLK Inactive Hold Time	t_{WRXDH}	7	—	ns
WADE/RX-WCLK Inactive Set-up Time	t_{WRXDS}	7	—	ns
IE Enable Set-up Time	t_{IES}	5	—	ns
IE Enable Hold Time	t_{IEH}	7	—	ns
IE Disable Set-up Time	t_{IEDS}	7	—	ns
IE Disable Hold Time	t_{IEDH}	7	—	ns

AC Characteristics (2/3)
FIFO Mode

Measurement Conditions: (V_{CC} = 2.8 to 3.3 V, Ta = 0 to 70°C)

Parameter	Symbol	Min.	Max.	Unit
RCLK Cycle Time	t_{RCLK}	60	—	ns
RCLK "H" Pulse Width	t_{WRCLH}	28	—	ns
RCLK "L" Pulse Width	t_{WRCLL}	28	—	ns
Serial Read Address Input Active Set-up Time	t_{RAS}	5	—	ns
Serial Read Address Input Active Hold Time	t_{RAH}	7	—	ns
Serial Read Address Input Inactive Hold Time	t_{RADH}	7	—	ns
Serial Read Address Input Inactive Set-up Time	t_{RADS}	7	—	ns
Serial Read X Address Set-up Time	t_{RXAS}	5	—	ns
Serial Read X Address Hold Time	t_{RXAH}	7	—	ns
$\overline{RE}$ Enable Set-up Time	t_{RES}	5	—	ns
$\overline{RE}$ Enable Hold Time	t_{REH}	t_{AC}	—	ns
$\overline{RE}$ Disable Hold Time	t_{REDH}	7	—	ns
$\overline{RE}$ Disable Set-up Time	t_{REDS}	7	—	ns
Read Port Read Enable Time	t_{SRE}	1500	—	ns
Read Port Read Data Hold Time	t_{OH}	12	—	ns
Access Time from RCLK	t_{AC}	—	50	ns
Read Data Hold Time from $\overline{RE}$	t_{DDRE}	12	—	ns
RR-RCLK Active Set-up Time	t_{RRS}	5	—	ns
RR-RCLK Active Hold Time	t_{RRH}	7	—	ns
RR-RCLK Inactive Hold Time	t_{RRDH}	7	—	ns
RR-RCLK Inactive Set-up Time	t_{RRDS}	7	—	ns
RXINC-RCLK Active Set-up Time	t_{RINS}	5	—	ns
RXINC-RCLK Active Hold Time	t_{RINH}	7	—	ns
RXINC-RCLK Inactive Hold Time	t_{RINDH}	7	—	ns
RXINC-RCLK Inactive Set-up Time	t_{RINDS}	7	—	ns
RADE/RX-RCLK Active Set-up Time	t_{RRXS}	5	—	ns
RADE/RX-RCLK Active Hold Time	t_{RRXH}	7	—	ns
RADE/RX-RCLK Inactive Set-up Time	t_{RRXDS}	7	—	ns
RADE/RX-RCLK Inactive Hold Time	t_{RRXDH}	7	—	ns
BLOCK-FRAM Mode Change Set-up Time	t_{DFS}	20	—	ns
BLOCK-FRAM Mode Change Hold Time	t_{DFH}	5	—	ns
Transition Time (Rise and Fall)	t_T	2	30	ns

AC Characteristics (3/3)
Block Mode

Measurement Conditions: (V_{CC} = 2.8 to 3.3 V, Ta = 0 to 70°C)

Parameter	Symbol	Min.	Max.	Unit
D/F to $\overline{RAS}$ Precharge Time	t_{DRP}	60	—	ns
D/F to $\overline{CAS}$ Precharge Time	t_{DCP}	60	—	ns
BLOCK Mode Set-up Time	t_{BS}	40000	—	ns
Row Address Set-up Time	t_{ASR}	0	—	ns
Row Address Hold Time	t_{AHR}	10	—	ns
Column Address Set-up Time	t_{ASC}	0	—	ns
Column Address Hold Time	t_{AHC}	15	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	35	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	ns
$\overline{CAS}$ Pulse Width	t_{CAS}	28	—	ns
$\overline{CAS}$ Precharge Time	t_{CP}	28	—	ns
BLOCK Mode Start to $\overline{CAS}$ Pulse Width	t_{CASB}	600	—	ns
BLOCK Mode Cycle Time	t_{BC}	60	—	ns
$\overline{RAS}$ Precharge Time (WRITE)	t_{RPW}	400	—	ns
$\overline{RAS}$ Precharge Time (READ)	t_{RPR}	60	—	ns
Access Time from $\overline{RAS}$	t_{RAC}	—	600	ns
Access Time from $\overline{CAS}$	t_{BAC}	—	50	ns
Data-in Set-up Time	t_{BDS}	0	—	ns
Data-in Hold Time	t_{BDH}	15	—	ns
Data-in Hold Time (Head Bit)	t_{FBDH}	585	—	ns
BLOCK Mode Write Hold Time	t_{BWH}	15	—	ns
BLOCK Mode Read Hold Time	t_{BRH}	15	—	ns
Write Command Set-up Time	t_{WCS}	0	—	ns
Write Command Hold Time	t_{WCH}	15	—	ns
Read Command Set-up Time	t_{RCS}	0	—	ns
Read Command Hold Time	t_{RCH}	15	—	ns
$\overline{RAS}$ Hold Time	t_{RSH}	50	—	ns
Output Data Hold Time from $\overline{RE}$	t_{DDRE}	12	—	ns
Output Data Enable Time from $\overline{RE}$	t_{DERE}	—	40	ns
Output Buffer Turn-off Delay Time	t_{OFF}	12	—	ns
Read Data Hold Time from $\overline{CAS}$	t_{BOH}	15	—	ns
Write Command Set-up Time from $\overline{CAS}$	t_{CWCS}	0	—	ns
Write Command Hold Time from $\overline{CAS}$	t_{CWCH}	15	—	ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{RPC}	10	—	ns
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$)	t_{RASB}	400	—	ns
$\overline{CAS}$ before $\overline{RAS}$ Cycle Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{RC}	465	—	ns
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{RP}	61	—	ns
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	—	ns
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	15	—	ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CPN}	28	—	ns
Transition Time (Rise and Fall)	t_T	2	30	ns

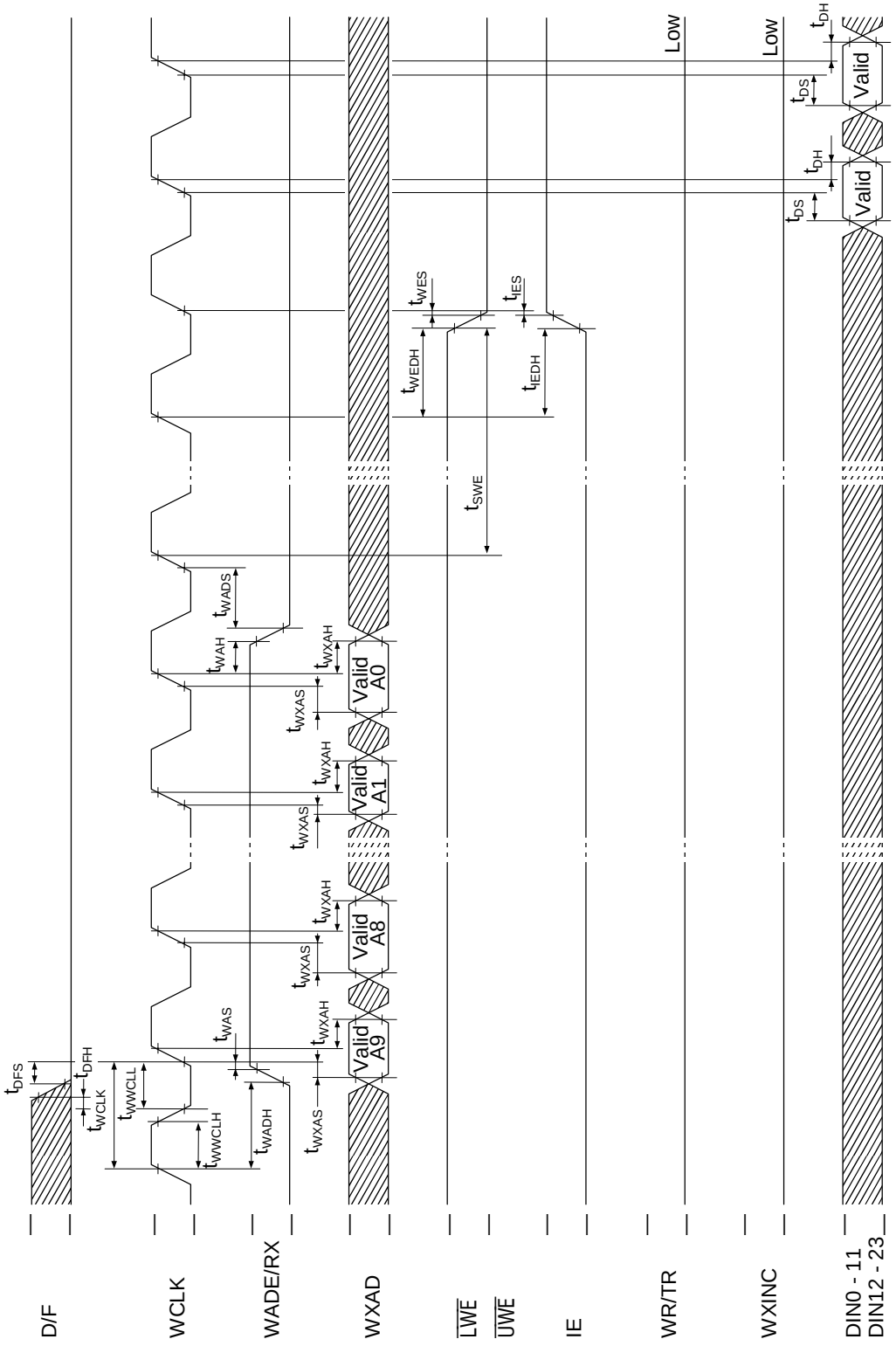
Note: Measurement conditions

Input pulse level	: V_{IH} = 2.1 V, V_{IL} = 0.8 V
Input timing reference level	: V_{IH} = 2.1 V, V_{IL} = 0.8 V
Output timing reference level	: V_{OH} = 2.2 V, V_{OL} = 0.6 V
Input rise/fall time	: 2 ns
Load condition	: CL = 30 pF

TIMING WAVEFORM

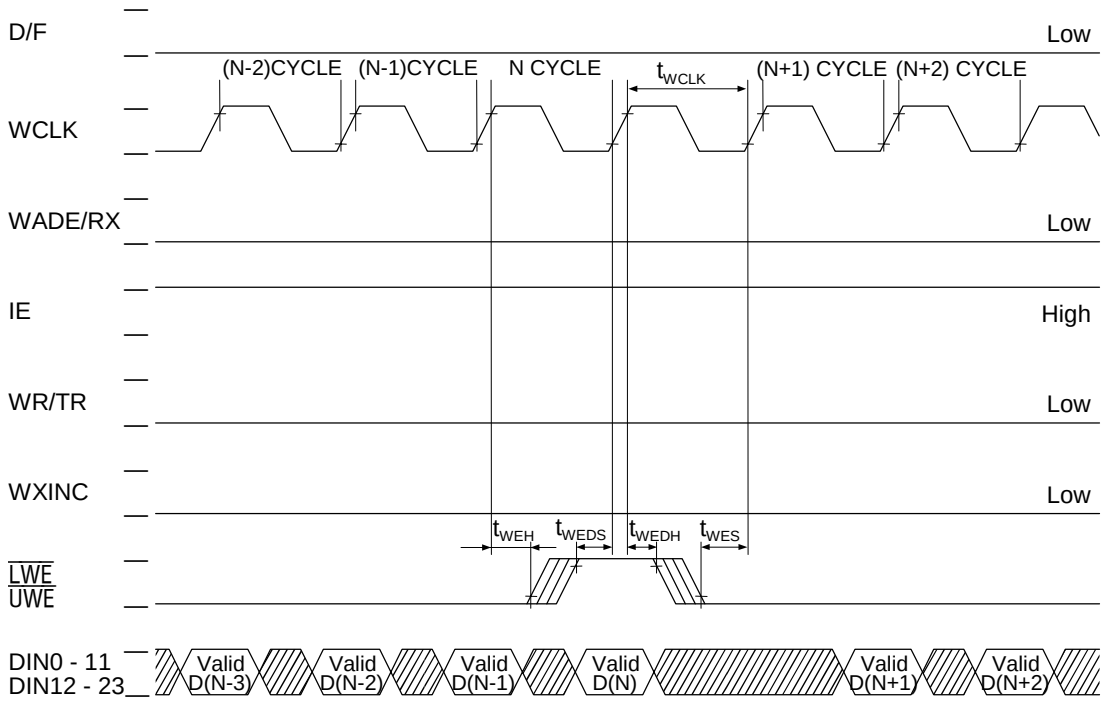
(FIFO Mode)

Write Cycle (Address Setting Cycle)

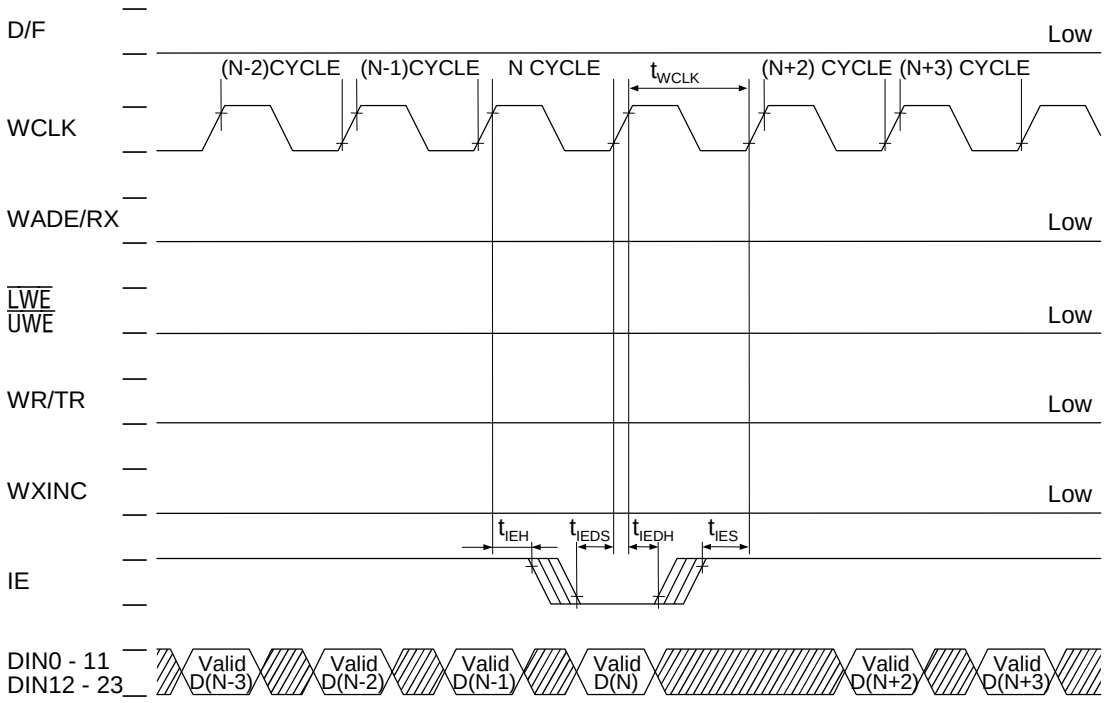


(FIFO Mode)

Write Cycle ($\overline{LWE}$/$\overline{UWE}$ Control)

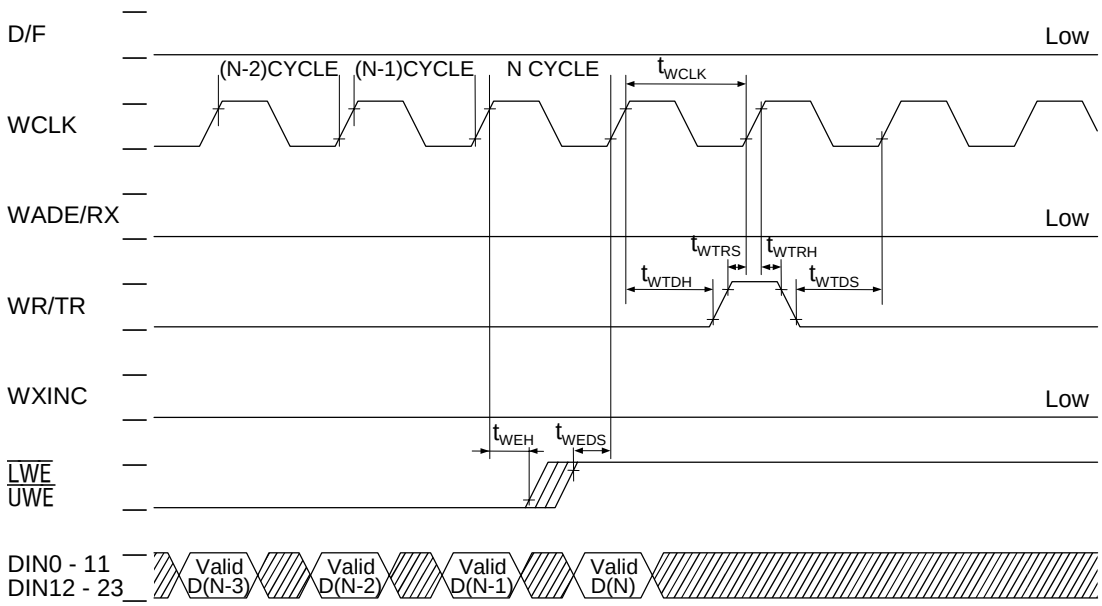


Write Cycle (IE Control)



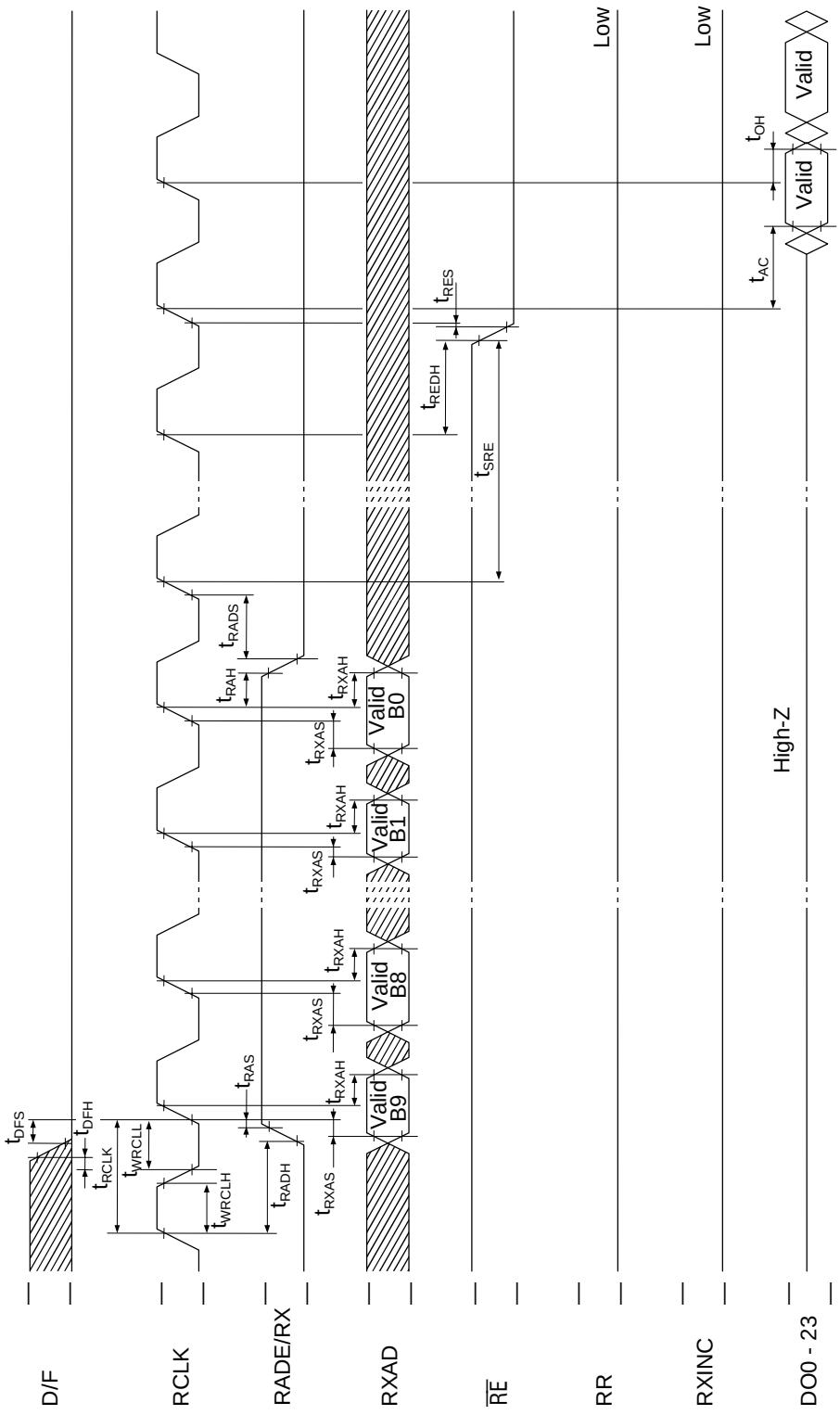
Note: In the IE = “L” cycle, the write address pointer is incremented, though no DIN data is written and the memory data is held.

(FIFO Mode)
Write Cycle (Write Transfer)

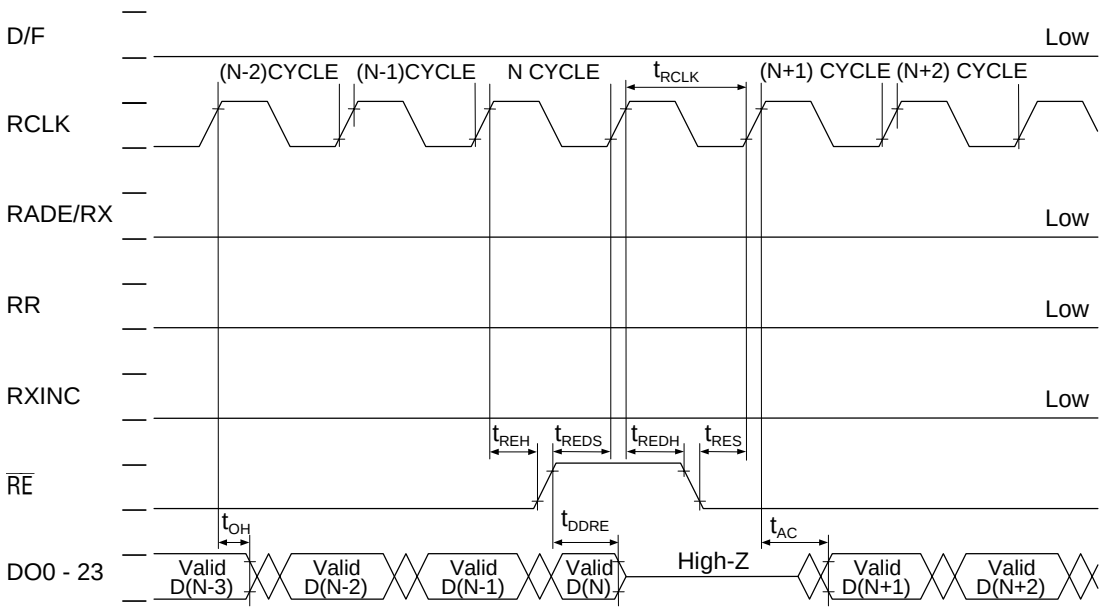


Note: When finishing the write operation on a line, be sure to perform a write transfer operation because the write data on the line is stored in the memory cell.

(FIFO Mode)
Read Cycle (Address Setting Cycle)

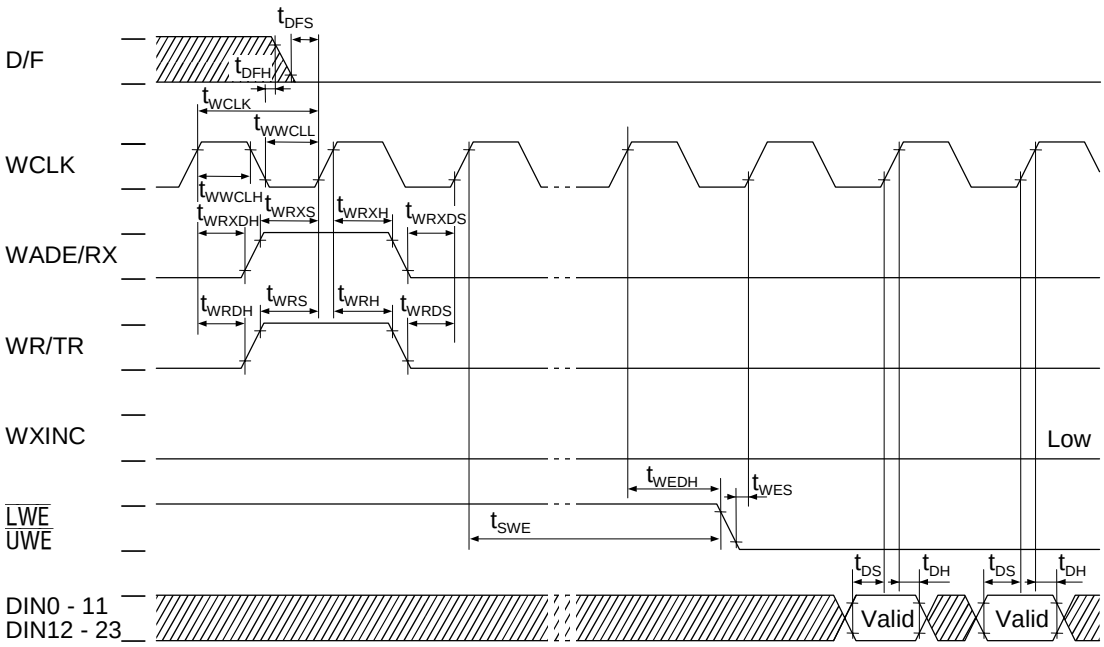


(FIFO Mode)
Read Cycle ($\overline{RE}$ Control)



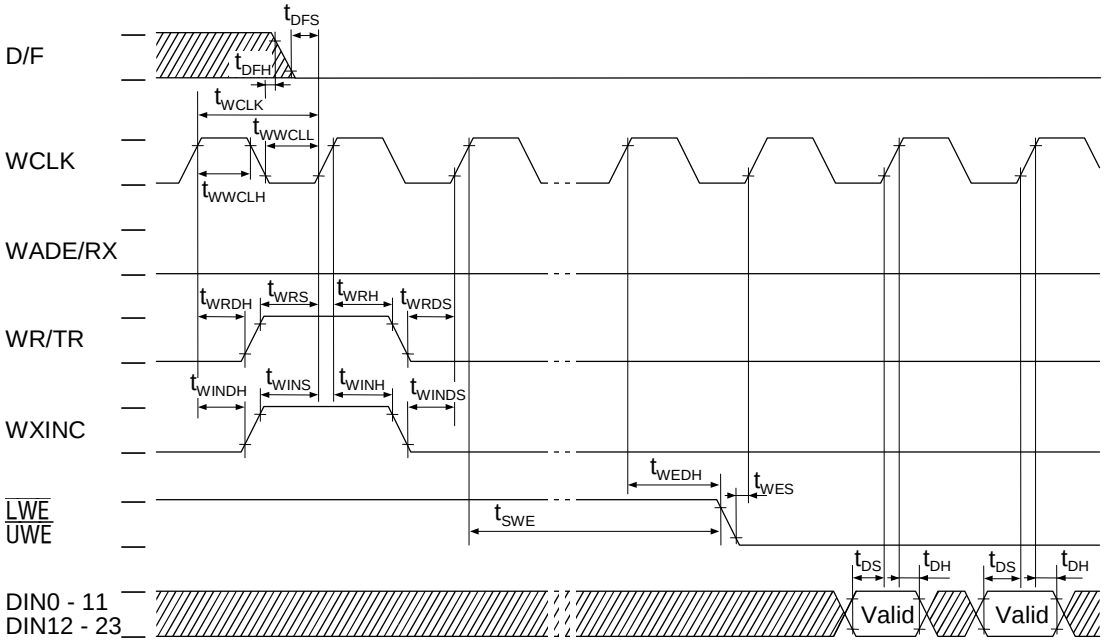
Note: In the cycle of $\overline{RE}$ = "H", the read address pointer is not incremented and the output enters the high impedance state.

(FIFO Mode)
Write Reset Mode



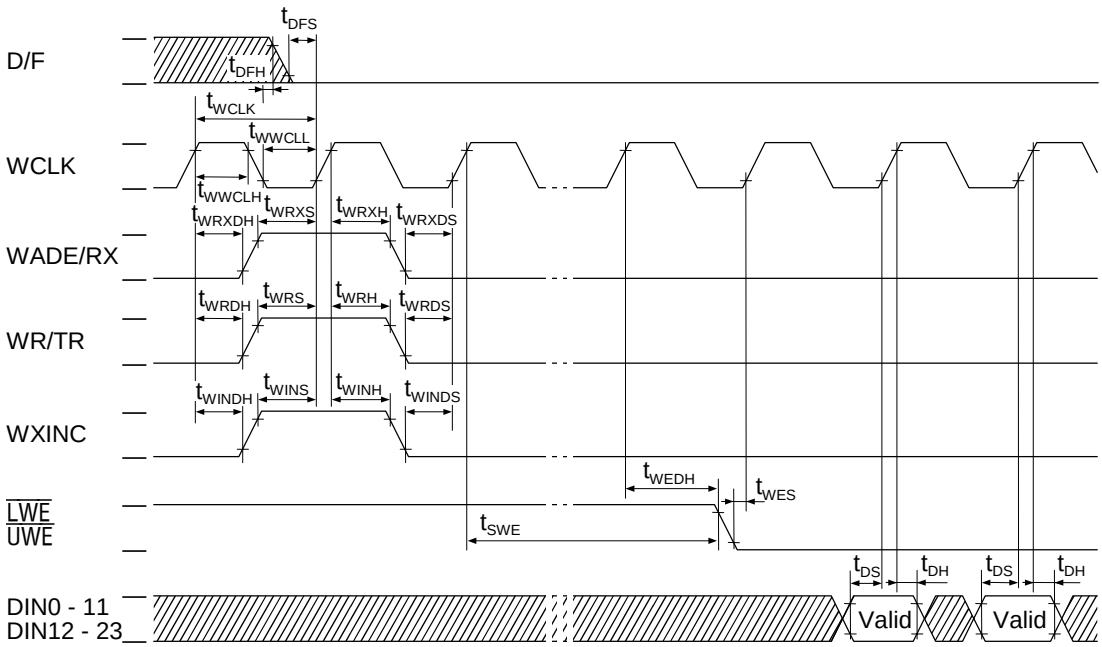
Note: Both the line address and word address are set to 0.

Write Line Increment Mode



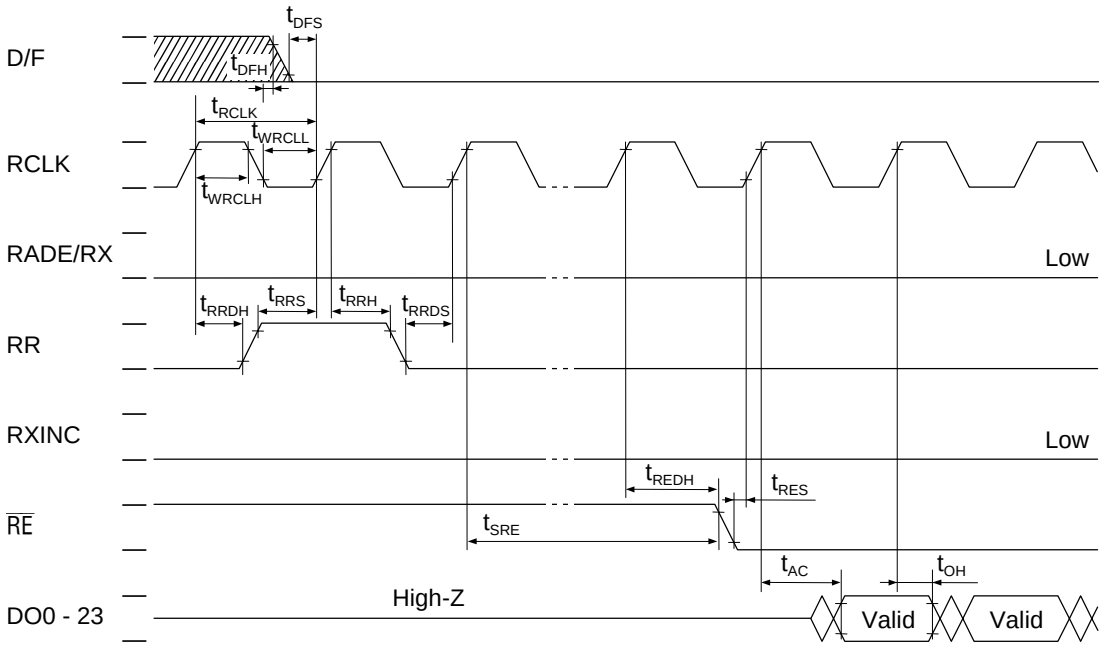
Note: The line address is incremented by 1 and the word address is set to 0.

(FIFO Mode)
Write Address Jump Mode



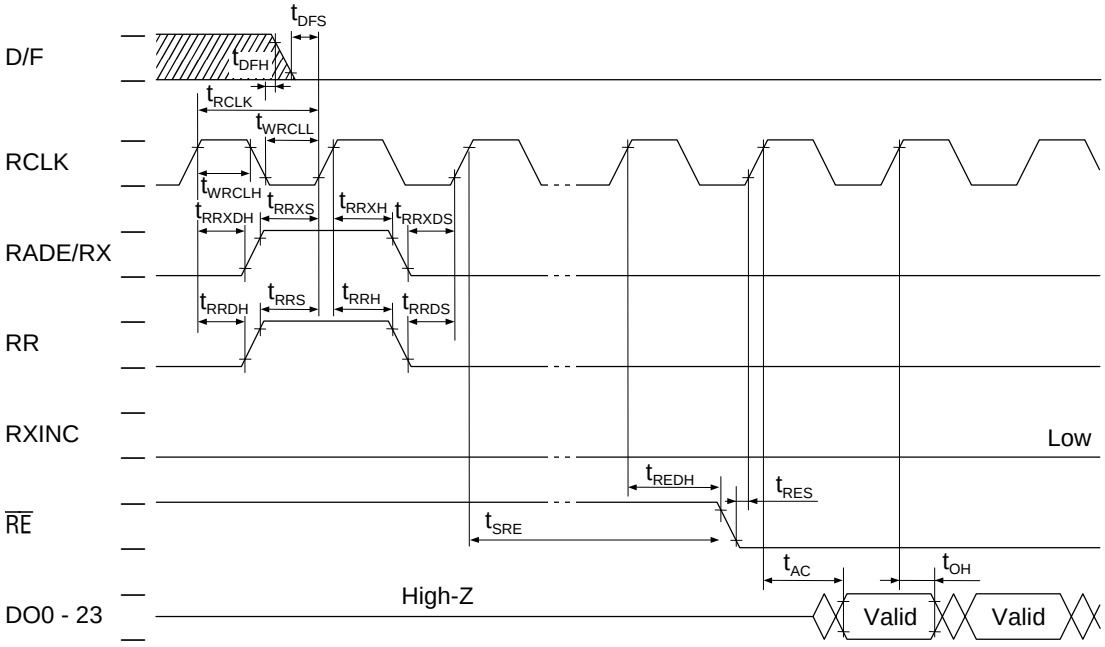
Note: The line address is reset to the initialized addresses and the word address is set to 0.

(FIFO Mode)
Read Line Hold Mode



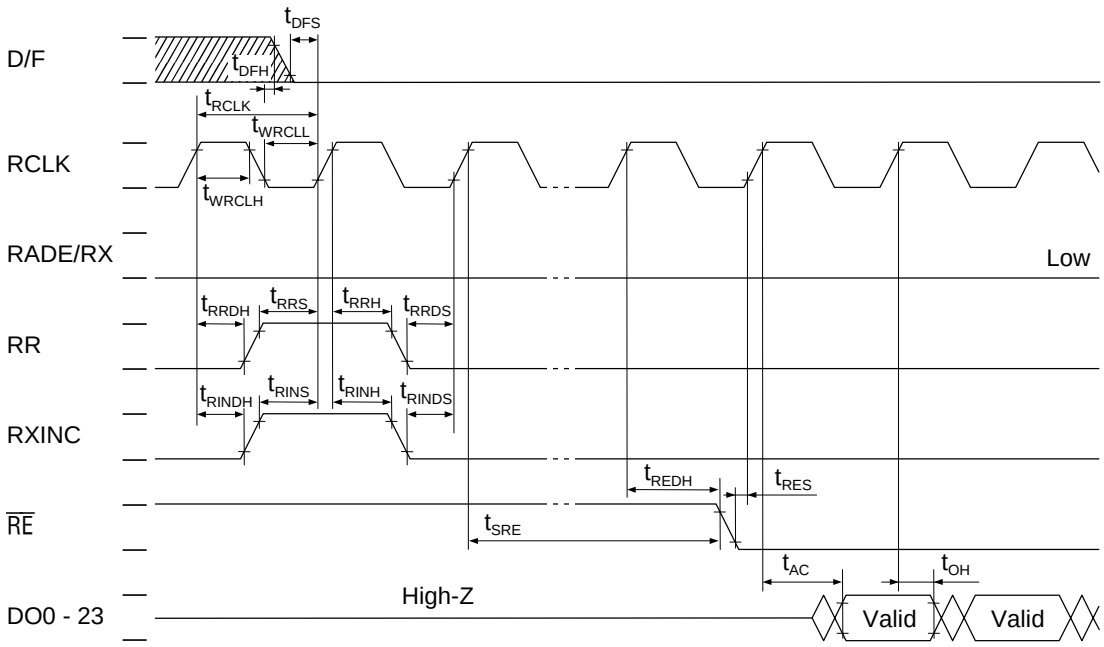
Note: The line address is held and the word address is set to 0.

Read Reset Mode



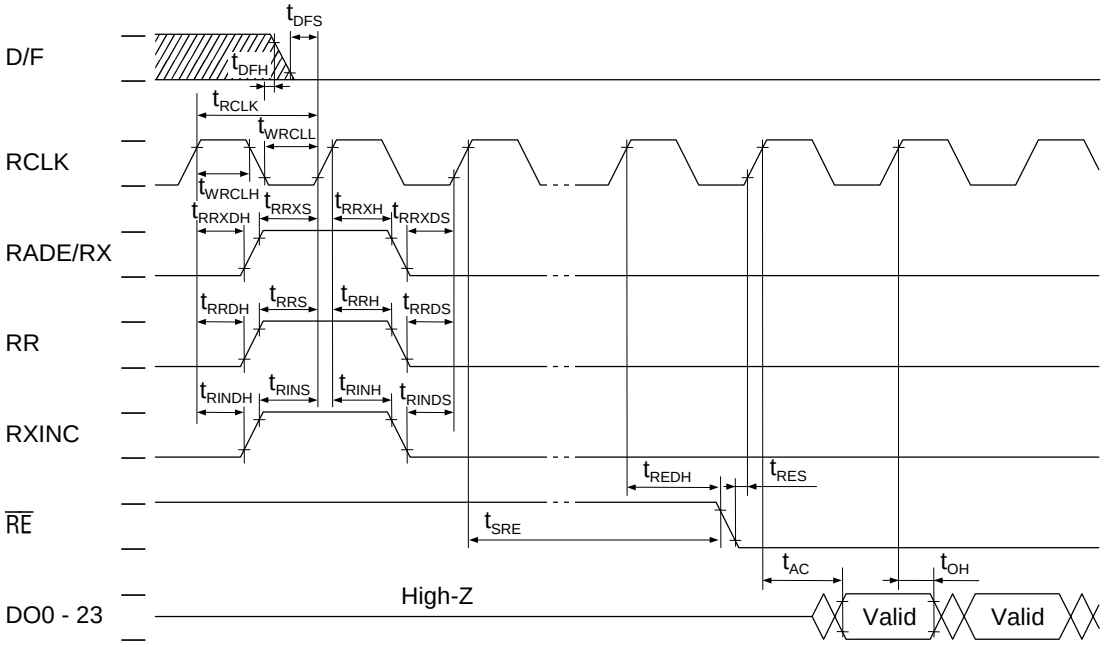
Note: Both the line address and word address are set to 0.

(FIFO Mode)
Read Line Increment Mode



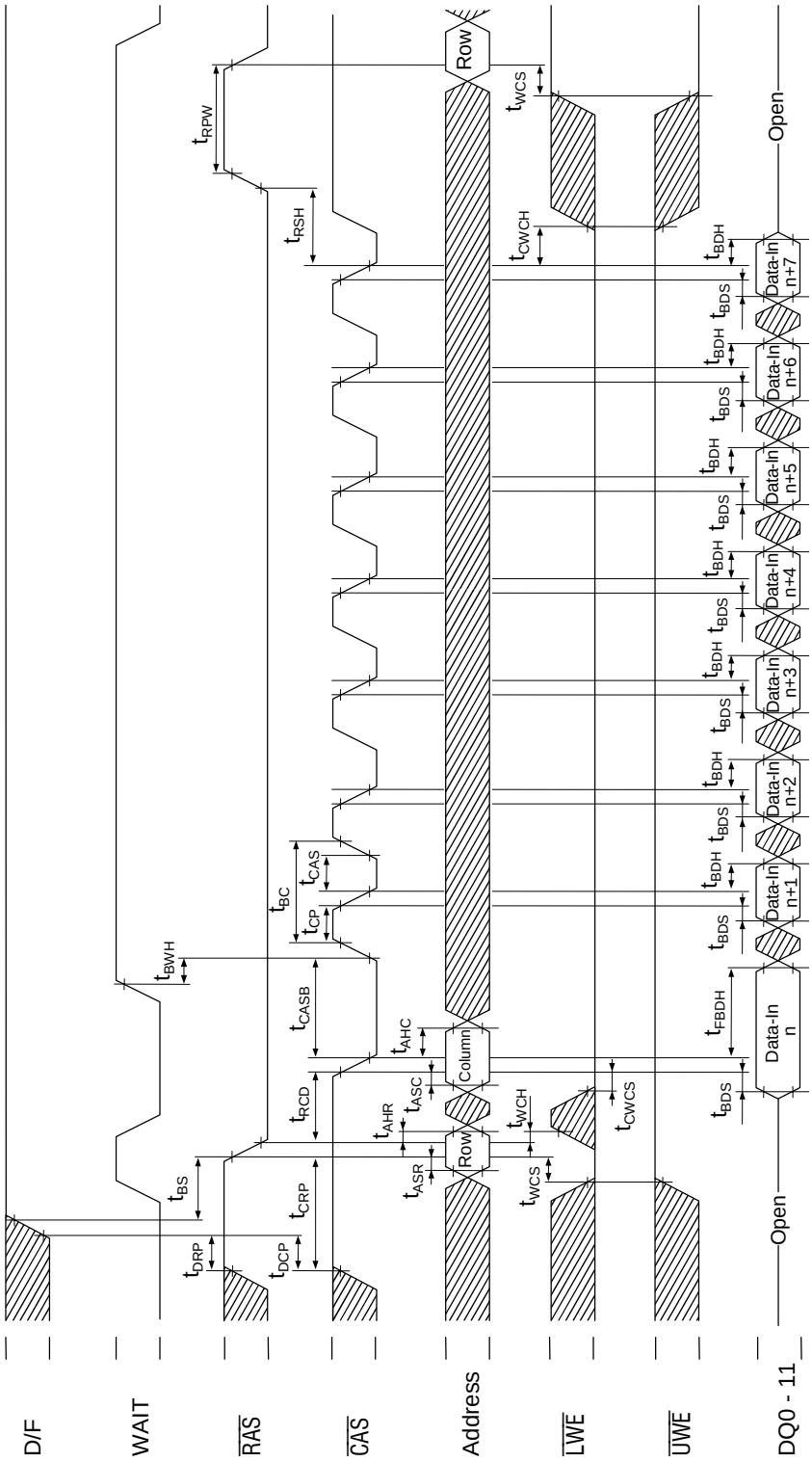
Note: The line address is incremented by 1 and the word address is set to 0.

Read Address Jump Mode



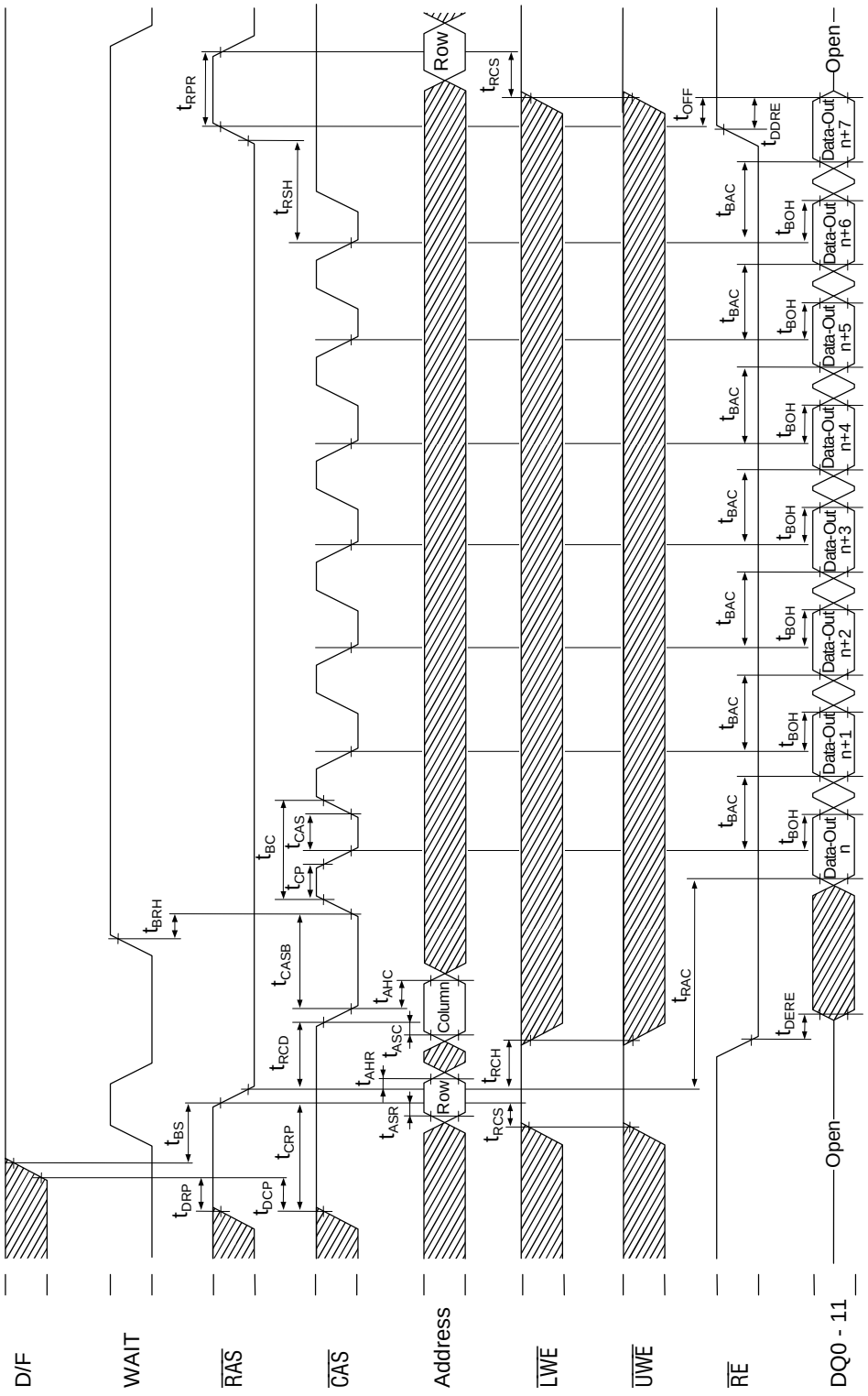
Note: The line address is reset to the initialized addresses and the word address is set to 0.

(Block Access Mode)
Write Cycle



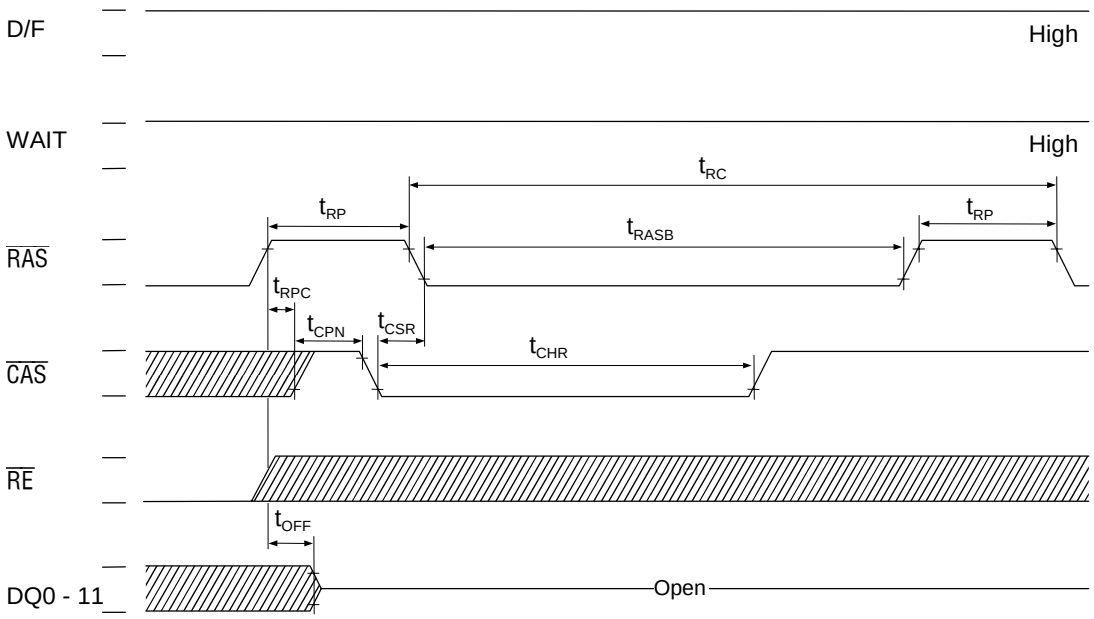
Note: Data is written to L-BANK if $\overline{LWE}$ = "L" during a falling edge of $\overline{RAS}$ or is written to U-BANK if $\overline{UWE}$ = "L". A data write to L-BANK or to U-BANK is undefined if $\overline{LWE}$ and $\overline{UWE}$ = "L".

(Block Access Mode)
Read Cycle



Note: Read data is read from L-BANK if A9 of the Row address is “0” and is read from U-BANK if A9 of the Row address is “1”.

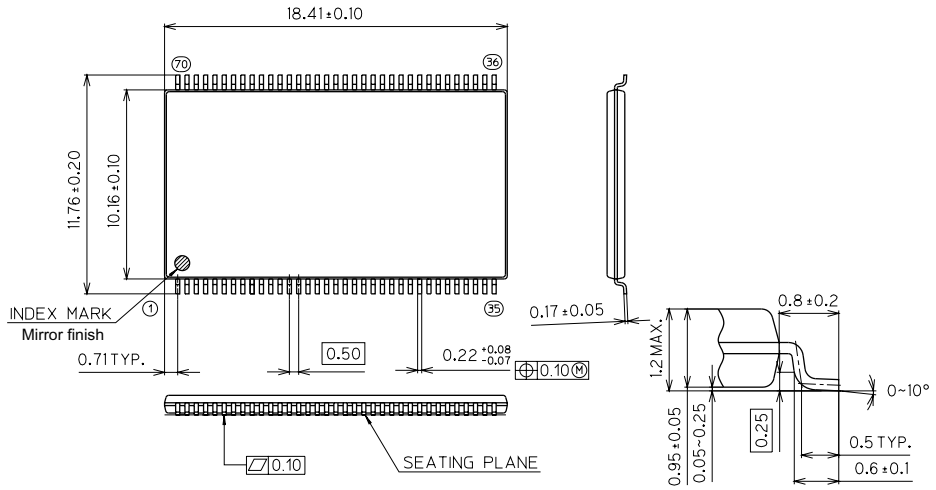
(Block Access Mode)
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



PACKAGE DIMENSIONS

(Unit: mm)

TSOP(2)70-P-400-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.49 TYP.
Rev. No./Last Revised	2/Nov. 13, 1998

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

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