REAL-TIME CLOCK **S-3530A**

S-3530A is a CMOS real-time clock IC supporting an I²C-BUS, which is designed to transfer or set each data of a clock and calender as requested by a CPU. It provides connection with a CPU via two wires and has two systems of an interrupt/alarm features, allowing the alleviation of software treatment on the side of a host.
It also works on lower power with the oscillating circuit operated at a constant voltage. The shipping form is either a die or an 8-pin SSOP ultra compact package.

■ Features

- Low power consumption : 0.7 μA typ. (V_{DD}=3.0 V)
- Wide area of operating voltage : 1.7 to 5.5 V
- BCD input/output of year, month, day, day of a week, hour, minute and second
- CPU interface via two wires (I²C- BUS)
- Auto calender till the year of 2,099 (automatic leap year arithmetic feature included)
- Built-in power voltage detecting circuit
- Built-in constant voltage circuit
- Built-in flag generating circuit on power on/off
- Built-in alarm interrupter (two systems)
- Steady-state interrupt frequency/duty setting feature
- Built-in 32 kHz crystal oscillating circuit (Internal Cd, External Cg)
- Die or 8-pin SSOP package (pin pitch: 0.65 mm)

(*) I²C-BUS is a trademark of PHILLIPS ELECTRONICS N.V.

■ Applications

- Cellular phone
- PHS
- A variety of pagers
- TV set and VCR
- Games

■ Block Diagram

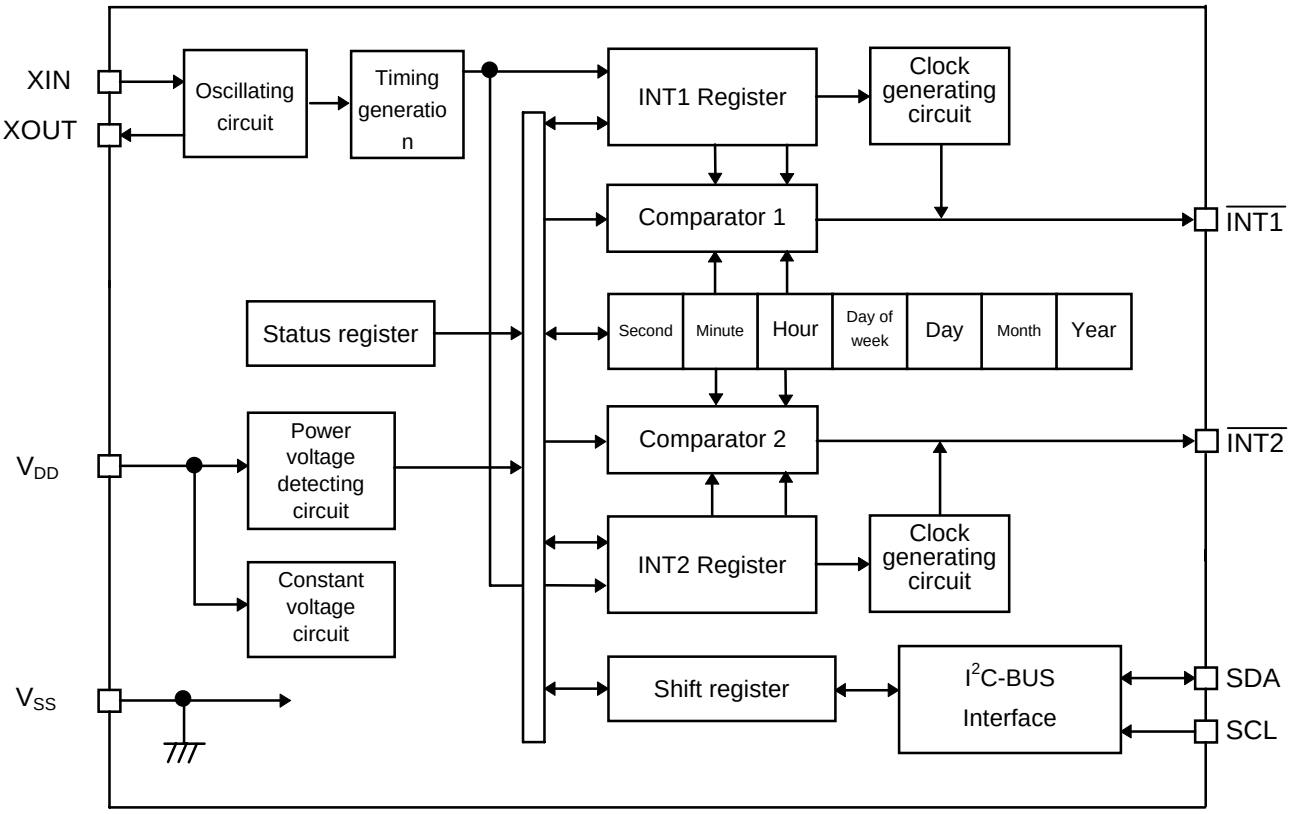


Figure 1 Block diagram

■ Pin Assignment

(1) Package : S-3530AEFS

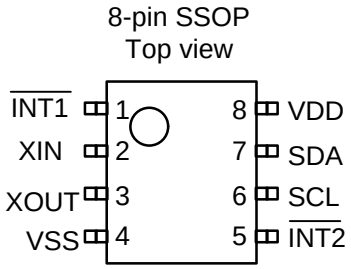
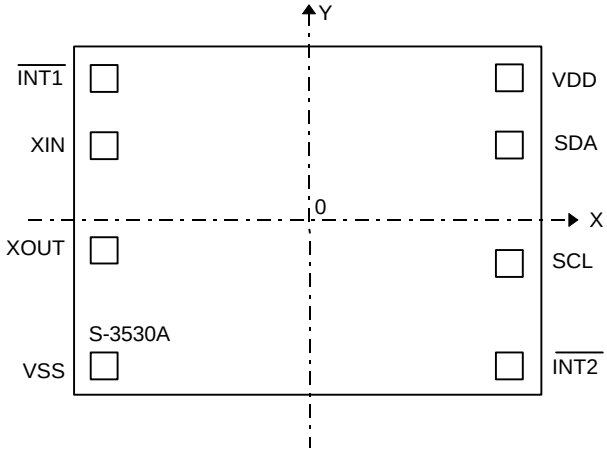


Figure 2 Pin assignment

(2) Die : S-3530AECA



(*1) Die size : 2.10 × 1.60 mm
Sizes shown are for design purposes only.
The corners of the die shrink by approximately 30 μm after dicing.

(*2) Pad size : 100 × 100 μm

Pad Coordinates

Symbol	X-Coordinate	Y-Coordinate	Symbol	X-Coordinate	Y-Coordinate
$\overline{\text{INT1}}$	–890	641	VDD	890	641
XIN	–890	351	SDA	890	356
XOUT	–890	–114	SCL	890	–240
VSS	–890	–641	$\overline{\text{INT2}}$	890	–641

Figure 2-2 Pad assignment

■ Description of Pins

Table 1 Description of pins

Pin No.	Symbol	Description	Configuration
1	$\overline{\text{INT1}}$	Alarm interrupt 1 output pin. Depending on the mode set by the INT1 register and status register, it outputs low or Clock when time is reached. It is disabled by rewriting the status register.	N-channel open drain output (No protective diode on the side of VDD)
2	XIN	Crystal oscillator connect pin (32,768 Hz) (Internal Cd, External Cg)	—
3	XOUT		
4	VSS	Negative power supply pin (GND)	—
5	$\overline{\text{INT2}}$	Alarm interrupt 2 output pin. Depending on the mode set by the INT2 register and status register, it outputs low or Clock when time is reached. It is disabled by rewriting the status register.	N-channel open drain output (No protective diode on the side of VDD)
6	SCL	Serial clock input pin. Follow the specification with great care to the rising/falling time of the SCL signal because the signal is treated at its rising/falling edge.	CMOS input (No protective diode on the side of VDD)
7	SDA	Serial data input/output pin. This pin is usually pulled up to VDD via a resistor, and connected to other open-drain or open-collector output devices in wired OR configuration.	N-channel open drain output (No protective diode on the side of VDD) CMOS input
8	VDD	Positive power supply pin.	—

■ Description of Operation

1. Serial interface

S-3530A receives various commands through the I^2C-BUS-based serial interface to read/write data. The method of I^2C-BUS-based transfer is described here.

1-1. Start condition

Changing the SDA line from “H” to “L” when the SCL line is “H” activates the start condition.
All the operations begin at the start condition.

1-2. Stop condition

Changing the SDA line from “L” to “H” when the SCL line is “H” activates the stop condition.
During a read sequence, any read operation is stopped and a device enters its stand-by mode when a stop condition is received.

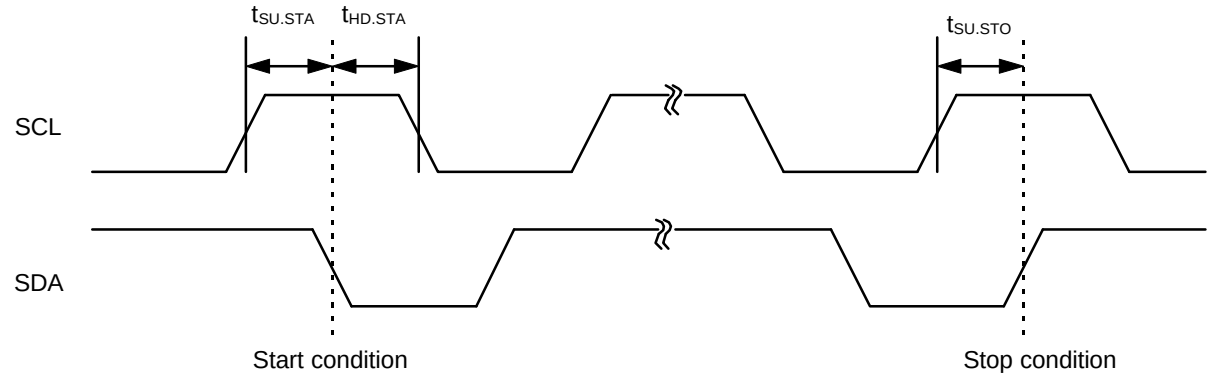


Figure 3 Start/Stop condition

1-3. Data transfer

When the SDA line is changed while the SCL line is on “L”, data transfer is performed.
When the SDA line is changed while the SCL line is on “H”, a start or stop condition is recognized.

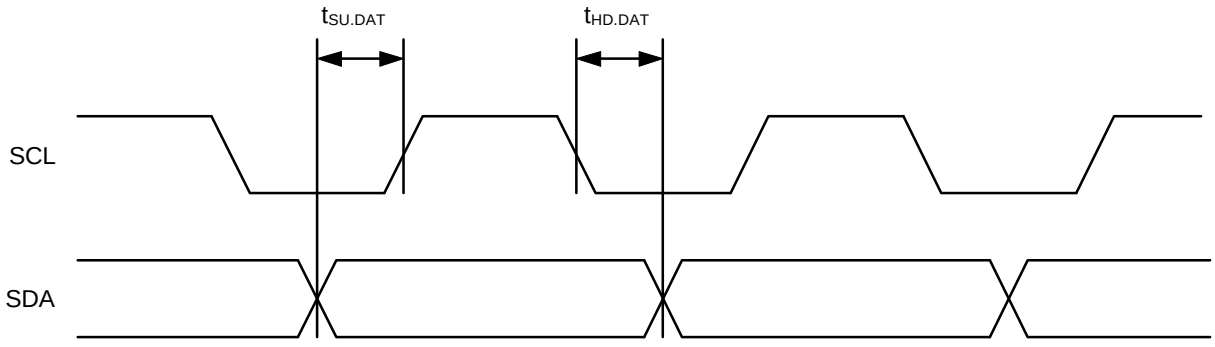


Figure 4 Data transfer timing

1-4. Acknowledge

Data transfer is performed in eight-bit sequence. A device on the system bus, which succeedingly receives data during a period of a ninth clock cycle, puts the SDA line on “L” and returns an acknowledge signal meaning that the data has been received.

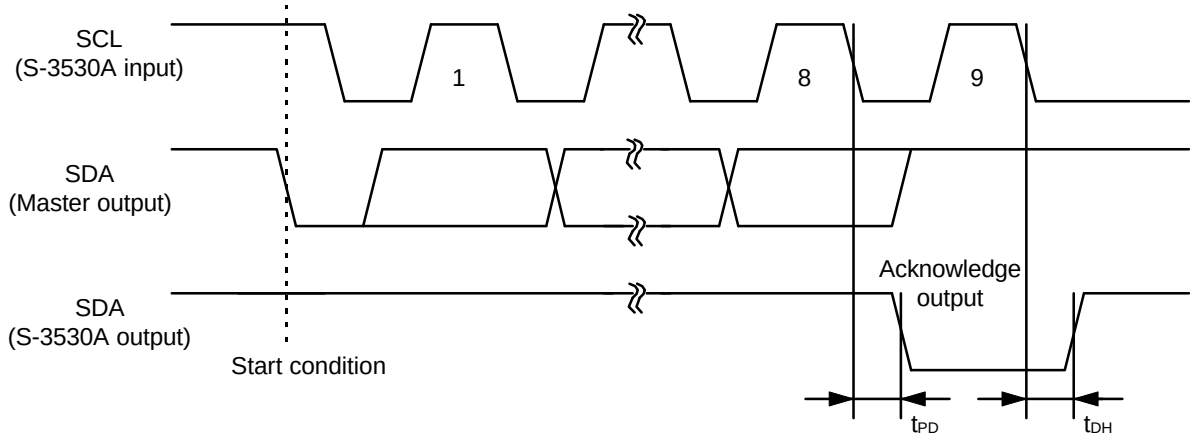


Figure 5 Acknowledge output timing

1-5. Device addressing

The master device on the system generates a start condition to its slave device to make communication. It continuously issues the device address of a four-bit length, the command of a three-bit length and the read/write command of a one-bit length over the SDA bus.

The upper four bits, called a device code, represent a device address and are fixed at “0110.”

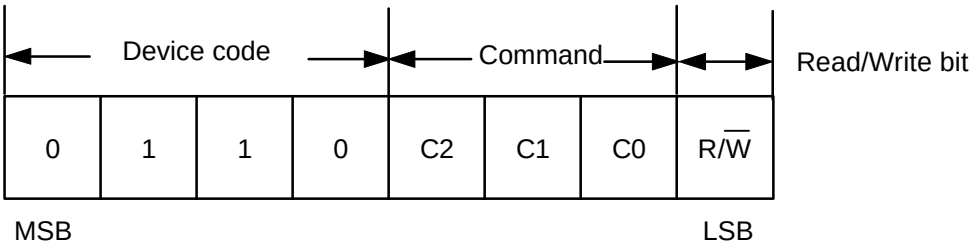
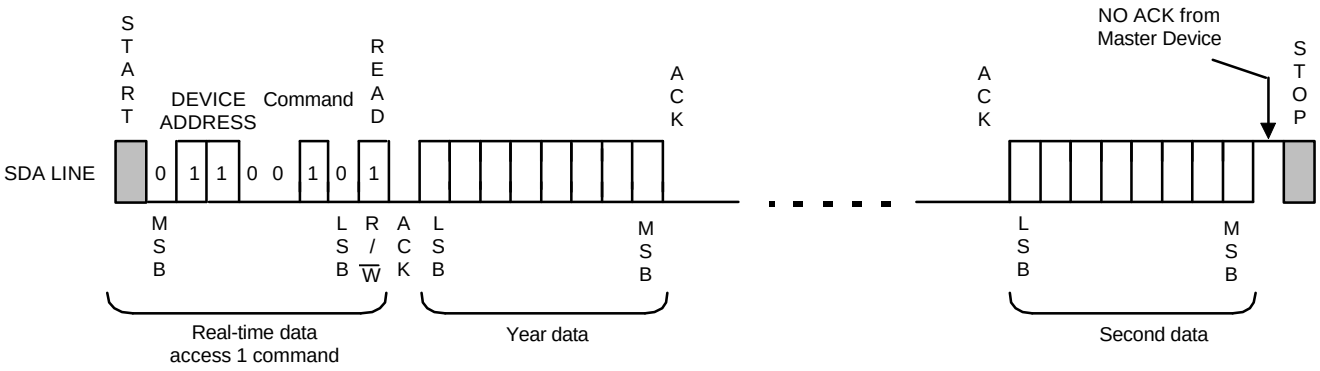


Figure 6 Communication data

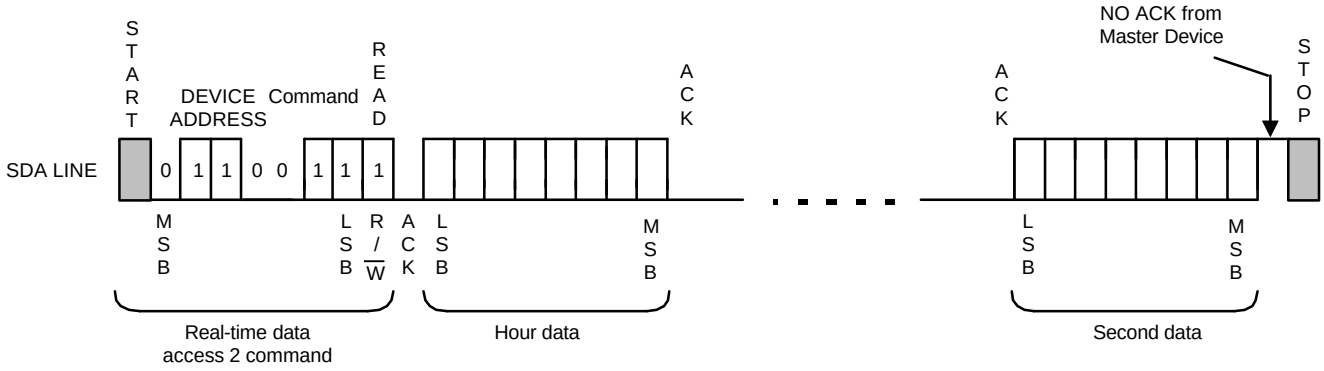
1-6. Data reading

After a start condition is detected from the outside, the device code and command are received. At this point, the real-time reading mode or status register reading mode is entered when the read/write bit is "1". In either the real-time reading mode or status register reading mode, data are output in the order from LSB.

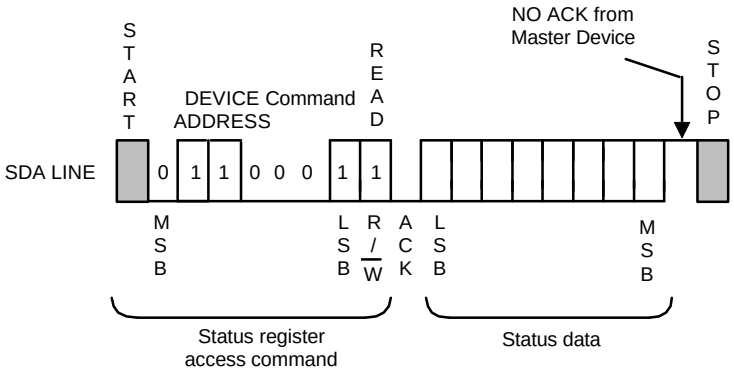
(1) Real-time data reading 1



(2) Real-time data reading 2



(3) Status register reading



ⓇNOTE

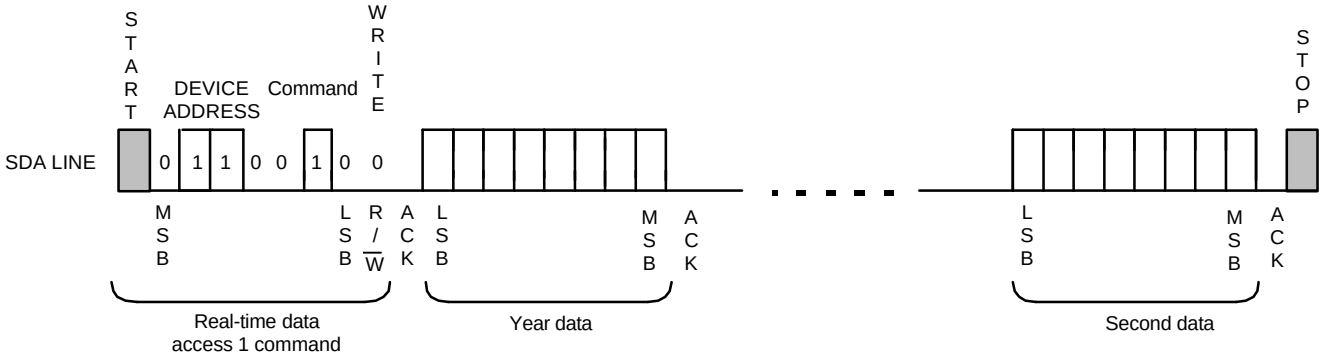
ACK Upside: Generate from the master device
ACK Downside: Generate from the S-3530A

Figure 7 Read communication

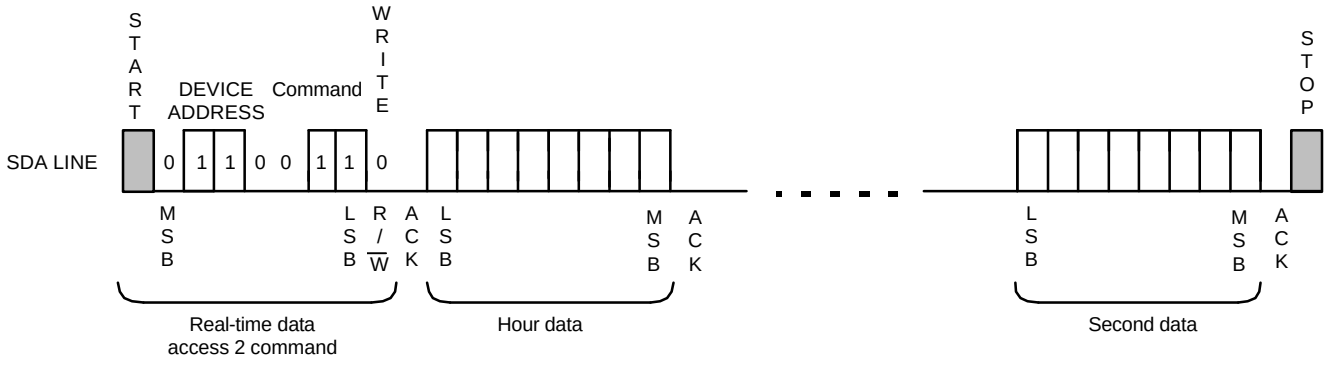
1-7. Data writing

After a start condition is detected from the outside, the device code and command are received. At this point, the real-time data writing mode or other register writing mode is entered when the read/write bit is "0". Data must be entered in the order from LSB of the real-time data writing mode or status register writing mode.
In real-time data writing, the counter of a calender and time is reset when the ACK signal rises following the real-time writing command, and any update operation is disabled. After a minute data is received, the end of a month is corrected while a second data is imported. Then, the count-up is started when the ACK signal rises after the second data is received.

(1) Real-time data writing 1



(2) Real-time data writing 2



(3) Status register writing

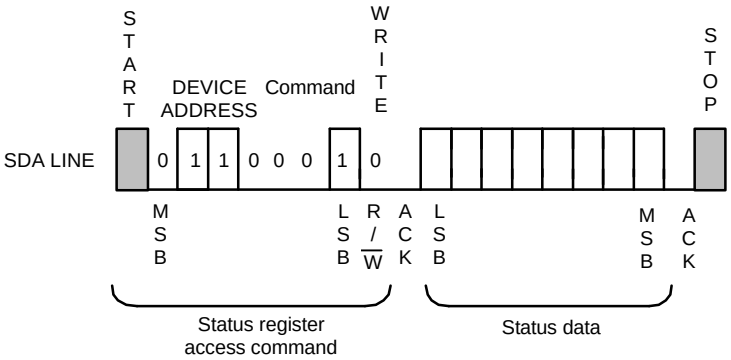


Figure 8 Write communication

2. Command configuration

There are eight commands by which the read/write operation of various registers is performed. The table below lists them.

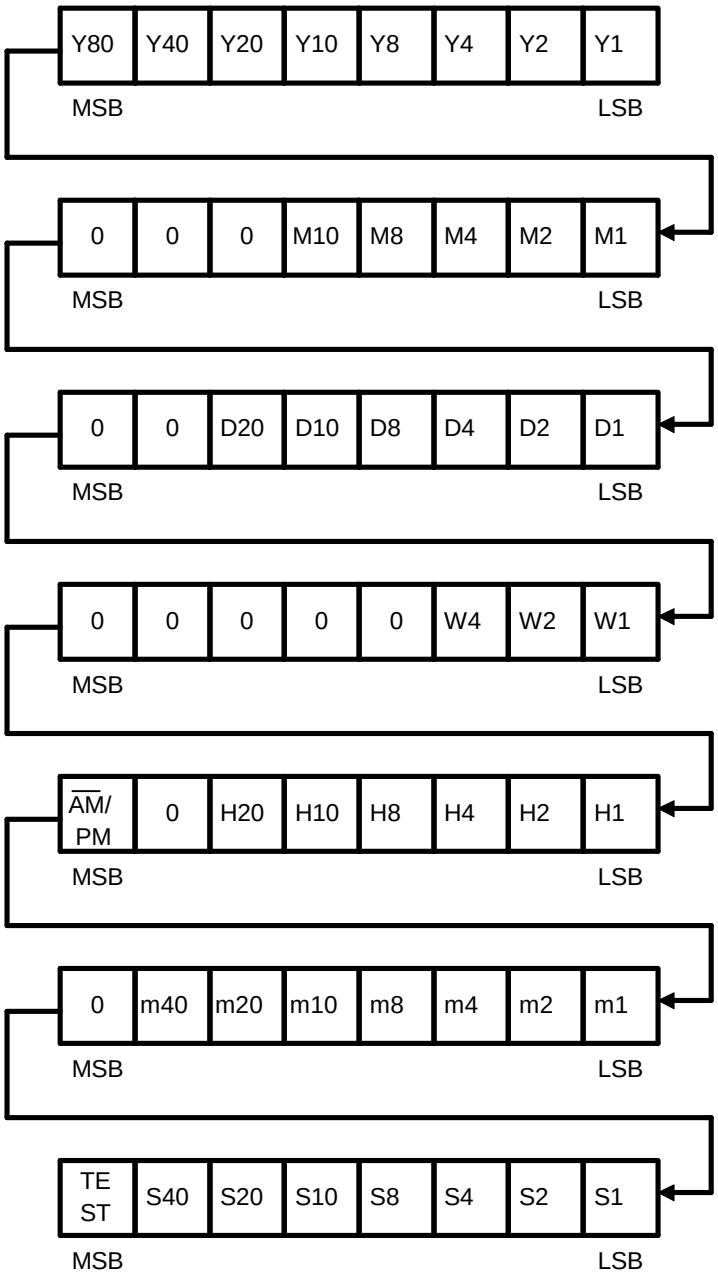
Table 2 Command list

C2	C1	C0	Description	Number of ACK
0	0	0	Reset (00 (year), 01 (month), 01 (day), 0 (day of week), 00 (minute), 00 (second)) (*1)	1
0	0	1	Status register access	2
0	1	0	Real-time data access 1 (year data to)	8
0	1	1	Real-time data access 2 (hour data to)	4
1	0	0	Alarm time/frequency duty setting 1 (for $\overline{INT1}$ pin)	3
1	0	1	Alarm time/frequency duty setting 2 (for $\overline{INT2}$ pin)	3
1	1	0	Test mode start (*2)	1
1	1	1	Test mode end (*2)	1

(*1) Don't care the R/$\overline{W}$ bit of this command.
(*2) This command is access-disabled due to specific use for the IC test.

2-1. Real-time data register

The real-time data register is a fifty-six-bit register which stores the BCD code of the data of year, month, day, day of week, hour, minute and second. Any read/write operation performed by the real-time data access command sends or receives the data from LSB on the first digit of the year data.



Year data (00 to 99)

Sets the lower two digits of the Christian era (00 to 99) and links together with the auto calender feature till 2,099.

Month data (01 to 12)

The count value is automatically changed by the auto calender feature:

1, 3, 5, 7, 8, 10, 12: 1 to 31
4, 6, 9, 11: 1 to 30
2 (leap year): 1 to 29
2 (common year): 1 to 28

Day data (01 to 31)

Day of week data (00 to 06)

A septenary counter. Set it so that it corresponds to the day of the week.

Hour data (00 to 23 or 00 to 11)

$\overline{\text{AM}}$/PM : For 12-hour expression, 0:AM and 1:PM. For 24-hour expression, this flag has no meaning but either 0 or 1 must be written.

Minute data (00 to 59)

Second data (00 to 59) and test flag

TEST : Turns to “1” during the test mode.

Figure 9 Real-time data register

2-2. Status register

The status register is an eight-bit register which allows you to display and set various modes. The POWER flag is read-only and others are read/write-enabled.

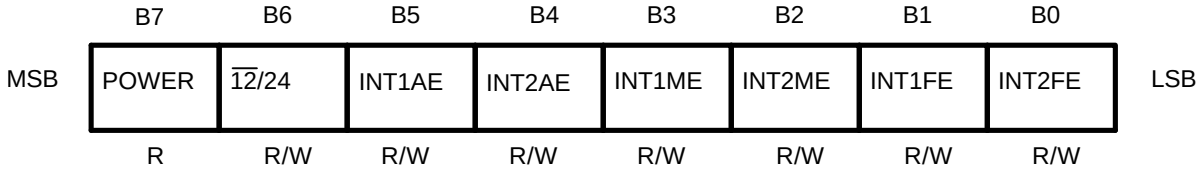


Figure 10 Status register

B7:POWER This flag turns to "1" if the power voltage detecting circuit operates during power-on or changes in power voltage (below VDET). Once turning to "1", this flag does not turns back to "0" even when the power voltage reaches or exceeds the detection voltage. When the flag is "1", you must send the reset command (or status register command) and turn it to "0." It is a read-only flag.

B6:$\overline{12}$/24 This flag is used to set 12-hour or 24-hour expression.

0 : 12-hour expression
1 : 24-hour expression

B5:INT1AE, B4:INT2AE

This flag is used to choose the state of $\overline{INT1}$ pin (or $\overline{INT2}$ pin) output with alarm interrupt output set. Enable this flag after setting alarm time that forms a meeting condition in the INT1 register (or INT2 register):

0 : Alarm interrupt output is disabled.
1 : Alarm interrupt output is enabled.

B3:INT1ME, B2:INT2ME

This flag is used to make the output of the $\overline{INT1}$ pin (or $\overline{INT2}$ pin) per-minute edge interrupt or per-minute steady interrupt. To make the output per-minute steady interrupt, set "1" at INT1ME and INT1FE (or INT2ME and INT2FE).

0 : Alarm interrupt or selected frequency steady interrupt output
1 : Per-minute edge interrupt or per-minute steady interrupt output

B1:INT1FE, B0:INT2FE

This flag is used to make the output of the $\overline{INT1}$ pin (or $\overline{INT2}$ pin) per-minute steady interrupt output (a period of one minute, 50% of duty) or selected frequency steady interrupt. Note that the INT1 register (INT2 register) is considered as the data of frequency/duty if selected frequency steady interrupt is chosen.

0 : Alarm interrupt or per-minute edge interrupt output
1 : Per-minute steady interrupt or selected frequency steady interrupt output

2-3. Alarm time/Frequency duty setting register

There are two types of alarm time/frequency duty setting registers, sixteen-bit registers, which set alarm time or frequency duty. They are switched by INTxAE or INTxFE register. AM/PM flag to be set must be in accordance with 12-hour or 24-hour expression. If AM/PM flag is not rightly then set hour data is not met to alarm data. The alarm time/frequency duty setting register is a write-only register.

(1) When INTxAE = 1

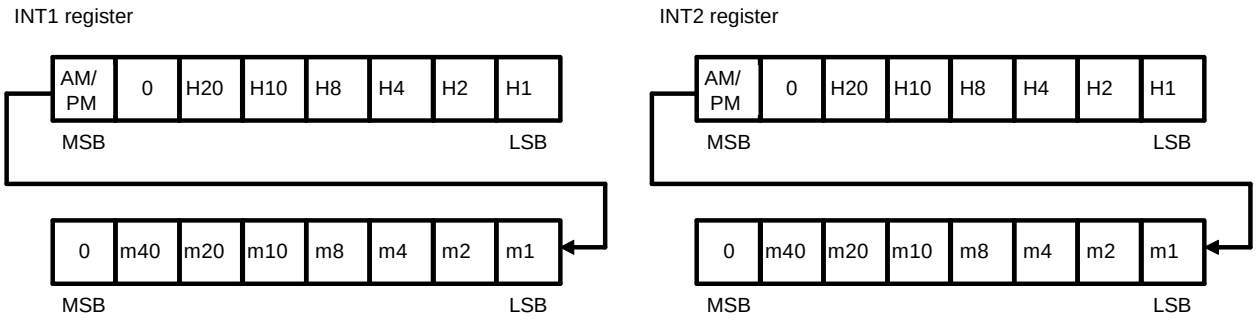
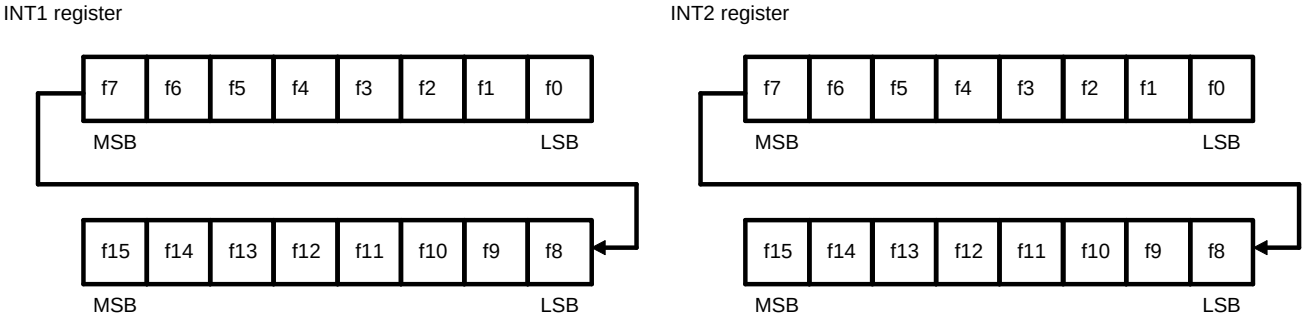


Figure 11 INT1 and INT2 registers (alarm)

INT1 and INT2 registers are considered as alarm time data. Having the same configuration as the time and minutes registers of real-time data register configuration, they represent hours and minutes with BCD codes. When setting them, do not set any none-existent day. Data to be set must be in accordance with 12-hour or 24-hour expression that is set at the status register.

(2) When INTxFE = 1

INT1 and INT2 registers are considered as frequency duty data. By turning each bit of the registers to "1", a frequency corresponding to each bit is chosen in an ANDed form.



f0	32768 Hz	f4	2048 Hz	f8	128 Hz	f12	8 Hz
f1	16384 Hz	f5	1024 Hz	f9	64 Hz	f13	4 Hz
f2	8192 Hz	f6	512 Hz	f10	32 Hz	f14	2 Hz
f3	4096 Hz	f7	256 Hz	f11	16 Hz	f15	1 Hz

Figure 12 INT1 and INT2 registers (frequency duty)

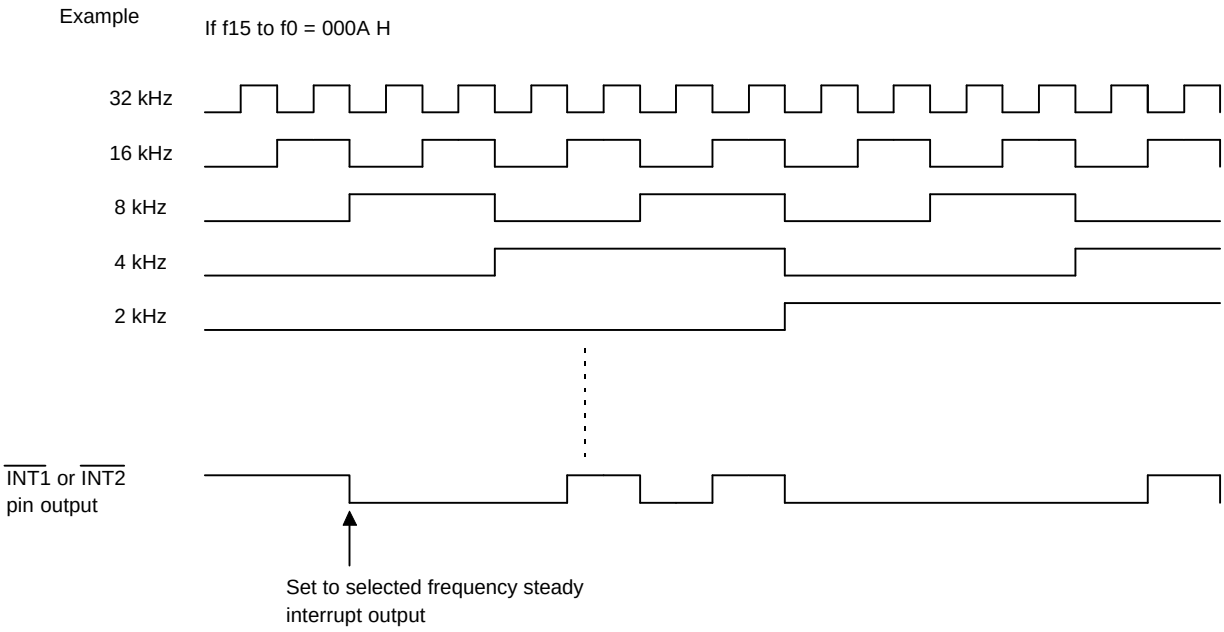


Figure 13 Clock output

2-4. Test flag

The test flag is a one-bit register which is assigned to MSB of the second data of the real-time data register. If transferred data is considered as the test mode starting command due to the receiving of the test mode starting command or noises, "1" is set. When "1" is set, you must send the test mode ending command or reset command.

3. Initialization

Note that S-3530A has different initializing operations, depending on states.

3-1. When power is turned on

When power is turned on, the status register is set to "82h" and the INT1 register to "8000h" by the power-on detecting circuit. In other words, "1" is sets at the bit 7 (POWER flag) of the status register and the clock of 1 Hz is output from the INT1 pin. This is provided to adjust oscillating frequencies. In normal use, the reset command must be sent when power is turned on.

Real-time data register : 00 (year), 01 (month), 01 (day), 0 (day of week), 00 (hour), 00 (minute), 00 (second)
Status register : "82h"
INT1 register : "8000h" INT2 register : "0000h"

3-2. When the power voltage detecting circuits operates

The power voltage detecting circuit included in S-3530A operates and sets "1" at the bit 7 (POWER flag) of the internal status register when power is turned on or power voltage is reduced. Once "1" is set, it is held even after the power voltage gets equal to or higher than the detection voltage, i.e., the power voltage detector threshold. When the flag has "1," you must send the reset command from CPU and initialize the flag. At this point, other registers does not change.
However, if the POWER flag has "0" during the power-on reset of CPU (S-3530A does not reach any indefinite area during backup), you do not have to send the reset command.

3-3. When the reset command is received

When the reset command is received, each register turns as follows:

Real-time data register : 00 (year), 01 (month), 01 (day), 0 (day of week), 00 (hour), 00 (minute), 00 (second)
Status register : "00h"
INT1 register : "0000h" INT2 register : "0000h"

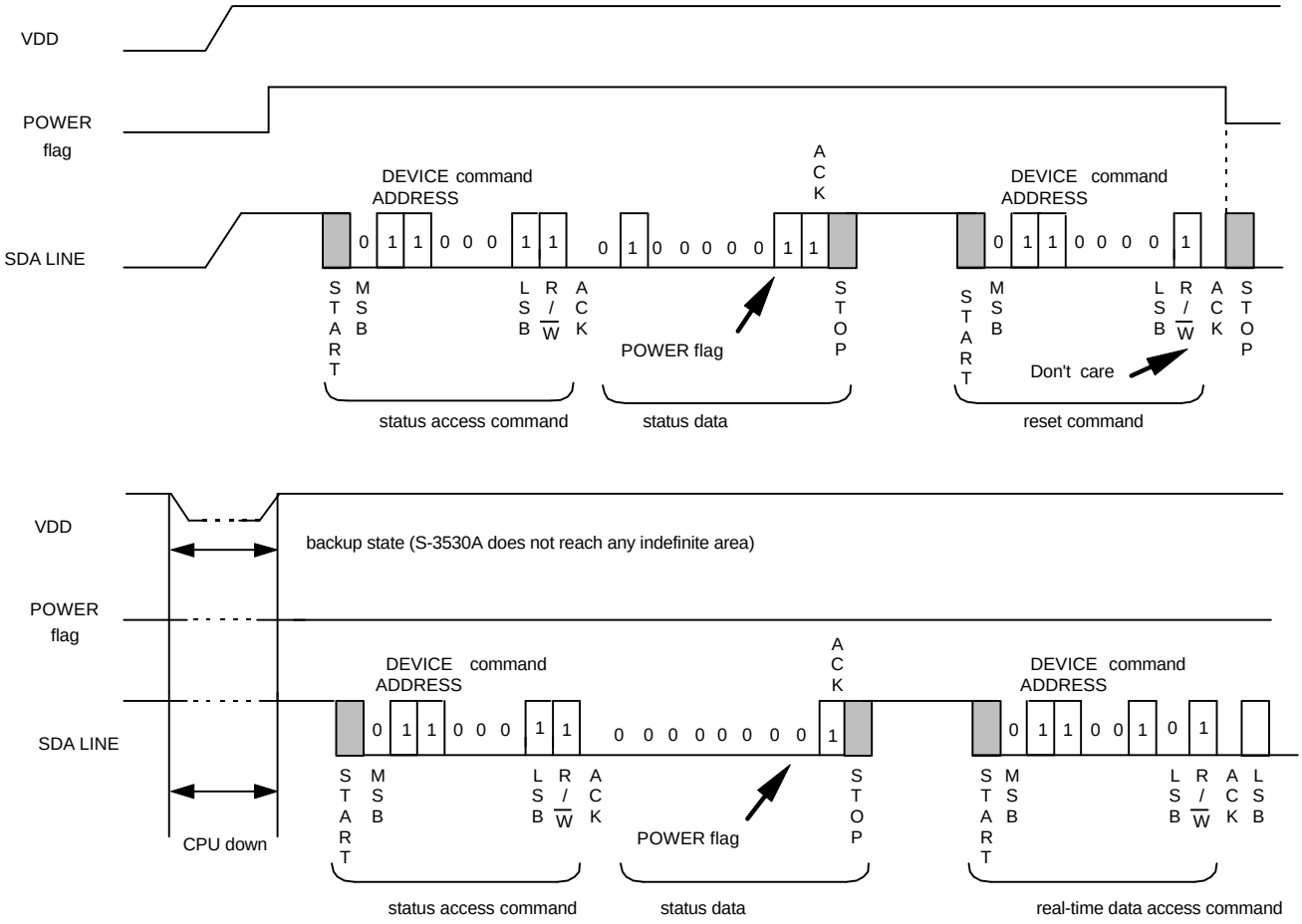


Figure 14 Initializing

4. Processing of none-existent data and end-of-month

When writing real-time data, validate it and treat any invalid data and end-of-month correction.

[None-existent data processing]

Table 3 None-existent data processing

Register	Normal data	Error data	Result
Year data	00 to 99	XA to XF, AX to FX	00
Month data	01 to 12	00, 13 to 19, XA to XF	01
Day data	01 to 31	00, 32 to 39, XA to XF	01
Day of week data	0 to 6	7	0
Hour data (24-hour) (*) (12-hour)	0 to 23 0 to 11	24 to 29, 3X, XA to XF 12 to 19, XA to XF	00 00
Minute data	00 to 59	60 to 79, XA to XF	00
Second data (**)	00 to 59	60 to 79, XA to XF	00

(*) For 12-hour expression, write the AM/PM flag.
The AM/PM flag is ignored in 24-hour expression, but "0" for 0 to 11 o'clock and "1" for 12 to 23 o'clock are read in a read operation.

(**) None-existent data processing for second data is performed by a carry pulse one second after the end of writing. At this point, the carry pulse is sent to the minute counter.

[End-of-month correction]

Any none-existent day is corrected to the first day of the next month. For example, February 30 is changed to March 1. Leap-year correction is also performed here.

5. Interrupt

There are different five output formats from the INT1 and INT2 pins, which are chosen by the INTxAE, INTxME and INTxFE bits of the status register (x:1 or 2).

(1) Alarm interrupt output
Alarm interrupt is enabled by setting hour and minute data to the INT1 register (or INT2 register) and turning the status register's INT1AE to "1" and INT1ME and INT1FE to "0" (or INT2AE to "1" and INT2ME and INT2FE to "0"). When set hour data is met, low is output from the INT1 pin (or INT2 pin). Since the output is held, rewrite INT1AE (or INT2AE) of the status register to "0" through serial communication to turn the output to high (OFF state).
The coincidence signal retains for one minute. Pay attention that the “Low” signal is output from the INTx pin once again when DISABLE or ENABLE communication is executed during this one-minute period.

(2) Selected frequency steady interrupt output
When you set frequency/duty data to the INT1 register (or INT2 register) and turn the status register's INT1ME to "0" and INT1FE to "1" (or INT2ME to "0" and INT2FE to "1"), clock set at the INTx register is output from the INT1 pin (or INT2 pin).

(3) Per-minute edge interrupt output
When a first minute carry is performed after the status register's INT1ME is set with "1" and INT1FE with "0" (or INT2ME with "1" and INT2FE with "0"), low is output from the INT1 pin (or INT2 pin). Since the output is held, rewrite INT1AE, INT1ME and INT1FE (or INT2AE, INT1ME and INT2FE) of the status register to "0" through serial communication to turn the output to high (OFF state). When you perform DISABLE or ENABLE communication while the minute carry processing signal is being retained (for 10 msec), "Low" signal is output from the INTx pin again.

(4) Per-minute steady interrupt output
When a first minute carry is performed after the status register's INT1ME and INT1FE are set with "1" (or INT2ME and INT2FE with "1"), clock is output from the INT1 pin (or INT2 pin) with a period of one minute (50% duty). When you perform DISABLE or ENABLE communication while the INTx pin is at "L," "Low" signal is output from the INTx pin again.

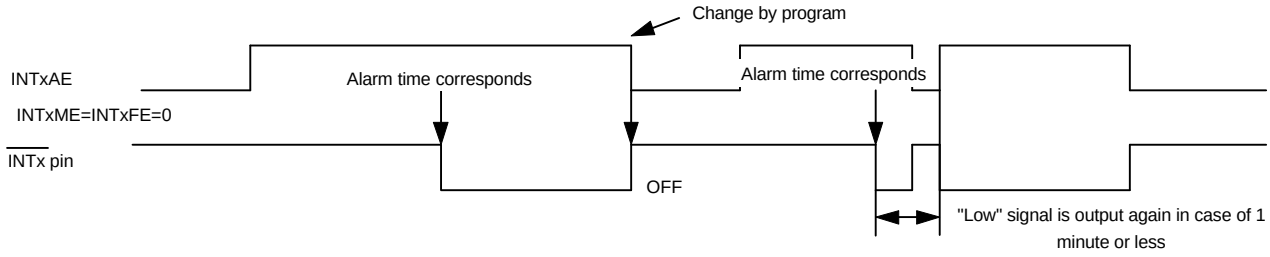
Note 1 : If changing an output mode, give care to the state of the INT1 and INT2 registers and output.
Note 2 : If per-minute edge interrupt output or per-minute steady interrupt output is chosen, the INT1 and INT2 registers have no meaning.

Table 4 Interrupt description

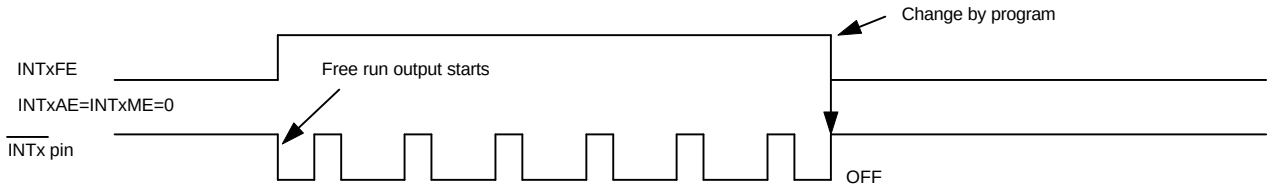
NO.	INT1AE	INT1ME	INT1FE	Description
0	0	0	0	$\overline{\text{INT1}}$ pin output disabled (No interrupt output)
1	*	0	1	Selected frequency steady interrupt output from the $\overline{\text{INT1}}$ pin
2	*	1	0	Per-minute edge interrupt output from the $\overline{\text{INT1}}$ pin
3	*	1	1	Per-minute steady interrupt output from $\overline{\text{INT1}}$ pin
4	1	0	0	Alarm interrupt output from $\overline{\text{INT1}}$ pin
NO.	INT2AE	INT2ME	INT2FE	Description
5	0	0	0	$\overline{\text{INT2}}$ pin output disabled (No interrupt output)
6	*	0	1	Selected frequency steady interrupt output from the $\overline{\text{INT2}}$ pin
7	*	1	0	Per-minute edge interrupt output from the $\overline{\text{INT2}}$ pin
8	*	1	1	Per-minute steady interrupt output from $\overline{\text{INT2}}$ pin
9	1	0	0	Alarm interrupt output from $\overline{\text{INT2}}$ pin

Note * : Don't care (both 0 and 1 are available)

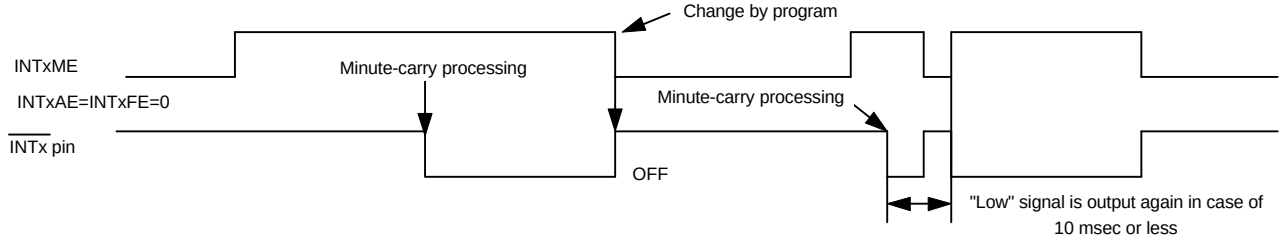
(1) Alarm interrupt output



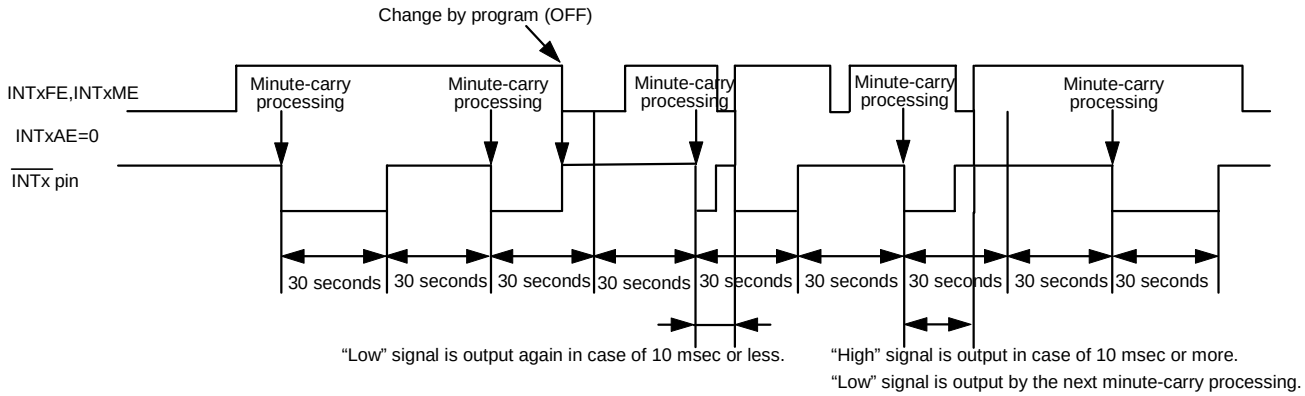
(2) Selected frequency steady interrupt output



(3) Per-minute edge interrupt output



(4) Per-minute steady interrupt output



(5) During power-on detecting circuit operation

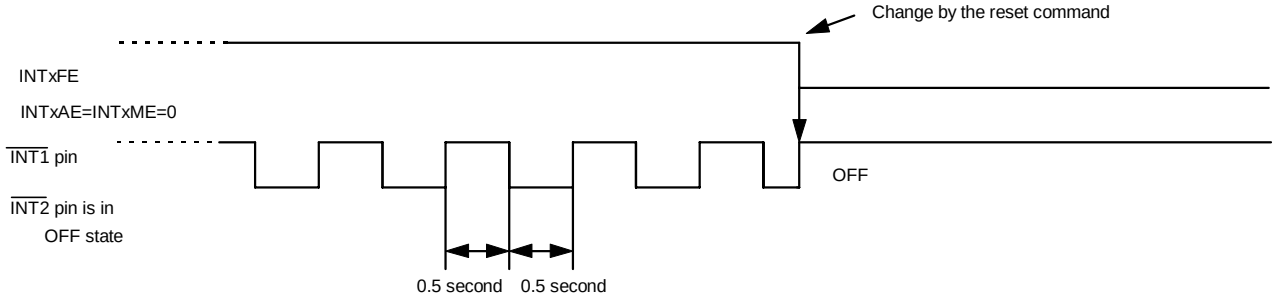


Figure 15 Output mode

6. Power voltage detecting circuit

S-3530 has an internal power voltage detecting circuit. This circuit gives sampling movement for only 15.6msec. once a second.
If the power voltage decreases below the detection voltage (VDET), the BLD latch circuit latches “H” level and sampling movement stops. Only when subsequent communication is of the status read command, the output of the latch circuit is transferred to the sift register and the sampling movement is resumed.
Decrease in power voltage can be monitored by reading the POWER flag.
That is to say, once decrease in power voltage is detected, any detecting operation is not performed and "H" is held unless you perform initialization or send the status read command.

[Note]
When power voltage is increased and the first read operation is performed after decrease in power voltage occurs and the latch circuit latches "H", "1" can be read on the POWER flag. However, if the next read operation is performed after the sampling of the detecting circuit, the POWER flag is reset since sampling is subsequently allowed. See the timing diagram below.

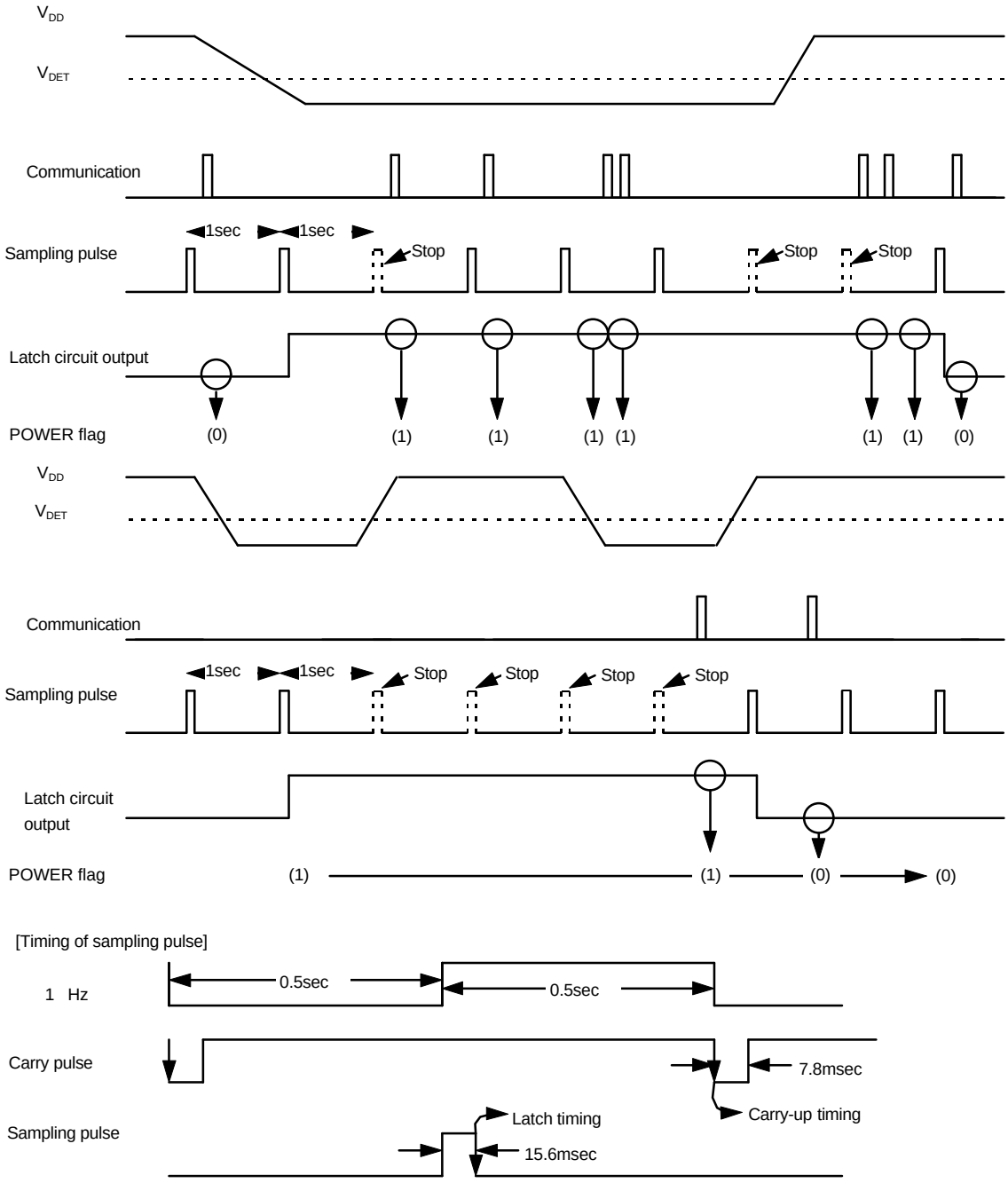
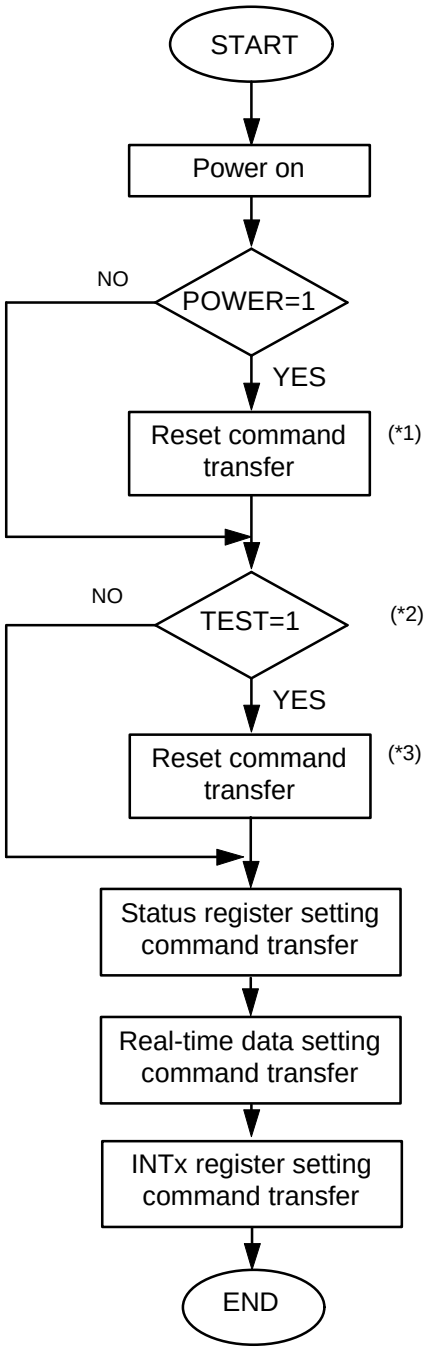


Figure 16 Timing of the power voltage detecting circuit

7. Example of software treatment

(1) Initialization flow at power-on



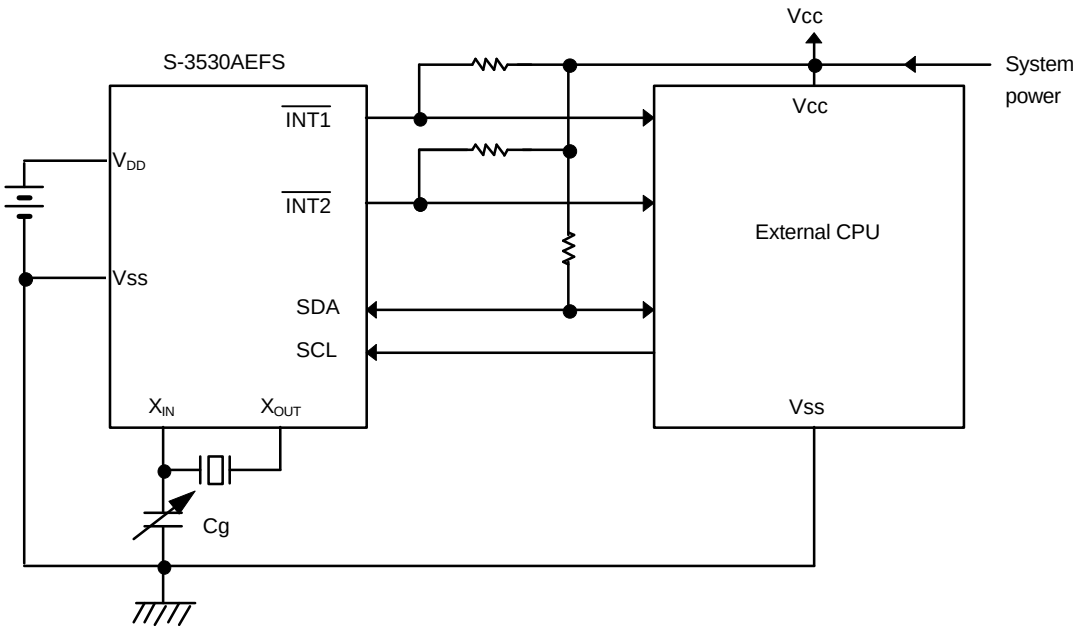
(*1) If S-3530 is back-up and power is turned on only on the CPU side, the reset command does not need transferring.

(*2) If conditions are no good (e.g., noise) and probable changes in commands occurs via serial communications, it is recommended to make sure the TEST flag.

(*3) The test ending command may be used alternately

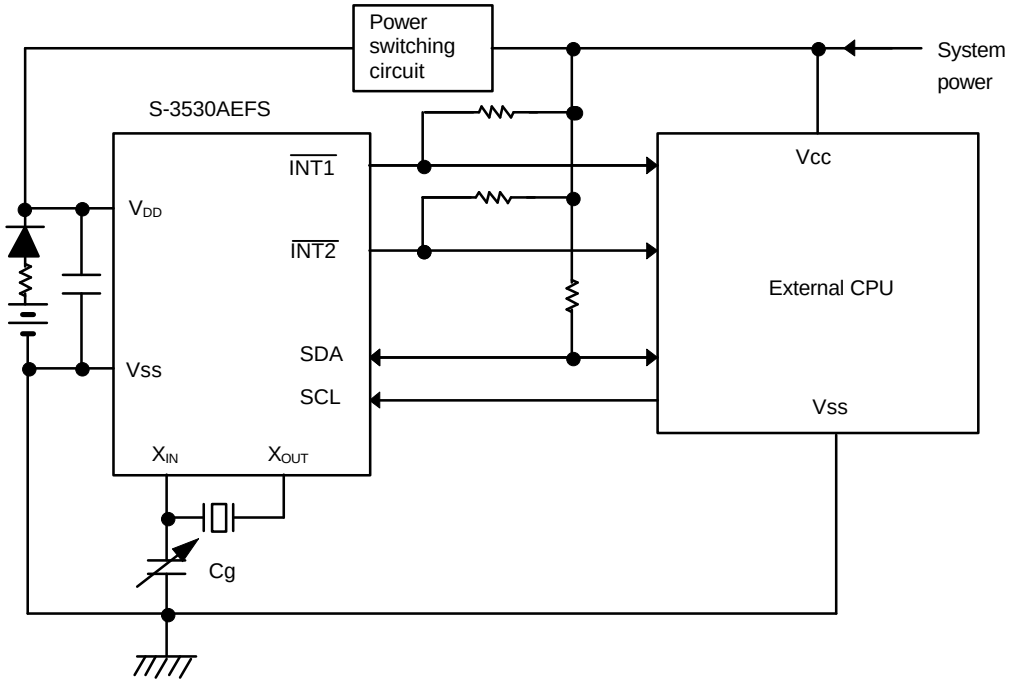
Figure 17 Initialization flow

■ Samples of Applied Circuits



Due to the I/O pin with no protective diode on the VDD side, the relation of VCC≥VDD has no problem. But give great care to the standard.
Make communications after the system power is turned on and a stable state is obtained.

Figure 18 Applied circuit 1



Make communications after the system power is turned on and a stable state is obtained.

Figure 19 Applied circuit 2

■ Order Specification

S-3530AE FS

Shipping form: FS: Package (8-pin SSOP)
CA: Die

Description (fixed)

■ Adjustment of Oscillating Frequency

1. Configuration of the oscillating circuit

   Since crystal oscillation is sensitive to external noises (clock accuracy is affected), the following measures are essential for optimizing your oscillating circuit configuration:

   (1) S-3530A, crystal oscillator and external capacitor (Cg) are placed as close to each other as possible.

   (2) Make high the insulation resistance between pins and the substrate wiring patterns of XIN and XOUT.

   (3) Do not place any signal or power lines close to the oscillating circuit.

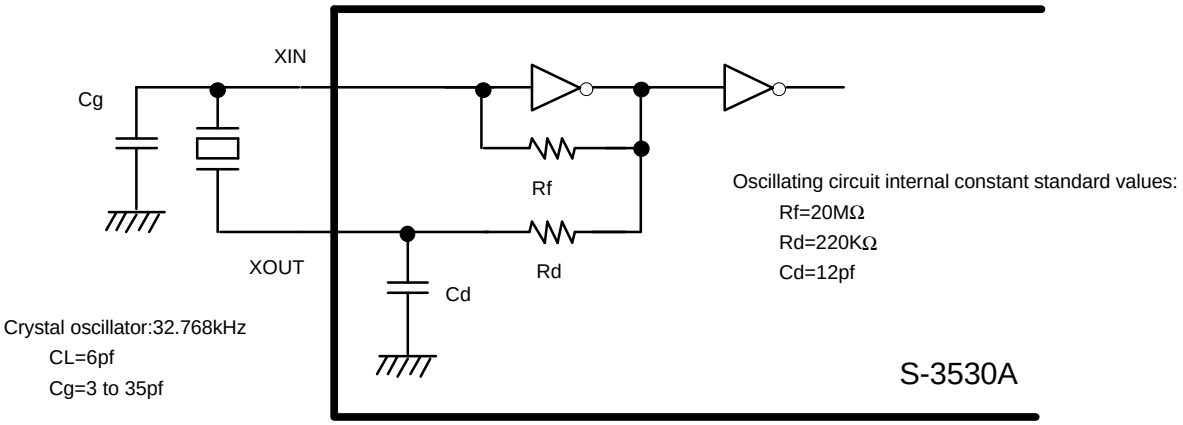
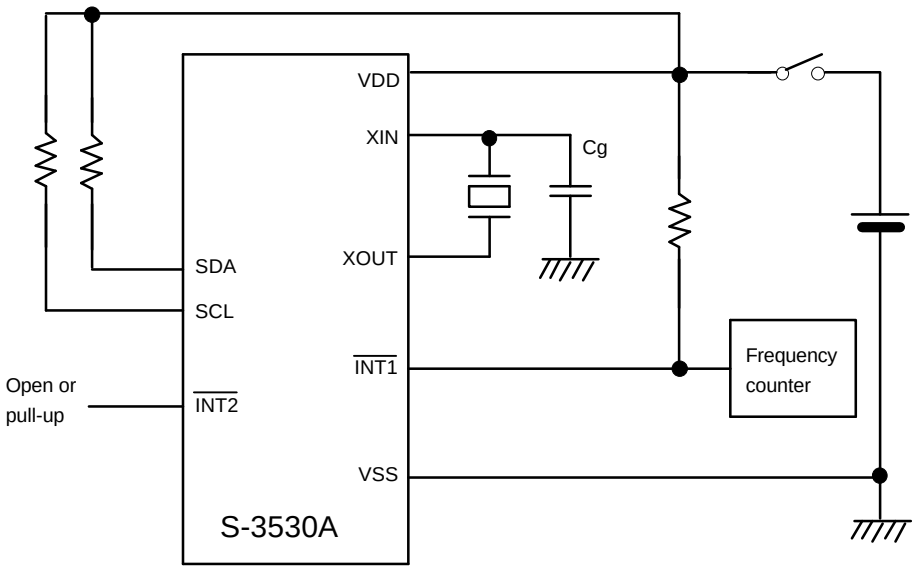


Figure 20 Connection diagram

2. Measurement of oscillating frequencies

When power is turned on, S-3530A has the internal power-on detecting circuit operating and outputs a signal of 1 Hz from the $\overline{INT1}$ pin to select the crystal oscillator and optimize the Cg value. Turn power on and measure the signal with a frequency counter following the circuit configuration shown in Figure 21. Refer to 12 and 16 pages in this document for further information.

(*) If the error range is ±1ppm in relation to 1 Hz, time is shifted by approximately 2.6 seconds a month:
10^{-6} (1ppm) × 60 seconds × 60 minutes × 24 hours × 30 days = 2.592 seconds

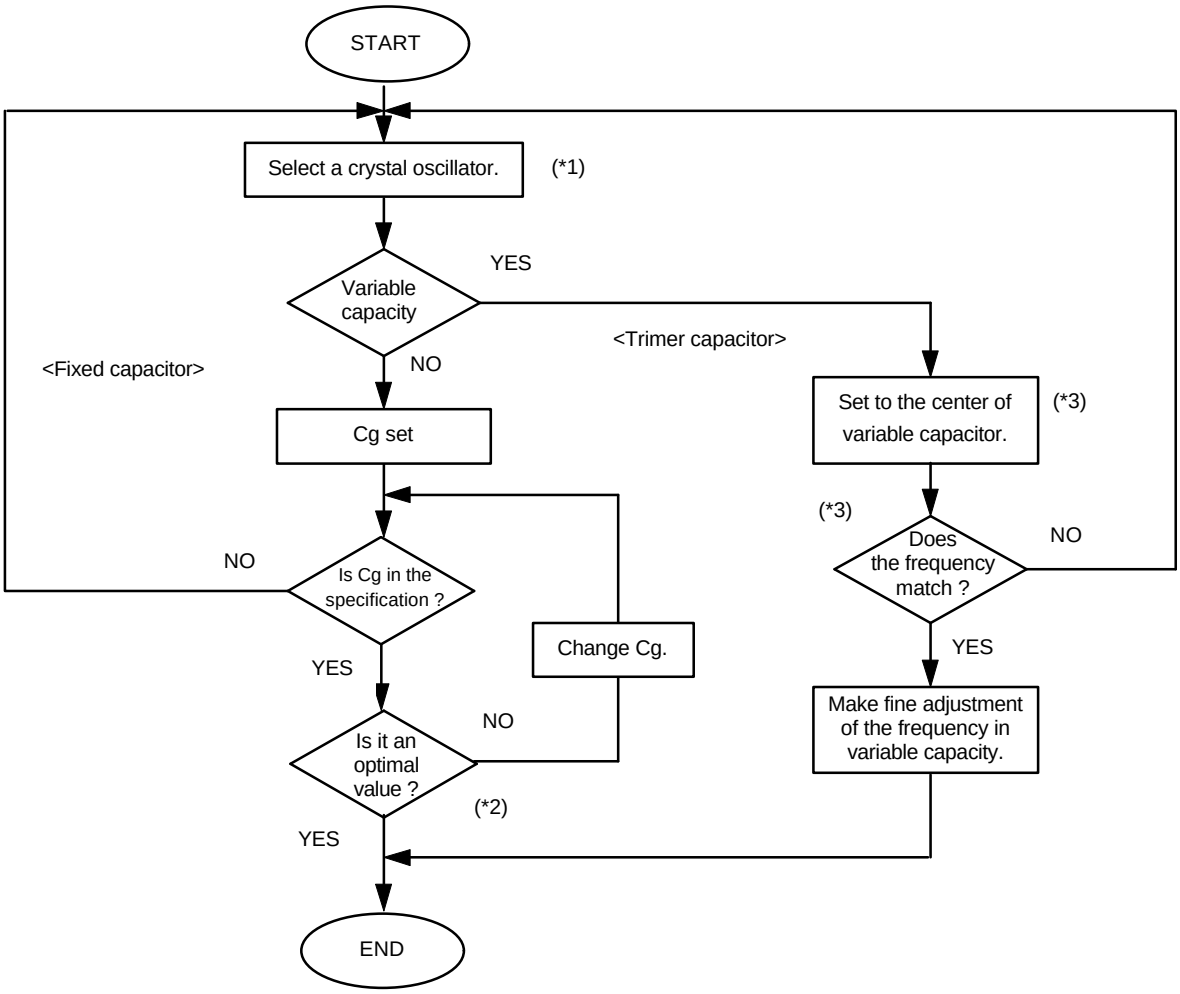


Note 1: Use a high-accuracy frequency counter (1ppm order).
Note 2: Since the 1 Hz signal continues to be output, you must send the reset command in normal operation.
Note 3: Determine Cg with its frequency slow/fast range property referred.

Figure 21 Connection diagram

3. Adjustment of oscillating frequencies

Matching of a crystal oscillator with the nominal frequency must be performed with parasitic capacitance on the board included. Select a crystal oscillator and optimize the Cg value in accordance with the flow chart below.



(*1) For making matching adjustment of the IC with a crystal, contact an appropriate crystal maker to determine the CL value (load capacity) and RI value (equivalent serial resistance). The CL value = 6 pf and RI value = 30 kΩ TYP. are recommended values.

(*2) Cg value selection must be performed on the actual PCB since parasitic capacitance affects it. Select the Cg value in a range from 3 pf to 35 pf. If the frequency does not match, change the CL value of the crystal.

(*3) Adjust the rotation angle of the variable capacity so that the capacity value is somewhat smaller than the center, and confirm the oscillating frequency and the center value of the variable capacity. This is done in order to make the capacity of the center value smaller than one half of the actual capacity value because a smaller capacity value makes a greater quantity of changes in a frequency. If the frequency does not match, change the CL value of the crystal.

Note 1 : Oscillating frequencies are changed by ambient temperature and power voltage. Refer to property samples.

Note 2 : The 32 kHz crystal oscillator operates slower at higher or lower ambient temperature than 20 to 25°C. Therefore, it is recommended to adjust or set the oscillator to operate somewhat faster at normal temperature.

■ Absolute Maximum Ratings

Table 5 Absolute maximum ratings

Item	Symbol	Rating	Unit	Applicable pin, conditions
Power voltage	VDD	-0.3 to +6.5	V	—
Input voltage	V_{IN}	-0.3 to +6.5	V	SCL,SDA
Output voltage	V_{OUT}	-0.3 to +6.5	V	SDA,$\overline{INT1}$, $\overline{INT2}$
Operating temperature	T_{opr}	-40 to +85	°C	VDD=3.0V
Storage temperature	T_{stg}	-55 to +125	°C	—

■ Recommended Operating Conditions

Table 6 Recommended operating conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power voltage	VDD	—	1.7	3.0	5.5	V
Operating temperature	T_{opr}	—	-20	+25	+70	°C

■ Oscillation Characteristics

Table 7 Oscillation characteristics

(Ta=25°C, VDD=3V, DS-VT-200 (crystal oscillator, CL=6pF, 32,768Hz) manufactured by Seiko Instruments Inc.)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{STA}	Within ten seconds	1.7	—	5.5	V
Oscillation start time	T_{STA}	—	—	—	1	SEC
IC-to-IC frequency diversity	δIC	—	-10	—	+10	ppm
Frequency voltage diversity	δV	VDD=1.7 to 5.5V	-3	—	+3	ppm/V
Input capacity	Cg	Applied to the XIN pin	3	—	35	pF
Output capacity	Cd	Applied to the XOUT pin	—	12	—	pF

■ DC Electrical Characteristics

Table 8 DC characteristics (3V)

(Ta=25°C, VDD=3V, DS-VT-200 (crystal oscillator, CL=6pF, 32,768Hz) manufactured by Seiko Instruments Inc.)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Range of operating voltage	VDD	Ta=-20 to +70°C	1.7	3.0	5.5	V	—
Current consumption 1	I_{DD1}	During no communications	—	0.7	1.5	µA	—
Current consumption 2	I_{DD2}	During communications (SCL=100 kHz)	—	12	20	µA	—
Input leak current 1	I_{IZH}	V_{IN}= VDD	-0.5	—	0.5	µA	SCL,SDA
Input leak current 2	I_{IZL}	V_{IN}= VSS	-0.5	—	0.5	µA	SCL,SDA
Output leak current1	I_{OZH}	V_{OUT}=VDD	-0.5	—	0.5	µA	$\overline{INT1}$,$\overline{INT2}$ SDA
Output leak current2	I_{OZL}	V_{OUT}=VSS	-0.5	—	0.5	µA	$\overline{INT1}$,$\overline{INT2}$ SDA
Input voltage 1	V_{IH}	—	0.8xVDD	—	—	V	SDA,SCL
Input voltage 2	V_{IL}	—	—	—	0.2xVDD	V	SDA,SCL
Output current 1	I_{OL1}	V_{OUT}=0.4V	1.5	2.5	—	mA	$\overline{INT1}$,$\overline{INT2}$
Output current 2	I_{OL2}	V_{OUT}=0.4V	5	10	—	mA	SDA
Power voltage detection voltage 1	V_{DET1}	Ta=+25°C	1.8	2.0	2.2	V	—
Power voltage detection voltage 2	V_{DET2}	Ta=-20 to +70°C	1.72	—	2.3	V	—

Table 9 DC characteristics (5V)

(Ta=25°C, VDD=3V, DS-VT-200 (crystal oscillator, CL=6pF, 32,768Hz) manufactured by Seiko Instruments Inc.)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Range of operating voltage	VDD	Ta=-20 to +70°C	1.7	3.0	5.5	V	—
Current consumption 1	I_{DD1}	During no communications	—	1.6	3.0	µA	—
Current consumption 2	I_{DD2}	During communications (SCL=100 kHz)	—	26	40	µA	—
Input leak current 1	I_{IZH}	V_{IN}= VDD	-0.5	—	0.5	µA	SCL,SDA
Input leak current 2	I_{IZL}	V_{IN}= VSS	-0.5	—	0.5	µA	SCL,SDA
Output leak current1	I_{OZH}	V_{OUT}=VDD	-0.5	—	0.5	µA	$\overline{INT1}$,$\overline{INT2}$ SDA
Output leak current2	I_{OZL}	V_{OUT}=VSS	-0.5	—	0.5	µA	$\overline{INT1}$,$\overline{INT2}$ SDA
Input voltage 1	V_{IH}	—	0.8xVDD	—	—	V	SDA,SCL
Input voltage 2	V_{IL}	—	—	—	0.2xVDD	V	SDA,SCL
Output current 1	I_{OL1}	V_{OUT}=0.4V	2.0	3.5	—	mA	$\overline{INT1}$,$\overline{INT2}$
Output current 2	I_{OL2}	V_{OUT}=0.4V	6	12	—	mA	SDA
Power voltage detection voltage 1	V_{DET1}	Ta=+25°C	1.8	2.0	2.2	V	—
Power voltage detection voltage 2	V_{DET2}	Ta=-20 to +70°C	1.72	—	2.3	V	—

■ AC Electrical Characteristics

Table 10 Measurement conditions

Input pulse voltage	0.1×VDD to 0.9×VDD
Input pulse rising/falling time	20ns
Output judgment voltage	0.5×VDD
Output load	100pF+pull-up resistance 1.0kΩ

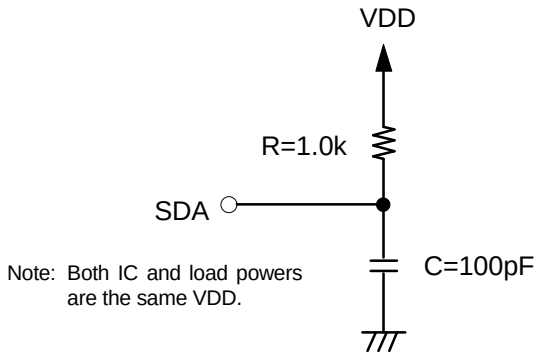


Figure 22 Output load circuit

Table 11 AC properties

Item	Symbol	VDD=1.7V to 5.5V			Unit
		Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	0	—	100	kHz
SCL clock “L” time	t_{LOW}	4.7	—	—	µs
SCL clock “H” time	t_{HIGH}	4.0	—	—	µs
SDA output delay time	t_{PD}	—	—	3.5	µs
Start condition setup time	$t_{SU.STA}$	4.7	—	—	µs
Start condition holding time	$t_{HD.STA}$	4.0	—	—	µs
Data input setup time	$t_{SU.DAT}$	250	—	—	ns
Data input holding time	$t_{HD.DAT}$	150	—	—	ns
Stop condition setup time	$t_{SU.STO}$	4.7	—	—	µs
SCL, SDA rising time	t_R	—	—	1.0	µs
SCL, SDA falling time	t_F	—	—	0.3	µs
Bus release time	t_{BUF}	4.7	—	—	µs
Noise suppression time	t_I	—	—	100	ns

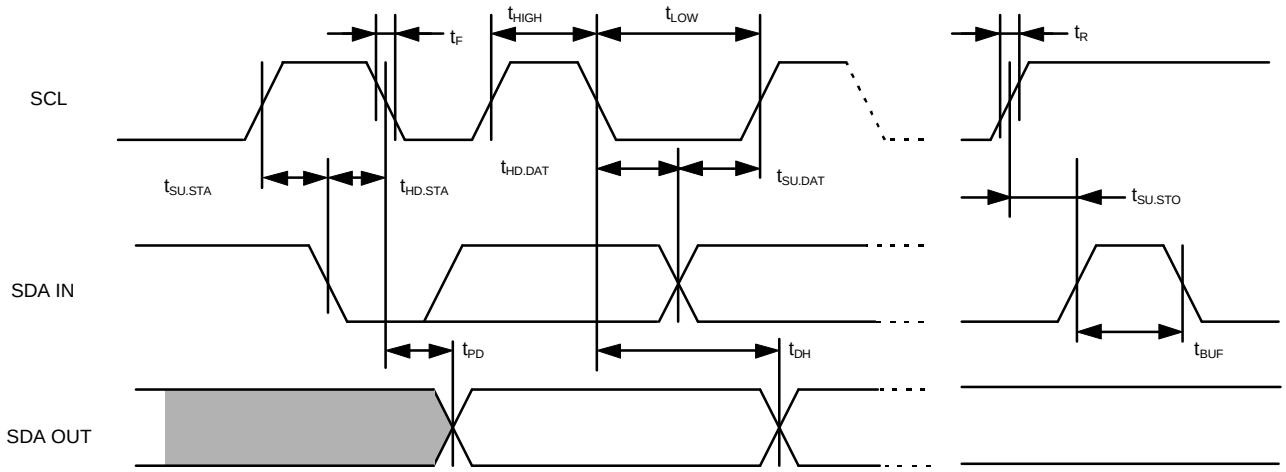
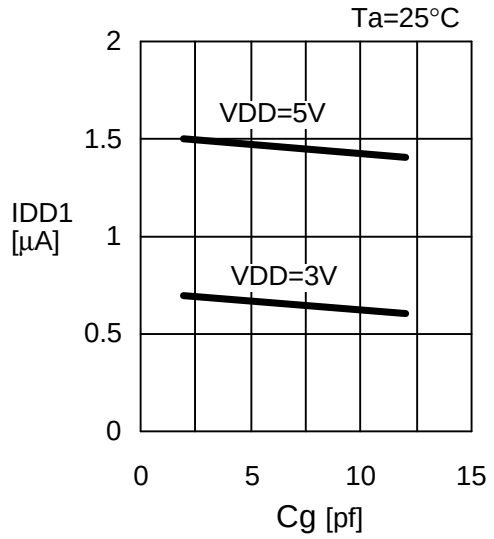


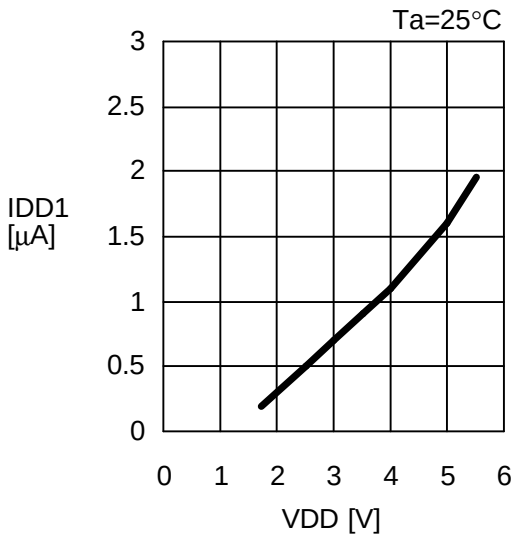
Figure 23 Bus timing

■ Sample of Characteristics (Reference values)

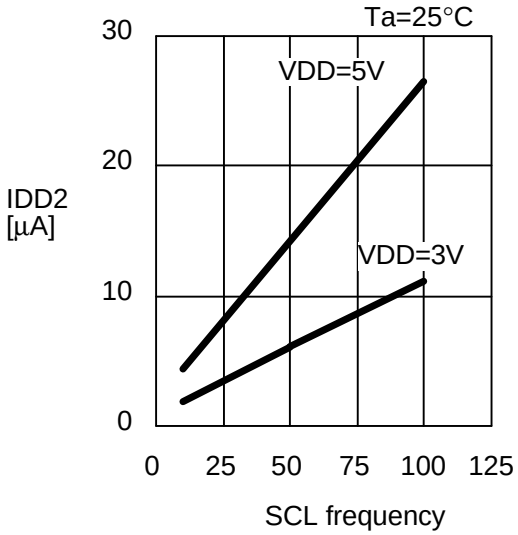
(1) Standby current versus Cg



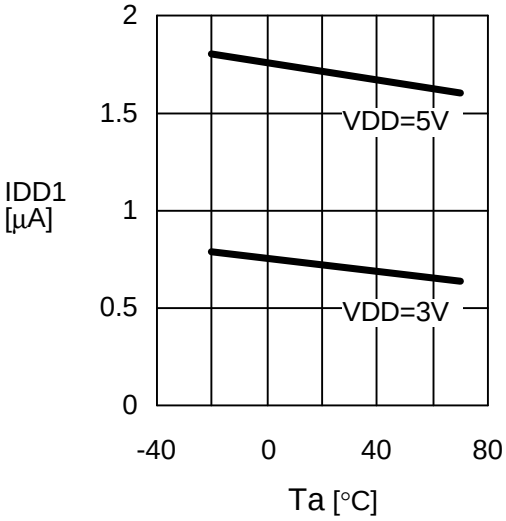
(2) Standby current versus VDD



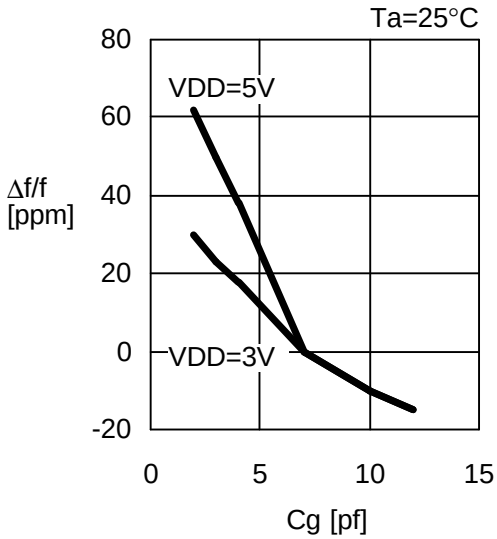
(3) Operating current consumption versus Input clock



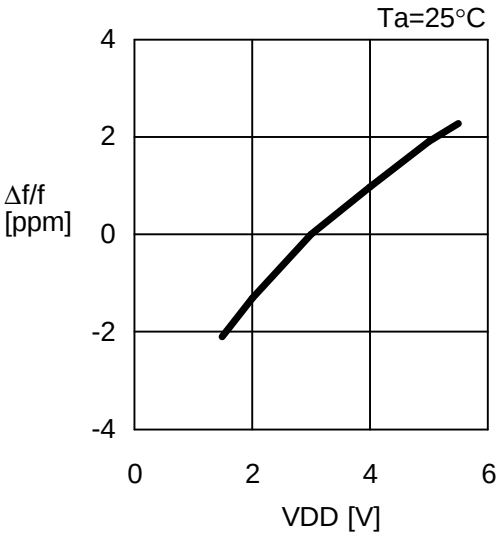
(4) Standby current versus temperature



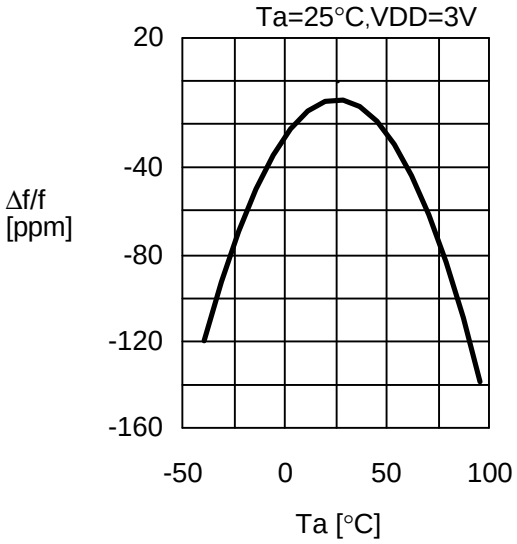
(5) Oscillating frequency versus Cg



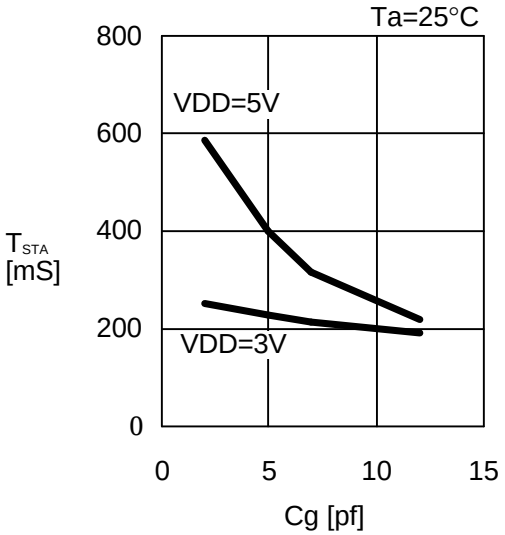
(6) Oscillating frequency versus VDD



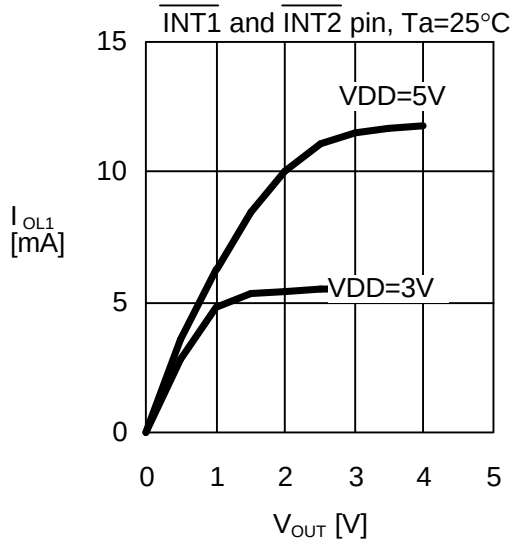
(7) Oscillating frequency versus temperature



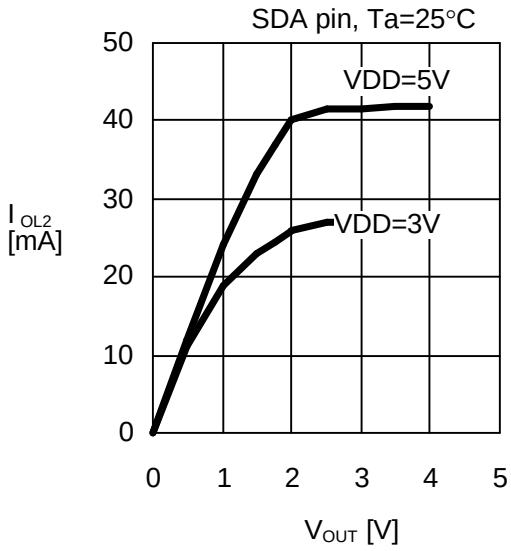
(8) Oscillation start time versus Cg



(9) Output current 1 (V_{OUT} versus I_{OL1})



(10) Output current 2 (V_{OUT} versus I_{OL2})



Purchase of I²C components of Seiko Instruments Inc. conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

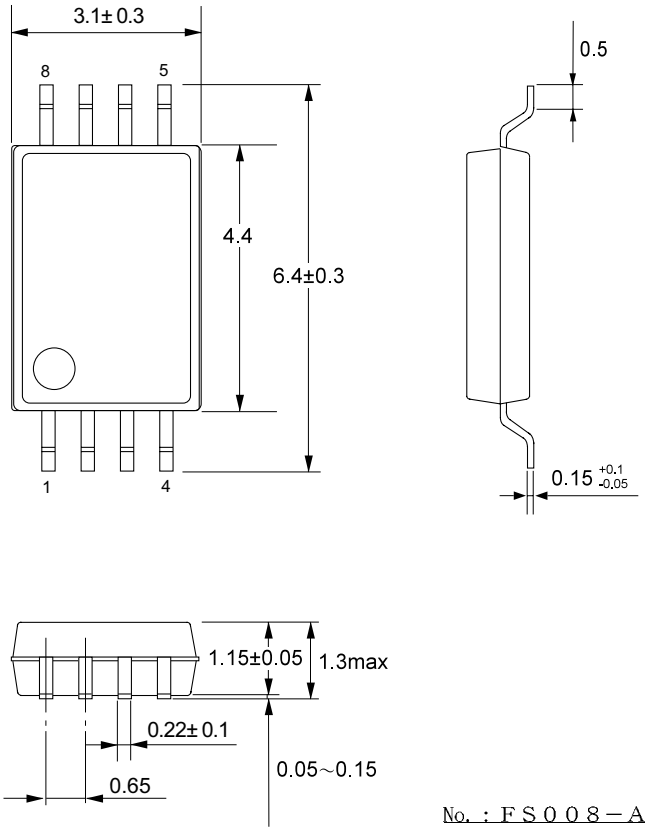
Please note that any product or system incorporating this IC may infringe upon the Philips I²C Bus Patent Rights depending upon its configuration.

In the event that such product or system incorporating the I²C Bus infringes upon the Philips Patent Rights, Seiko Instruments Inc. shall not bear any responsibility for any matters with regard to and arising from such patent infringement.

■ 8-pin SSOP

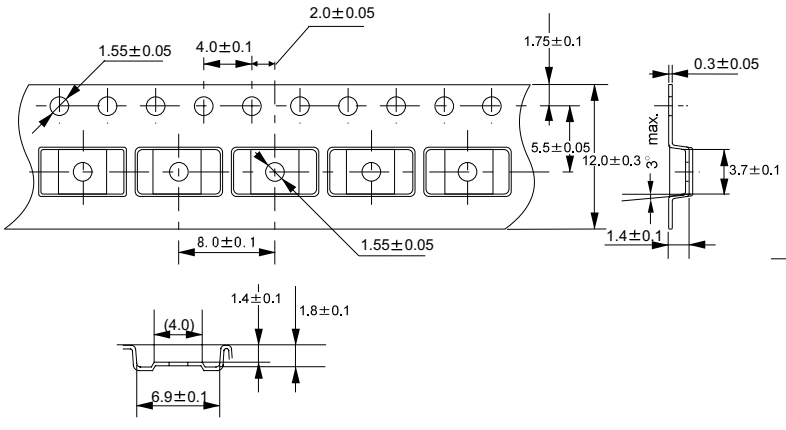
●Dimensions

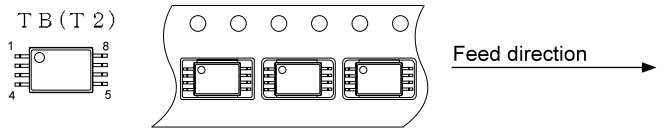
Unit:mm



No.：FS008-A-P-SD-1.0

●Taping Specifications

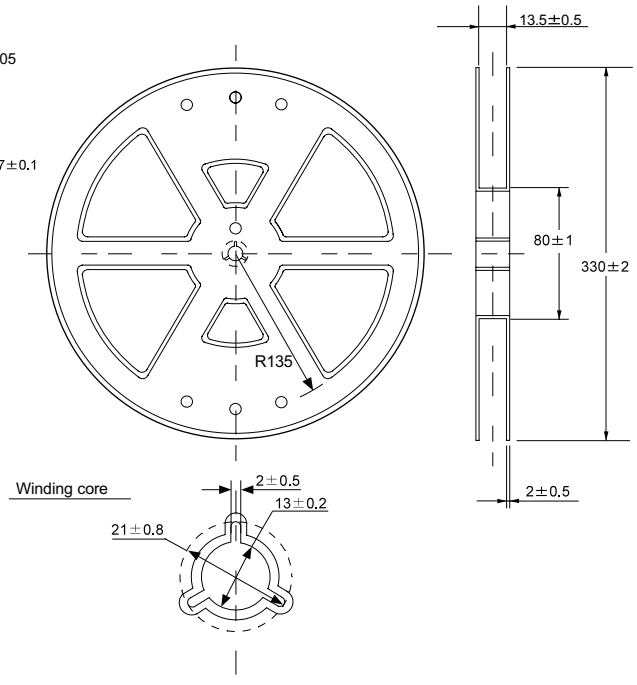




No.：FS008-A-C-SD-1.0

●Reel Specifications

1 reel holds 2000 ICs.



No.：FS008-A-R-SD-1.0

- The information described herein is subject to change without notice.
- Seiko Instruments Inc. is not responsible for any problems caused by circuits or diagrams described herein whose related industrial properties, patents, or other rights belong to third parties. The application circuit examples explain typical applications of the products, and do not guarantee the success of any specific mass-production design.
- When the products described herein are regulated products subject to the Wassenaar Arrangement or other agreements, they may not be exported without authorization from the appropriate governmental authority.
- Use of the information described herein for other purposes and/or reproduction or copying without the express permission of Seiko Instruments Inc. is strictly prohibited.
- The products described herein cannot be used as part of any device or equipment affecting the human body, such as exercise equipment, medical equipment, security systems, gas equipment, or any apparatus installed in airplanes and other vehicles, without prior written permission of Seiko Instruments Inc.
- Although Seiko Instruments Inc. exerts the greatest possible effort to ensure high quality and reliability, the failure or malfunction of semiconductor products may occur. The user of these products should therefore give thorough consideration to safety design, including redundancy, fire-prevention measures, and malfunction prevention, to prevent any accidents, fires, or community damage that may ensue.