

LINEAR IMAGE SENSOR IC FOR CONTACT IMAGE SENSOR**S-8603AWI**

The S-8603AWI is a suitable linear image sensor for a multichip-type contact image sensor with a resolution of 8 dots per mm. This IC integrates a 64dots photo-transistor array and a CMOS scanning circuit. Picture signals are output one after another in analog signals, synchronized with a clock signal.

■ Features

- Adjustable scanning length for various sizes of paper : 8mm.
 ...Various sizes of paper can be read by simply changing the number of chips aligned in a line.
- 2-input signals : SI, CLK.
 ...Only these two input signals, start and clock, make the scanning easily.
- High sensitivity : High sensitive photo transistor.
- Low current consumption : 5V single power supply and CMOS scanning circuit.

■ Terminal functions

Table-1

Terminal No.	Symbol	Name	Operation
1	SI	Start input pin	Shift register data input pin
2	CLK	Clock input pin	Shift register clock input pin
3	VDD	Power supply pin	Normally +5V
4	GND	Ground pin	Normally 0V
5	SIG	Video signal output pin	Picture image analog signal output pin
6	N.C.	—	—
7	SO	Start output pin	Shift register data output pin

■ Circuit diagram

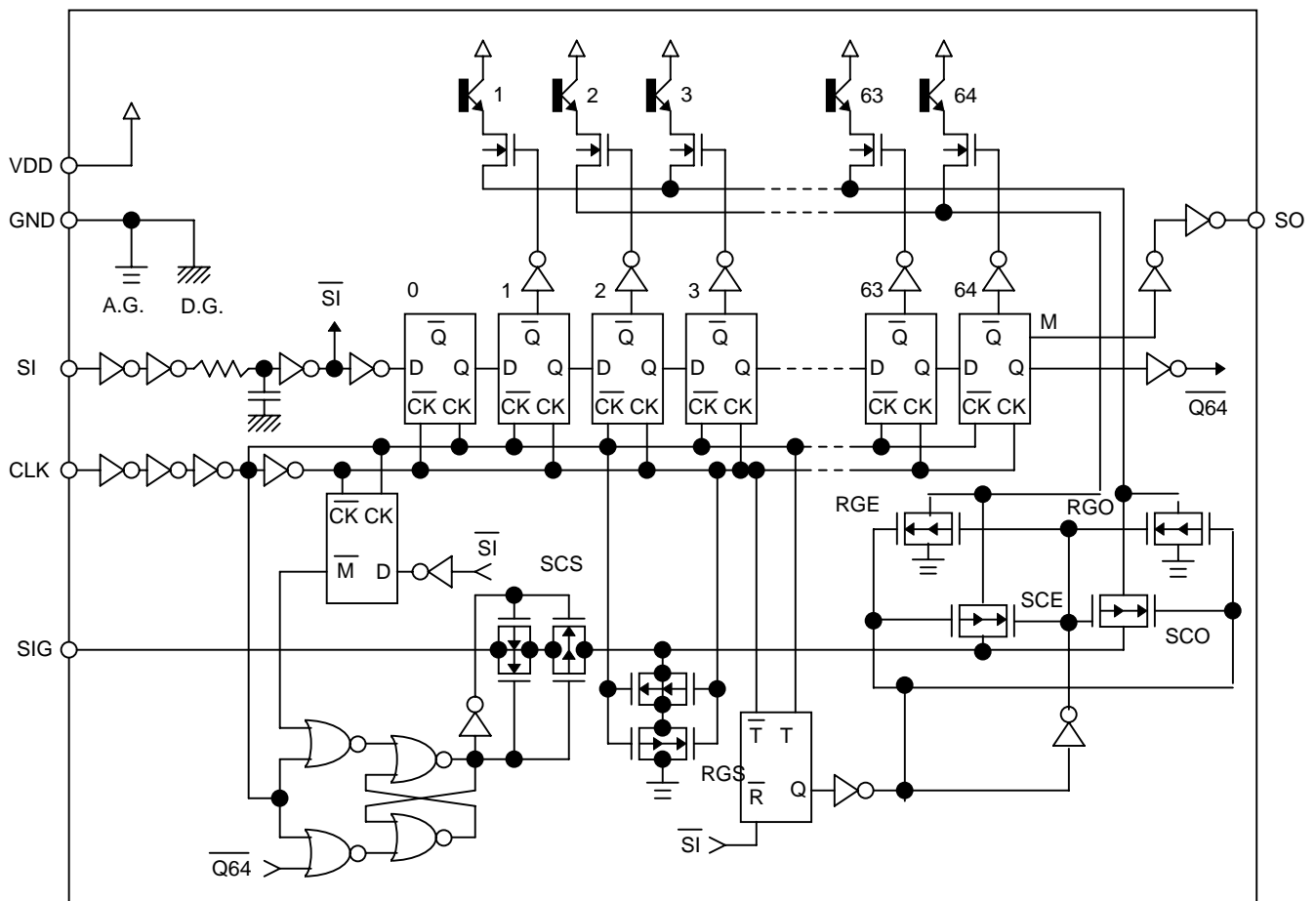


Figure-1

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■ Timing chart

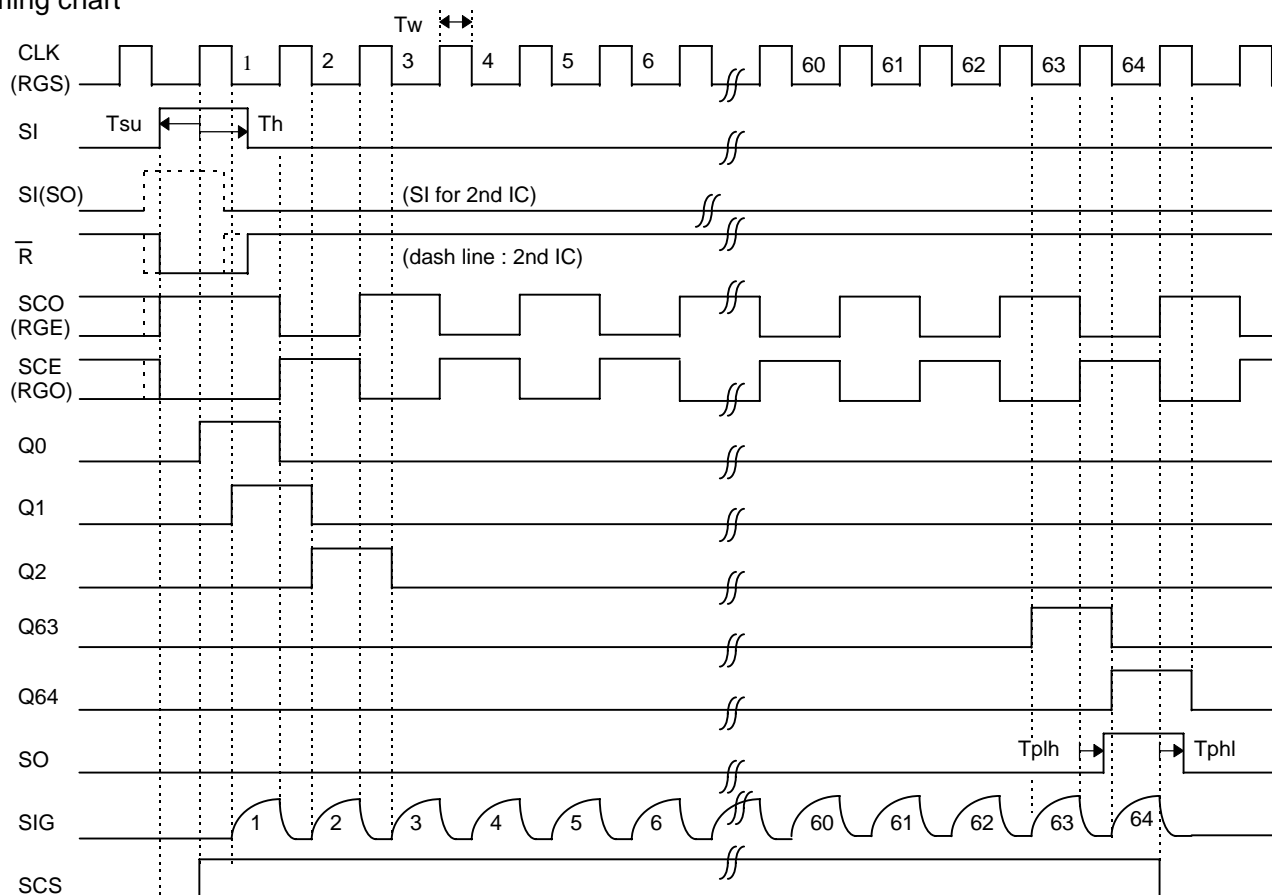


Figure-2

■ Absolute maximum ratings

Table-2

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	VDD	VDD-GND	-0.4 ~ +7.0	V
Input voltage	VIN	SI, CLK	-0.4 ~ VDD+0.4	V
Output voltage	VOU	SO, SIG	-0.4 ~ VDD+0.4	V
Operating temperature	TOPR	—	-5 ~ +85	°C
Storage temperature	TSTR	—	-40 ~ +125	°C

■ Electric characteristics

1) DC characteristics

Table-3

VDD=5V±10%, TOPR=typ.55°C

Parameter	Symbol	Condition	Rating			Unit
			min.	typ.	max.	
Input voltage	V _{IH}	SI, CLK	2.4	—	—	V
	V _{IL}		—	—	0.8	
Input current	I _{IH}	SI, CLK	—	—	0.5	μA
	I _{IL}		-0.5	—	—	
Output voltage	V _{OH}	I _{OH} = -100μA	3.8	—	—	V
	V _{OL}	I _{OL} = 100μA	—	—	0.4	
Current consumption	I _{DD}	f _{clk} = 1 MHz	—	0.2	3.0	mA
Leak current	I _s	VDD-GND	—	—	0.2	μA

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2) Switching characteristics

Parameter	Symbol	Condition	Rating			Unit	A *1)	B *2)
			min.	typ.	max.			
Clock pulse width	T_w	High period of CLK	100	—	$(1/f_{ck})$ -100	nsec	○	
Data set up time	T_{su}		100	—	$1/f_{ck}$	nsec	○	
Data hold time	T_h		0	—	$(1/f_{ck})$ -200	nsec	○	
Clock frequency	f_{ck}	Assurance of shift-register operation	—	—	2.5	MHz	○	
CLK-SO L-H delay time	T_{plh}	$f_{ck} = 2.5\text{MHz}$ $CL = 10\text{pF}$	—	—	150	nsec	○	
CLK-SO H-L delay time	T_{phl}	$f_{ck} = 2.5\text{MHz}$ $CL = 10\text{pF}$	—	—	150	nsec	○	
Output stable time 1 *3)	T_{pd1}		—	—	900	nsec		○
Output stable time 2 *3)	T_{pd2}		—	—	300	nsec		○

*1) All products are tested.

*2) Extracted products are examined.

*3) At measuring light level of photoelectric conversion characteristics.

(Note)

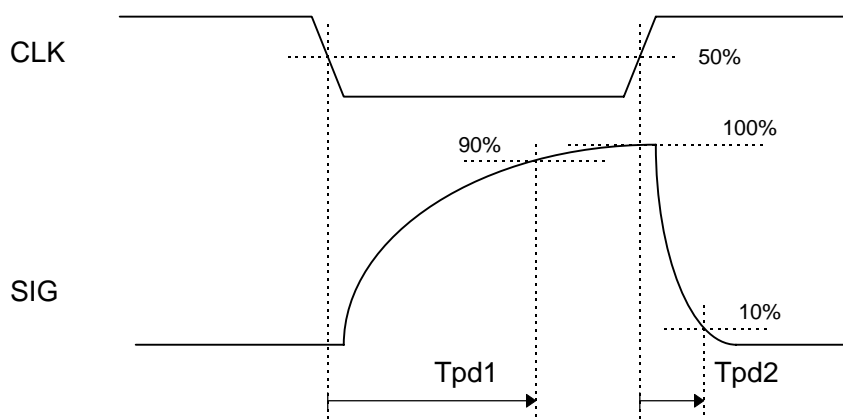


Figure-3

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3) Photoelectric conversion characteristics

Condition : $V_{DD}=5V$, $T_{OPR}=55^{\circ}C$, $f_{ck}=500\text{ kHz}$ (duty=50%)
 Read period $RT=5\text{ msec}$, load capacitor $CL=100\text{pF}$
 Light source LED
 ($\lambda =570\text{ nm}$, half width $\Delta\lambda \cong 30\text{nm}$, illuminance 12 lx)
 Connecting a capacitor of $0.1\mu\text{F}$ between V_{DD} and GND .
 V_p is measured using the measurement circuit of Figure-4.

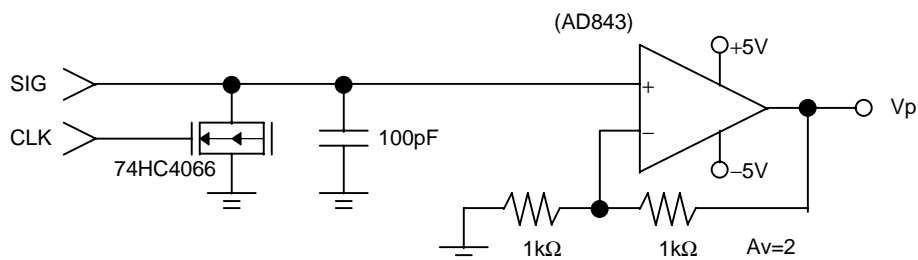


Figure-4 Measurement circuit

Table-5

Parameter	Symol	Condition	Rating			Unit	Note	A *1)	B *2)
			min.	typ.	max.				
Light level	V_{pave}	Exposure value $E_p = 0.06\text{lx}\cdot\text{sec}$	0.570	—	1.268	V	3)-2	○	
Light level deviation	dV1	Read period	-6.0	—	+6.0	%	3)-1	○	
	dV2	$RT = 5\text{ msec}$	-6.0	—	+6.0	%		○	
	dV3		0.0	—	+7.5	%		○	
	dV4	“, $i = 2 \sim 62$	-7.0	—	+7.0	%		○	
		“, $i = 1, 64$	-15.0	—	+15.0	%		○	
dV1 +dV2	$RT = 5\text{ msec}$	-10.0	—	+10.0	%	○			
Dark level 1	V_{d1}	$RT = 5\text{ msec}$ $f_{ck} = 500\text{ kHz}$	—	24	60	mV		○	
Dark level 2	V_{d2}	$RT = 32\text{ msec}$ $f_{ck} = 2\text{ kHz}$	—	—	240	mV		○	
Dark level deviation inside the wafer *4)	$\Delta\text{ dark}$	$RT = 5\text{ msec}$ $f_{ck} = 500\text{ kHz}$	0	—	9	mV		○	
Linearity	γ		0.95	1.1	1.2		3)-3		○
Image lag	R_{IL}	measuring V_{pave}	—	—	40	%	3)-1	○	
Light response	R_{IR}	measuring V_{pave}	35	—	—	%	3)-1	○	

*1) All products are tested.

*2) Extracted products are examined.

*4) The deviation of the average value of V_{d1} (1~64bit) inside a wafer.

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3)-1 Parameter definition

- V_{pave} : average of all bit output
- $V_{p\ max}$: maximum output
- V_{ave1} : average of 2 ~ 10bit
- $V_{p\ min}$: Fminimum output
- V_{ave2} : average of 28 ~ 36bit
- $V_{p(i)}$: i bit output (i =1~63)
- V_{ave3} : average of 55 ~ 63bit
- $\Delta V1 = V_{ave2} - V_{ave1}$
- $\Delta V2 = V_{ave3} - V_{ave2}$
- $dV1 = \frac{\Delta V1}{V_{pave}} \times 100$ (%)
- $dV2 = \frac{\Delta V2}{V_{pave}} \times 100$
- $dV3 = \frac{V_{p\ max} - V_{p\ min}}{V_{p\ max} + V_{p\ min}} \times 100$
- $dV4 = \frac{V_{p(i)} - V_{p(i+1)}}{V_{pave}} \times 100$
- $dV1 + dV2 = \frac{V_{ave3} - V_{ave1}}{V_{pave}} \times 100$
- RIL : Image lag (cf. Figure-5)
- RIR : Light response (cf. Figure-5)

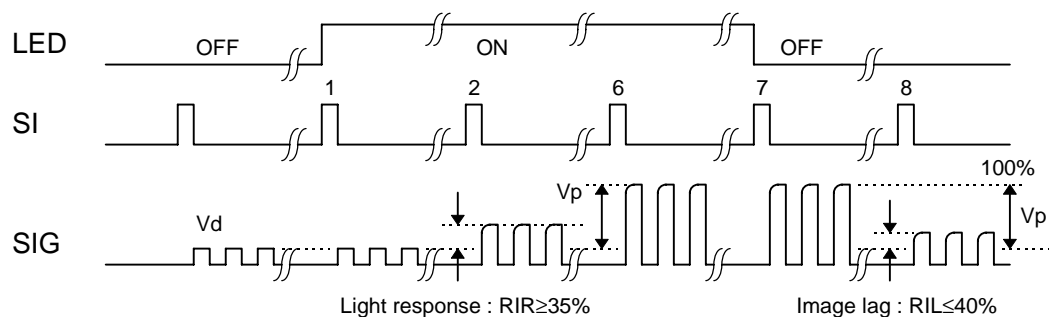


Figure-5

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3)-2 Light level ranking

RANK	$V_{pave}(V)$			RANK	$V_{pave}(V)$		
	min.(\leq)	typ.	max.($<$)		min.(\leq)	typ.	max.($<$)
0	0.570	0.584	0.599	8	0.850	0.872	0.893
1	0.599	0.614	0.630	9	0.893	0.916	0.939
2	0.630	0.646	0.662	A	0.939	0.963	0.987
3	0.662	0.679	0.696	B	0.987	1.013	1.038
4	0.696	0.714	0.731	C	1.038	1.065	1.091
5	0.731	0.750	0.769	D	1.091	1.119	1.147
6	0.769	0.789	0.808	E	1.147	1.177	1.206
7	0.808	0.829	0.850	F	1.206	1.237	1.268

3)-3 Linearity

γ value is achieved using the non-linear regression based on the following equation, measuring V_p every 0.01 $Lx \cdot sec$ from dark status to 0.06 $Lx \cdot sec$.

$$V_{pave} = A + B \cdot E_p^\gamma \quad (A, B: \text{constant}, E_p: \text{exposure value})$$

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■ Pad configuration

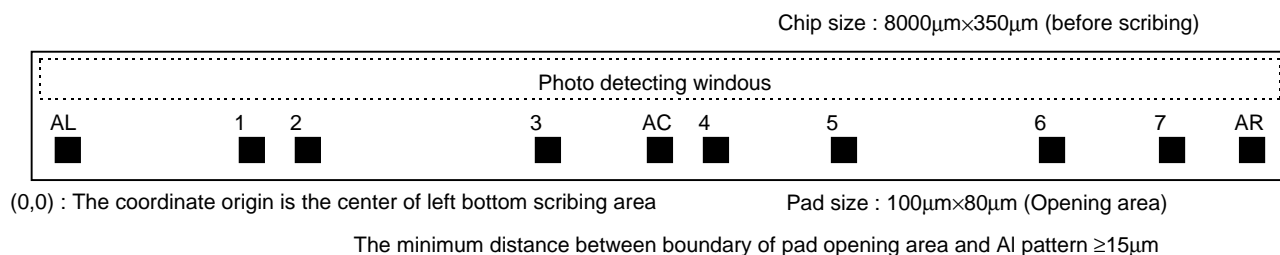


Figure-6

Table-7

Unit : μ m

PAD No.	Name	Coordinate		PAD No.	Name	Coordinate	
		X	Y			X	Y
1	SI	1431	102	5	SIG	4870	102
2	CK	1832	102	6	N.C.	6223	102
3	VDD	3182	102	7	SO	7021	102
4	GND	4245	102				

Table-8 Unit: μ m

Alignment mark name	Coordinate	
	X	Y
AL	240	102
AC	4000	102
AR	7790	102

Note : The coordinate value is the center coordinate of the pad and the alignment mark .

■ Chip size and sensor arrangement diagram

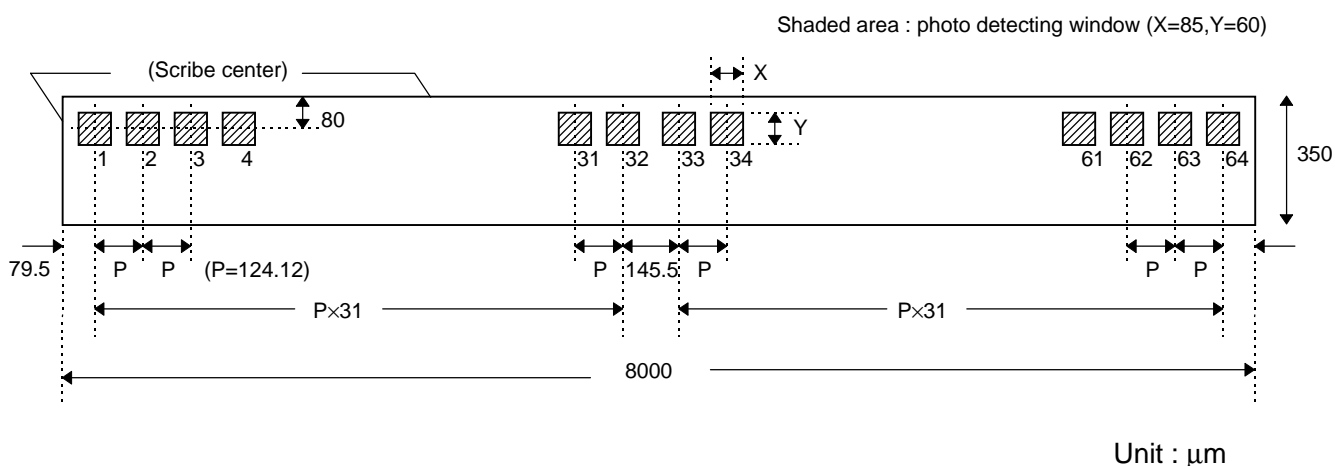


Figure-7

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■ Wafer form

Note: The arrangement of IC is subject to change without notes.

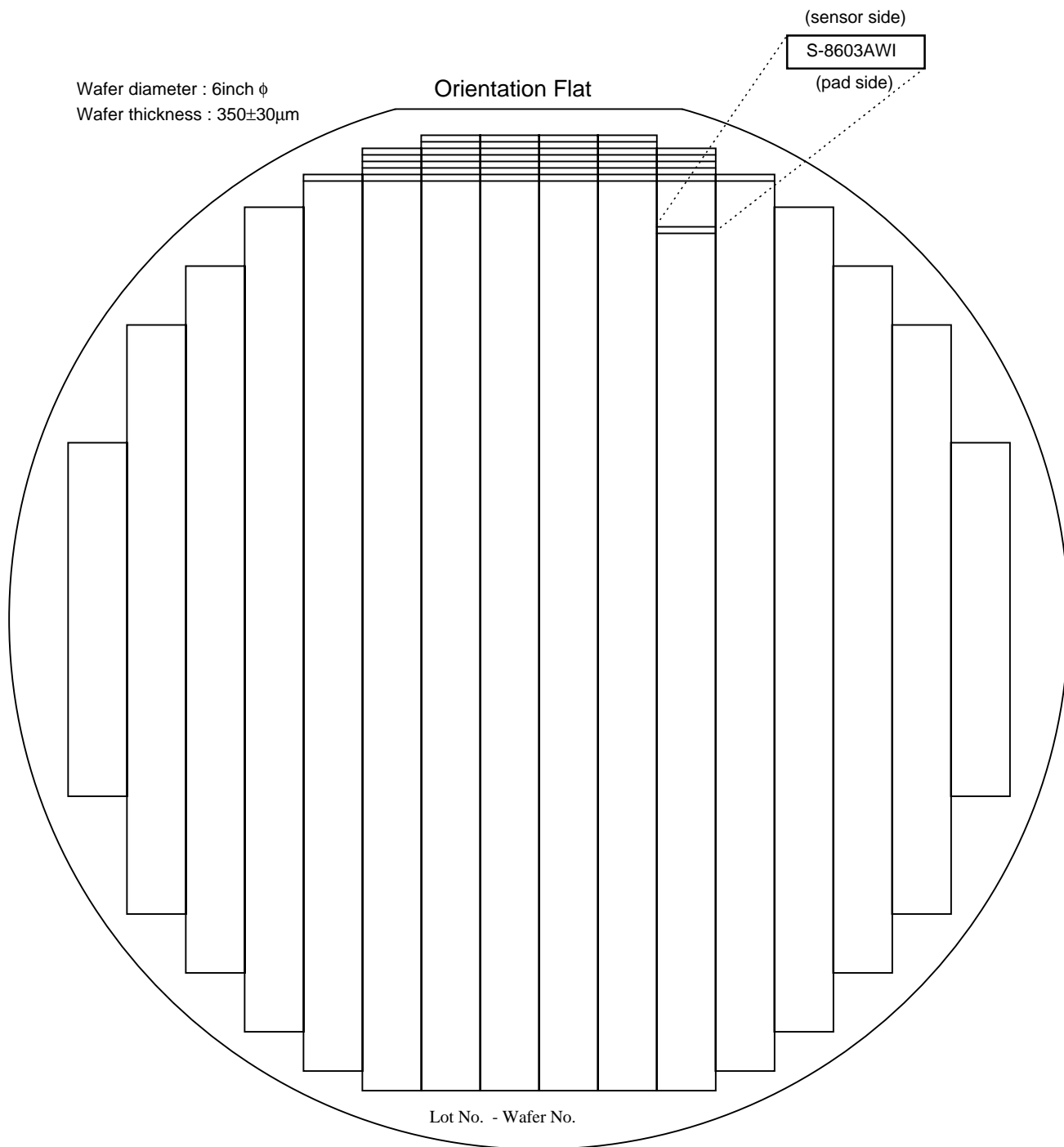
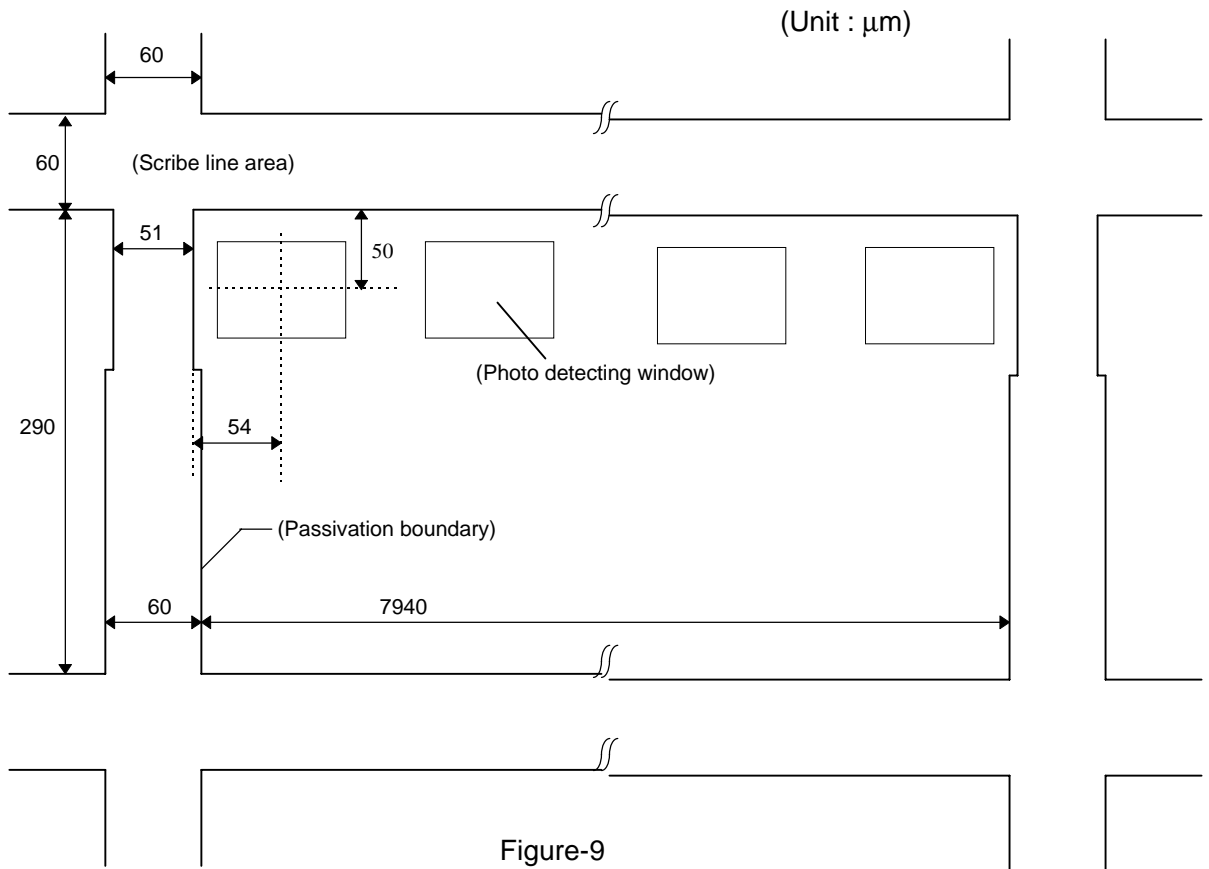


Figure-8

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■ Scribe line



■ Alignment mark

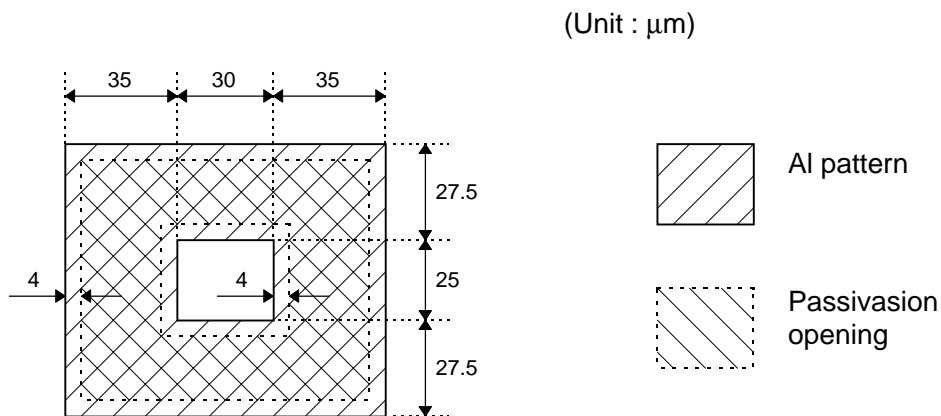


Figure-10

The minimum distance between boundary of pad opening area and Al pattern area has to be $15\mu\text{m}$ or more.