

## SERIAL NON-VOLATILE RAM

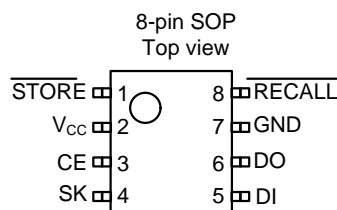
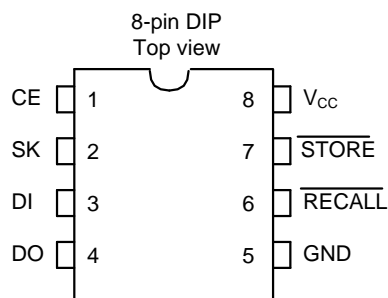
## S-24 Series

The S-24 Series is a non-volatile CMOS RAM, composed of a CMOS static RAM and a non-volatile electrically erasable and programmable memory (E<sup>2</sup>PROM) to backup the SRAM. The organization is 16-word×16-bit (total 256 bits) for the S-24H45 and the S-24S45, and 8-word×8-bit (total 64 bits) for the S-24H30 and the S-24S30.

### ■ Features

- 256 bits
  - S-24H45 : TTL input, compatible with the X2444 of Xicor
  - S-24S45 : Schmitt input for  $\overline{\text{STORE}}$  and  $\overline{\text{RECALL}}$  pins
- 64 bits
  - S-24H30 : TTL input
  - S-24S30 : Schmitt input for  $\overline{\text{STORE}}$  and  $\overline{\text{RECALL}}$  pins
- Non-volatile functions can be controlled by software and hardware
- Erroneous store protection :  $\approx 3.5 \text{ V}$
- All inputs and outputs are compatible with TTL
  - \* Except  $\overline{\text{STORE}}$  and  $\overline{\text{RECALL}}$  pins for the S-24S Series
- +5-V single power supply (+5 V $\pm$ 10%)
- Low current consumption
  - Operating : 5 mA typ.
  - Standby : 1  $\mu\text{A}$  max.
- E<sup>2</sup>PROM store cycles : 10<sup>5</sup> times
- E<sup>2</sup>PROM data retention: 10 years
- 8-pin DIP/SOP package

### ■ Pin Assignment



CE	Chip enable
SK	Serial clock
DI	Serial data input
DO	Serial data output
$\overline{\text{RECALL}}$	Recall
$\overline{\text{STORE}}$	Store
GND	Ground
V <sub>CC</sub>	Power supply voltage (+5 V)

Figure 1

# SERIAL NON-VOLATILE RAM

## S-24 Series

### ■ Block Diagram

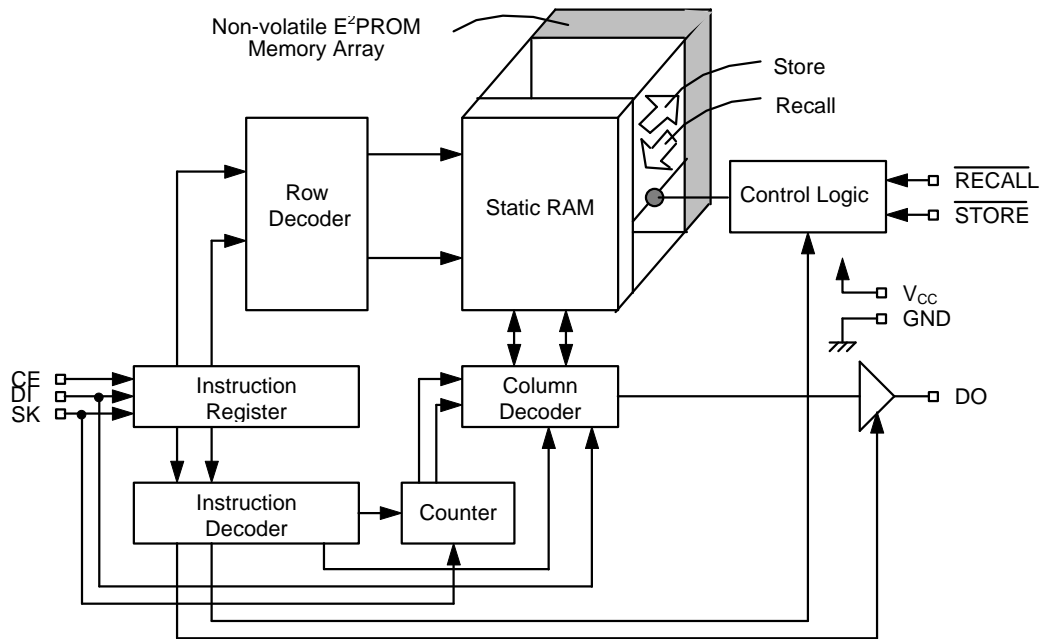


Figure 2

### ■ Absolute Maximum Ratings

Table 1

Parameter	Symbol	Ratings	Unit
Power supply voltage	$V_{CC}$	-0.3 to +6.0	V
Input voltage	$V_{IN}$	-0.3 to $V_{CC}+0.3$	V
Output voltage	$V_{OUT}$	0.0 to $V_{CC}$	V
Storage temperature under bias	$T_{bias}$	-50 to +95	°C
Storage temperature	$T_{stg}$	-65 to +150	°C

### ■ Recommended Operating Conditions

Table 2

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	$V_{CC}$		4.5	5.0	5.5	V
High level input voltage 1	$V_{IH}$	S-24H Series : All inputs S-24S Series : CE, SK and DI	2.0	—	$V_{CC}$	V
High level input voltage 2	$V_{IHS}$	S-24S Series : $\overline{STORE}$ and $\overline{RECALL}$	3.4	—	$V_{CC}$	V
Low level input voltage 1	$V_{IL}$	S-24H Series : All inputs S-24S Series : CE, SK and DI	0.0	—	0.8	V
Low level input voltage 2	$V_{ILS}$	S-24S Series : $\overline{STORE}$ and $\overline{RECALL}$	0.0	—	0.8	V
Operating temperature	$T_{opr}$		-40	—	+85	°C

### ■ Pin Capacitance

Table 3

( $T_a=25^\circ\text{C}$ ,  $f=1.0\text{ MHz}$ ,  $V_{CC}=5\text{ V}$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	$C_{IN}$	$V_{IN}=0\text{ V}$	—	—	6	pF
Output capacitance	$C_{OUT}$	$V_{OUT}=0\text{ V}$	—	—	8	pF

■ **DC Electrical Characteristics**

**Table 4**

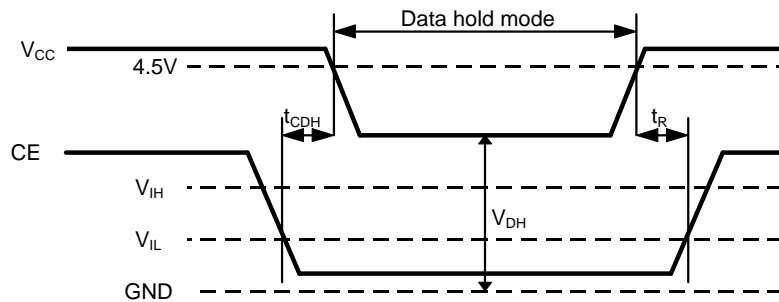
(Ta=-40°C to 85°C, V<sub>CC</sub>=+5 V±10%)

Parameter	Symbol	Conditions	Min.	Typ.	Max	Unit
Operating current consumption	I <sub>CC</sub>	DO unloaded	—	5	10	mA
Sleep current	I <sub>SL</sub>	All inputs are V <sub>CC</sub>	—	—	1	μA
Standby current	I <sub>SB</sub>	CE=GND, Other inputs are V <sub>CC</sub>	—	—	1	μA
Store current	I <sub>STO</sub>		—	5	10	mA
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =GND to V <sub>CC</sub>	—	0.1	1	μA
Output leakage current	I <sub>LO</sub>	V <sub>OUT</sub> =GND to V <sub>CC</sub>	—	0.1	1	μA
Low level output voltage	V <sub>OL</sub>	CMOS : I <sub>OL</sub> =100 μA	—	—	0.1	V
		TTL : I <sub>OL</sub> =2.1 mA	—	—	0.4	V
High level output voltage	V <sub>OH</sub>	CMOS : I <sub>OH</sub> =-100 μA	V <sub>CC</sub> -0.1	—	—	V
		TTL : I <sub>OH</sub> =-400 μA	2.4	—	—	V
Store inhibition voltage	V <sub>WI</sub>		—	3.5	4.2	V
Schmitt width	V <sub>WD</sub>	S-24S Series : STORE and RECALL	0.4	—	—	V

■ **Data Hold Characteristics**

**Table 5**

Parameter	Symbol	Conditions	Min.	Typ.	Max	Unit
Data hold voltage	V <sub>DH</sub>	CE≤0.2V, RECALL≥V <sub>CC</sub> -0.2V	1.5	—	5.5	V
Data hold setup time	t <sub>CDH</sub>		50	—	—	ns
Recovery time	t <sub>R</sub>		300	—	—	ns



**Figure 3 Data hold timing chart**

# SERIAL NON-VOLATILE RAM

## S-24 Series

### AC Electrical Characteristics

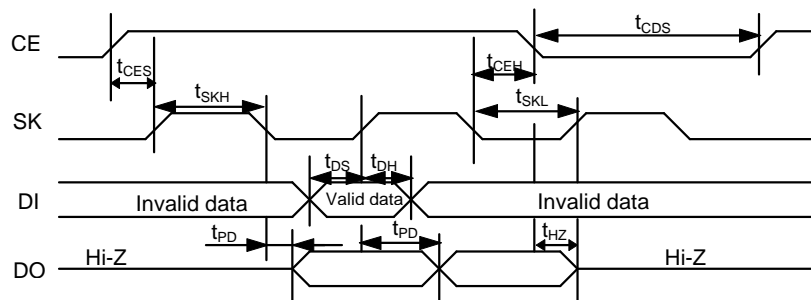
**Table 6 Measuring conditions**

Parameter	Conditions	
Input pulse voltage	S-24H Series : All inputs	0.0 to 3.0 V
	S-24S Series : <u>CE, SK and DI</u>	
	S-24S Series : <u>STORE and RECALL</u>	0.0 to 4.0 V
Input pulse rise/fall time		10 ns
I/O reference voltage		1.5 V
Output load		1TTL+100pF

#### 1. Data input/output timing

**Table 7**

Parameter	Symbol	Min.	Typ.	Max	Unit
SK frequency	$f_{SK}$	—	—	1	MHz
SK high level pulse width	$t_{SKH}$	0.4	—	—	$\mu$ s
SK low level pulse width	$t_{SKL}$	0.4	—	—	$\mu$ s
Input data setup time	$t_{DS}$	0.4	—	—	$\mu$ s
Input data hold time	$t_{DH}$	0.08	—	—	$\mu$ s
SK data valid time	$t_{PD}$	—	—	0.3	$\mu$ s
Output disable time	$t_{HZ}$	—	—	1.0	$\mu$ s
CE setup time	$t_{CES}$	0.8	—	—	$\mu$ s
CE hold time	$t_{CEH}$	0.4	—	—	$\mu$ s
CE deselect time	$t_{CDS}$	0.8	—	—	$\mu$ s



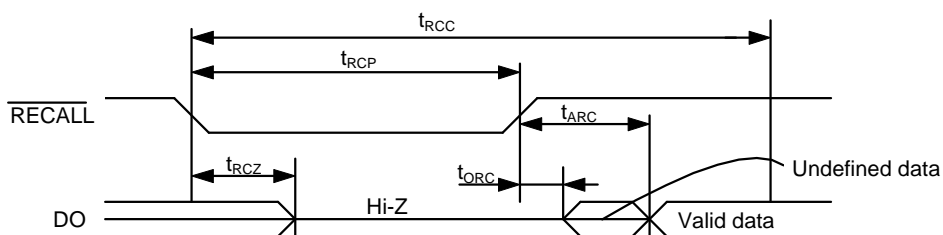
- CE must be kept high during instructions.
- When SK rises after selecting CE, the first 1 is taken into DI input and the fetch of an instruction starts. All previous 0 is ignored.

#### 2. Recall Cycle

**Figure 4 Control data timing**  
**Table 8**

Parameter	Symbol	Min.	Typ.	Max	Unit
Recall cycle time	$t_{RCC}$	2500	—	—	ns
Recall pulse width	$t_{RCP}$	500	—	—	ns
Recall disable time	$t_{RCZ}$	—	—	500	ns
Recall enable time	$t_{ORC}$	10	—	—	ns
Recall data access time	$t_{ARC}$	—	—	1000	ns

\* Recall times are not limited.



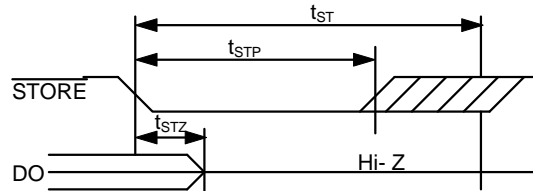
**Figure 5 Hardware recall**

3. Store Cycle

**Table 9**

Parameter	Symbol	Min.	Typ.	Max	Unit
Store time	$t_{ST}$	—	—	10	ms
Store pulse width	$t_{STP}$	0.2	—	—	$\mu$ s
Store disable time	$t_{STZ}$	—	—	1.0	$\mu$ s

Store times:  $10^5$  times  
Data retention : 10 years



**Figure 6 Hardware store**

■ **Instruction Set**

**Table 10**

Instruction	Symbol	Format $l_2 l_1 l_0$	Function
Write enable latch reset	WRDS	1XXXX000	Reset write enable latch (Disable write and store)
Write enable latch set	WREN	1XXXX100	Set write enable latch (Enable write and store)
Read	READ	1AAAA11X	Read data from RAM address AAAA
Write	WRITE	1AAAA011	Write data into RAM address AAAA
Store	STO	1XXXX001	Store RAM data in E <sup>2</sup> PROM
Recall	RCL	1XXXX101	Recall E <sup>2</sup> PROM data into RAM
Sleep	SLEEP	1XXXX010	Enter sleep mode

X : Don't care

A : Address bit

- The format is composed of a start bit(1), address( $A_3 A_2 A_1 A_0$ ) and an instruction( $l_2 l_1 l_0$ ).
- Address  $A_0$  is "X" for the S-24H30 and the S-24S30.

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## S-24 Series

### ■ Operation

#### 1. Internal latches

The S-24 Series has two latches, one of which controls write operation of the SRAM, and both of which control permission/inhibition of store operation of the E<sup>2</sup>PROM.

##### 1.1 Previous recall latch

The previous recall latch controls permission/inhibition of store operation of E<sup>2</sup>PROM. It is reset when the power is turned on, and it inhibits store operation of the E<sup>2</sup>PROM. It is set by executing the software recall instruction or hardware recall, and it permits store operation of the E<sup>2</sup>PROM.

##### 1.2 Write enable latch

The write enable latch controls permission/inhibition of both store operation of the E<sup>2</sup>PROM and write operation of the SRAM. It is reset when the power is turned on or by executing WRDS instruction, and it inhibits both store operation of the E<sup>2</sup>PROM and write operation of the SRAM.

It is set by executing WREN instruction, and it permits both store operation of the E<sup>2</sup>PROM and write operation of the SRAM.

When store operation of the E<sup>2</sup>PROM is completed, the write enable latch is automatically reset. Therefore, in order to execute store operation again, it is necessary to execute WREN instruction and to set the write enable latch.

##### 1.3 Both the previous recall latch and the write enable latch must be set for permission of store operation.

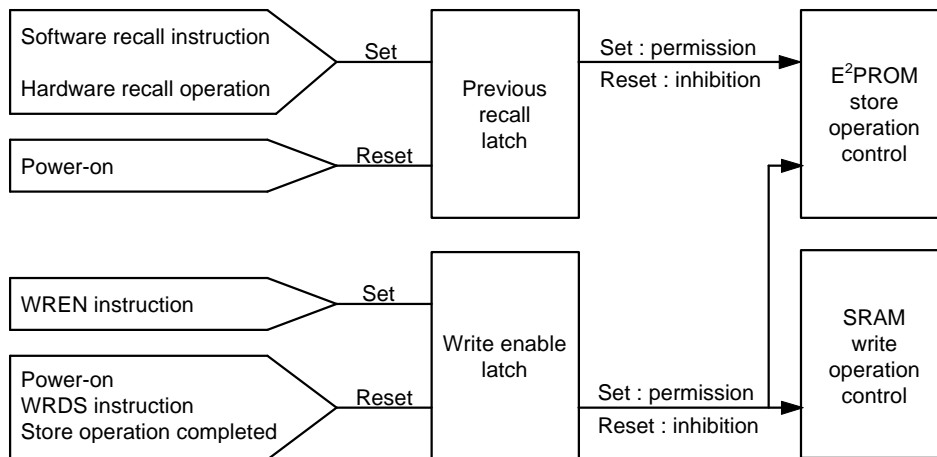


Figure 7 Internal latch

#### 2. SRAM mode

##### 2.1 Read

The data is read from the SRAM through READ instruction. Inputting a start bit, address and instruction code causes data output on DO. In the S-24 Series, a bi-directional serial interface can be made by connecting DI and DO. See Figures 8 and 9 for the timing.

##### 2.2 Write

The data is written into the SRAM through WRITE instruction. Input data on DI after a start bit, address and instruction code. See Figures 10 and 11 for the timing. The write enable latch must be set before WRITE instruction.

### 3. E<sup>2</sup>PROM mode

Data is input to and output from the E<sup>2</sup>PROM through the SRAM.

#### 3.1 Store

The SRAM data is copied into the E<sup>2</sup>PROM when STO instruction is executed or  $\overline{\text{STORE}}$  goes low. The SRAM data does not change after STO instruction. Since the data stored in the E<sup>2</sup>PROM is non-volatile, it is retained even if power is turned off. In the case that store operation is performed while data is output on DO and during read operation of the SRAM, DO becomes high-impedance. During store operation, all other operations are inhibited.

Both the previous recall latch and the write enable latch must be set before store operation.

#### 3.2 Recall

The E<sup>2</sup>PROM data is recopied into the SRAM when  $\overline{\text{RECALL}}$  goes low or RCL instruction is executed. In the case that recall operation is performed while data is output on DO and during read operation of SRAM, DO becomes high-impedance. During recall operation, all other operations are inhibited.

### 4. Sleep mode

Executing SLEEP instruction disables operation of the SRAM. The E<sup>2</sup>PROM data is retained. The sleep mode can be released by recall operation.

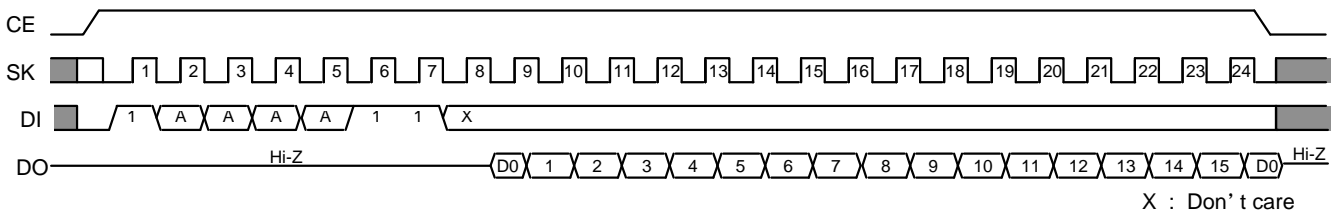
Since the S-24 Series is in standby status and the current consumption is low when CE is at GND level, it is not necessary to execute SLEEP instruction in order to reduce the current consumption while not operating.

### 5. Operation timing

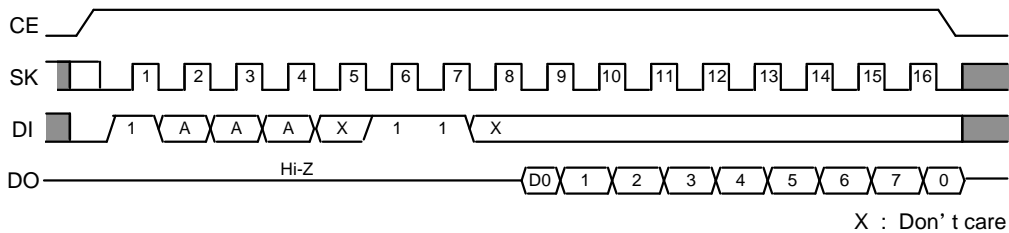
After CE rose, when SK clock rises and DI goes high, a start bit is recognized and the fetch of an instruction starts. Data is fetched to DI terminal at the rise of SK clock.

#### 5.1 Read

DO is output at the fall of the 8th clock, and others are output at the rise of the clock.



**Figure 8 Read mode timing(S-24H45, S-24S45)**



**Figure 9 Read mode timing(S-24H30, S-24S30)**

# SERIAL NON-VOLATILE RAM

## S-24 Series

### 5.2 Write

Data is written to the SRAM at the rise of SK clock.

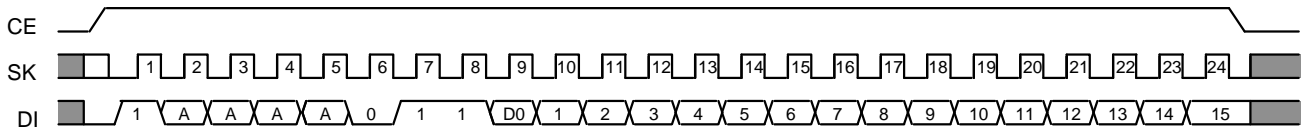


Figure 10 Write mode timing(S-24H45, S-24S45)

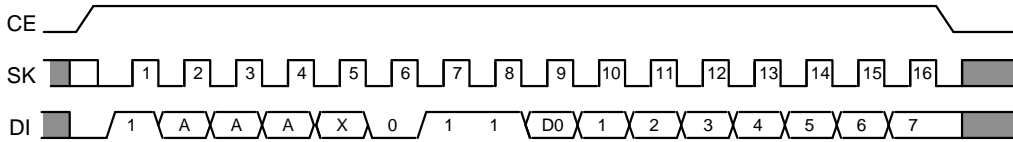


Figure 11 Write mode timing(S-24H30, S-24S30)

### 5.3 Other operation modes

CE must be low between instructions.

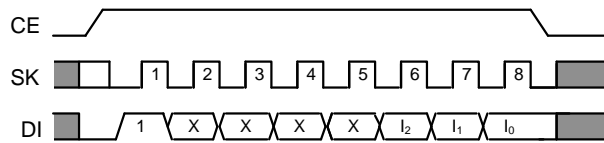


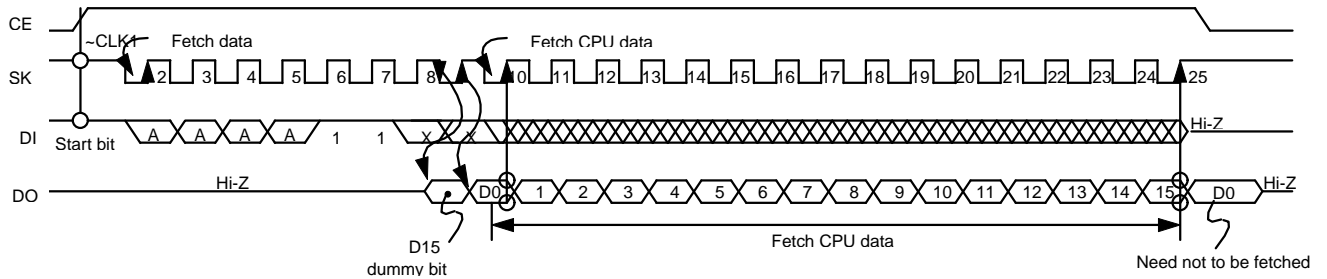
Figure 12 Other operation modes timing



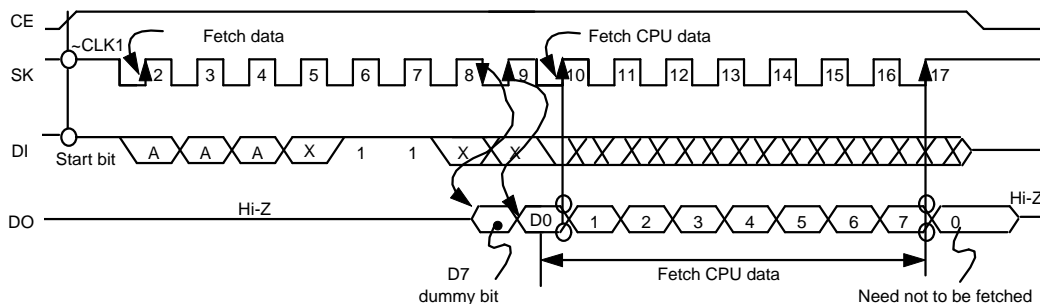
■ **Interface with CPU with Serial Port**

- When SK and DI are high at the rise of CE, high of DI is regarded as a start bit and the clock 1 generates and the high of DI is fetched. When DI is low, DI is not regarded as a start bit until DI becomes high at the rise of SK.
- After power on or after an instruction is performed, DI must be set 1 for preparing the fetch of the start bit of the next instruction.

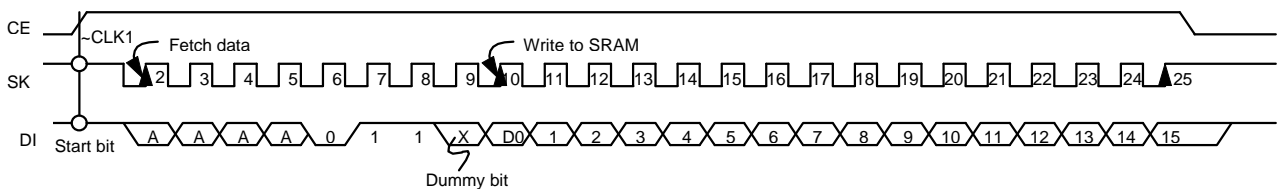
Figures 13 to 17 show the timings of write/read, and other operation modes, and interfacing examples are shown in Figures 18 to 20.



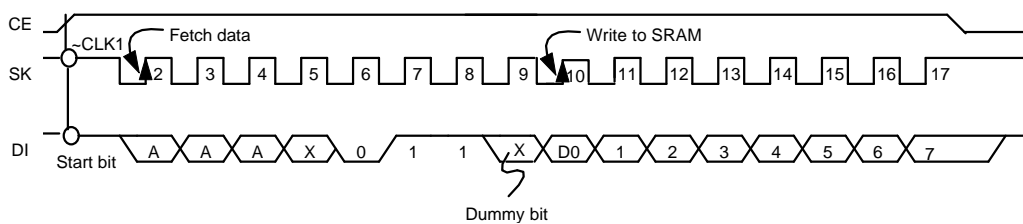
**Figure 13 Read mode timing(S-24H45, S-24S45)**



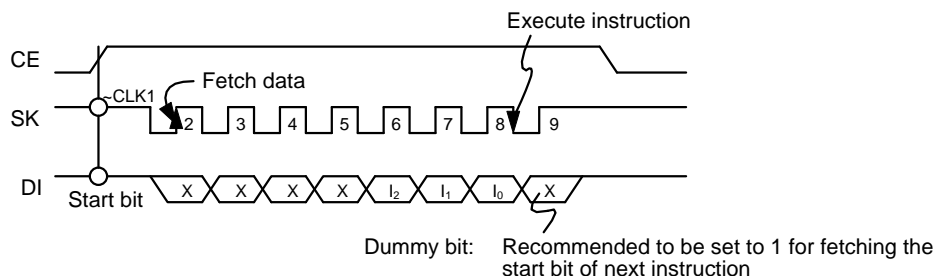
**Figure 14 Read mode timing(S-24H30, S-24S30)**



**Figure 15 Write mode timing(S-24H45, S-24S45)**



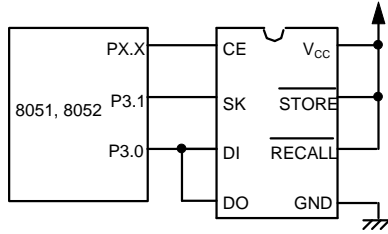
**Figure 16 Write mode timing(S-24H30, S-24S30)**



**Figure 17 Other operation mode timing**

**SERIAL NON-VOLATILE RAM**  
**S-24 Series**

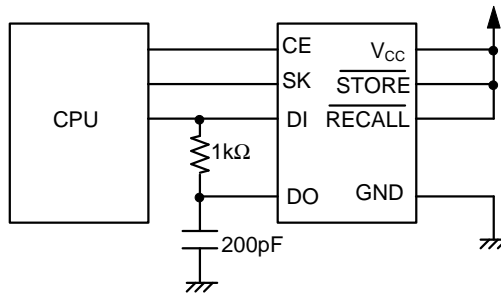
Interfacing example 1 : With Intel 8051, 8052



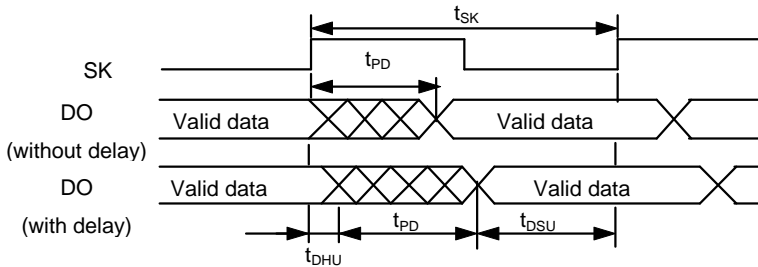
**Figure 18**

Interfacing example 2 : With other CPU

When the S-24 Series is connected to CPU other than Intel 8051 and 8052, delay circuit should be set by a capacitor and a resistor at DO terminal (Figure 19), delaying the signal more than 200 ns as in Figure 20 to assure the data hold time ( $t_{DHU}$ ) and the data setup time ( $t_{DSU}$ ) of CPU.



**Figure 19**



**Figure 20**

The maximum speed of the SK clock ( $f_{SKMAX}$ ) is expressed by the following formula:

$$f_{SKMAX} = \frac{1}{t_{SK}} = \frac{1}{t_{DSU} + t_{DHU} + t_{PD \max}}$$

For example, when interfacing with NEC  $\mu$ PD75XX series,  $f_{SKMAX}$  is as follows:

$\mu$ PD75XX series	$t_{DSU}$ : 300 ns min.
	$t_{DHU}$ : 450 ns min.
S-24 Series	$t_{PD}$ : 0 ns min. , 300 ns max.

$$f_{SKMAX} = \frac{1}{t_{SK}} = \frac{1 \times 10^9}{300 + 450 + 300} = \frac{1}{1.05 \mu s} = 952 \text{ kHz}$$



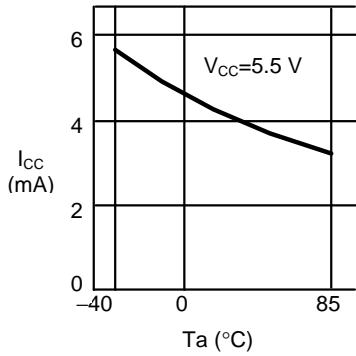
# SERIAL NON-VOLATILE RAM

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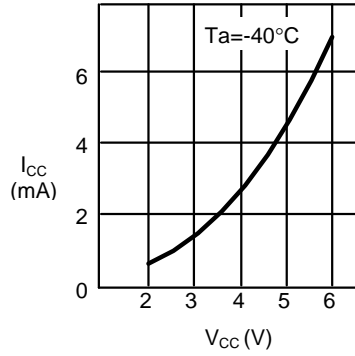
### ■ Characteristics

#### 1. DC Characteristics

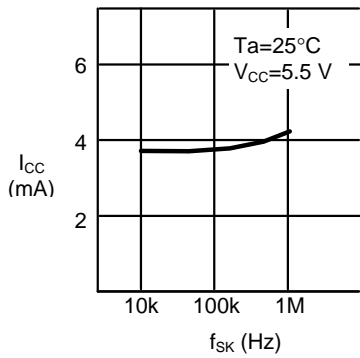
1.1 Operating current consumption  $I_{CC}$  – Ambient temperature  $T_a$



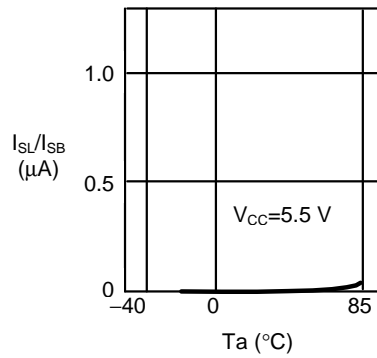
1.2 Operating current consumption  $I_{CC}$  – Power supply voltage  $V_{CC}$



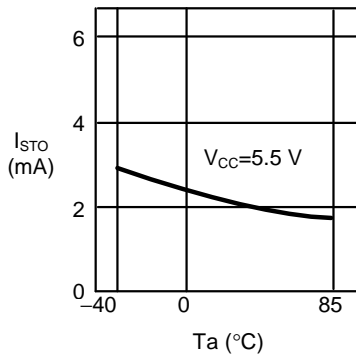
1.3 Operating current consumption  $I_{CC}$  – SK frequency  $f_{SK}$



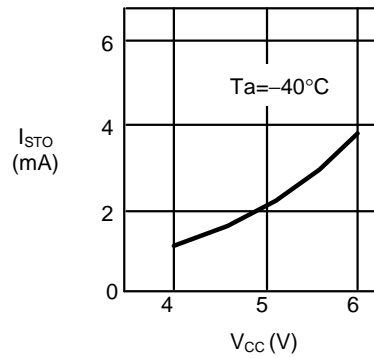
1.4 Sleep/standby current consumption  $I_{SL}/I_{SB}$  – Ambient temperature  $T_a$



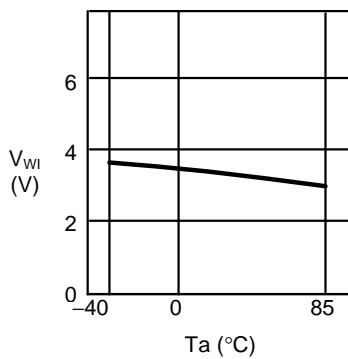
1.5 Store current consumption  $I_{STO}$  – Ambient temperature  $T_a$



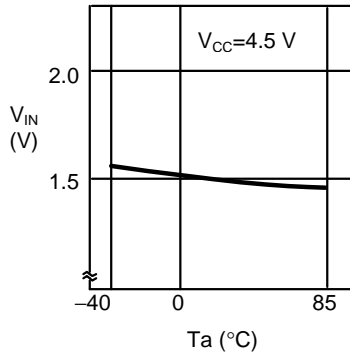
1.6 Store current consumption  $I_{STO}$  – Power supply voltage  $V_{CC}$



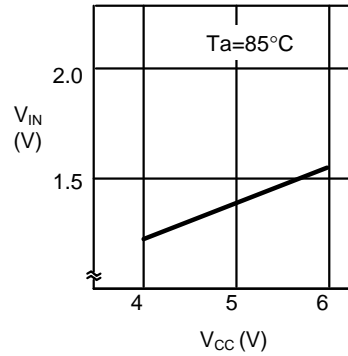
1.7 Store inhibition voltage  $V_{WI}$  – Ambient temperature  $T_a$



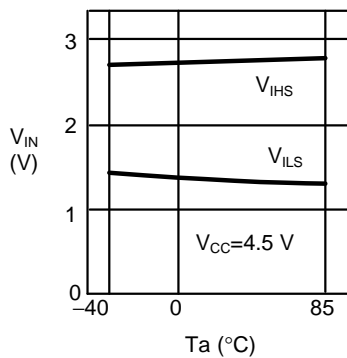
1.8 Input voltage  $V_{IN}$  – Ambient temperature  $T_a$   
S-24H Series : All inputs  
S-24S Series : CE, SK and DI



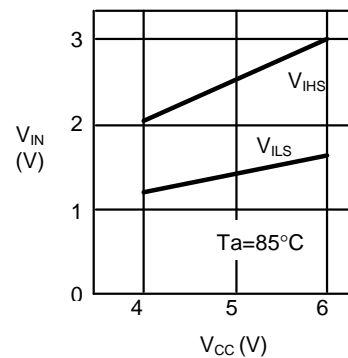
1.9 Input voltage  $V_{IN}$  – Power supply voltage  $V_{CC}$   
S-24H Series : All inputs  
S-24S Series : CE, SK and DI



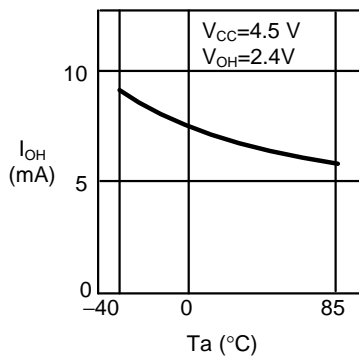
1.10 Input voltage  $V_{IN}$  – Ambient temperature  $T_a$   
S-24S Series : STORE and RECALL



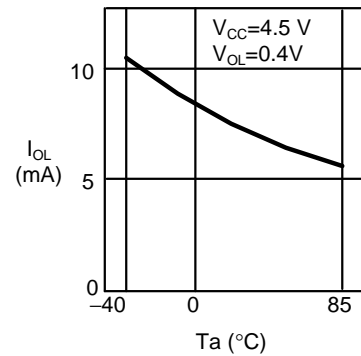
1.11 Input voltage  $V_{IN}$  – Power supply voltage  $V_{CC}$   
S-24S Series : STORE and RECALL



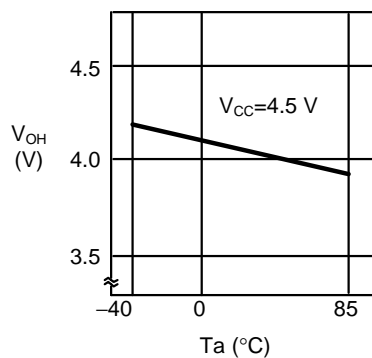
1.12 High level output current  $I_{OH}$  – Ambient temperature  $T_a$



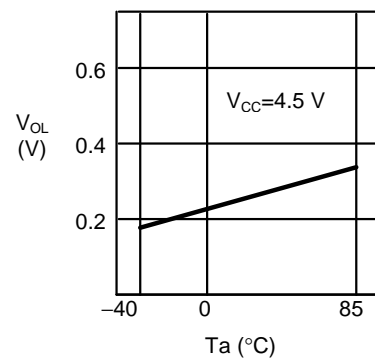
1.13 Low level output current  $I_{OL}$  – Ambient temperature  $T_a$



1.14 High level output voltage  $V_{OH}$  – Ambient temperature  $T_a$



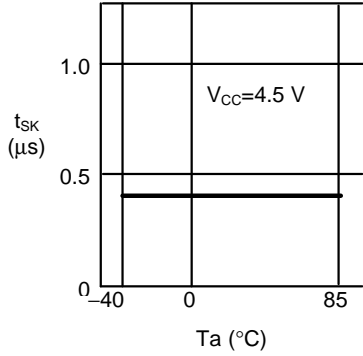
1.15 Low level output voltage  $V_{OL}$  – Ambient temperature  $T_a$



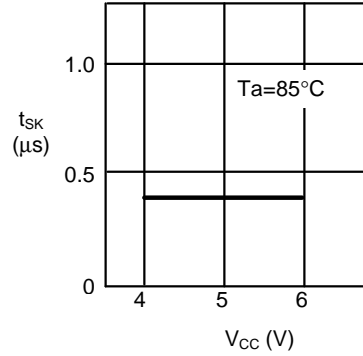
**SERIAL NON-VOLATILE RAM**  
**S-24 Series**

2. AC Characteristics

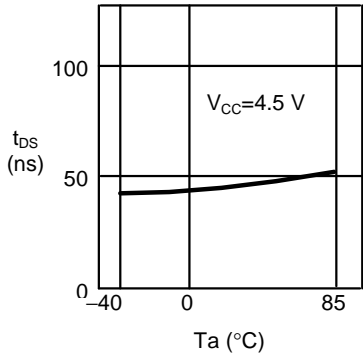
2.1 SK pulse width  $t_{SK}$  – Ambient temperature  $T_a$



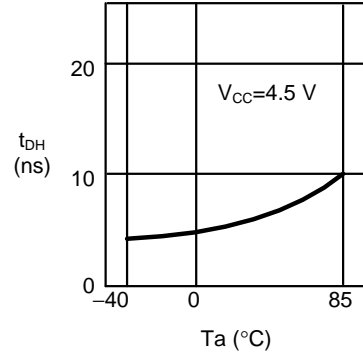
2.2 SK pulse width  $t_{SK}$  – Power supply voltage  $V_{CC}$



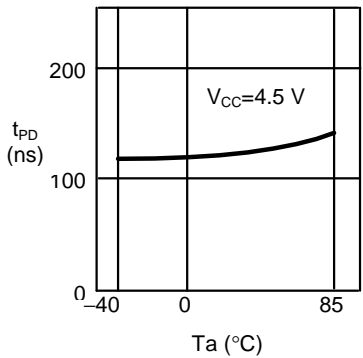
2.3 Input data setup time  $t_{DS}$  – Ambient temperature  $T_a$



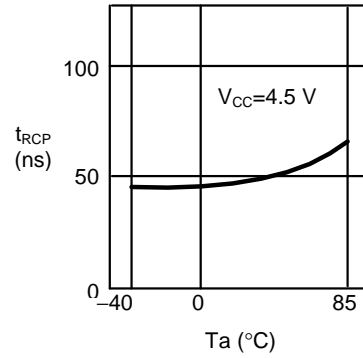
2.4 Input data hold time  $t_{DH}$  – Ambient temperature  $T_a$



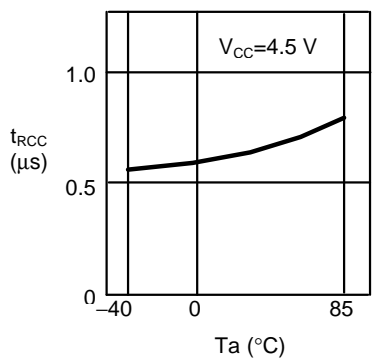
2.5 SK data valid time  $t_{PD}$  – Ambient temperature  $T_a$



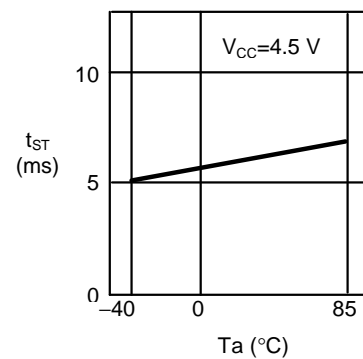
2.6 Recall pulse width  $t_{RCP}$  – Ambient temperature  $T_a$



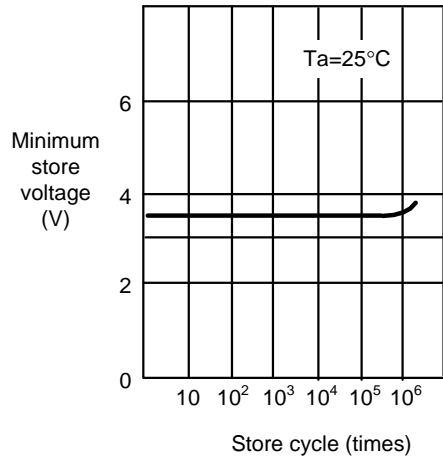
2.7 Recall cycle time  $t_{RCC}$  – Ambient temperature  $T_a$



2.8 Store time  $t_{ST}$  – Ambient temperature  $T_a$



3. Rewriting Characteristics

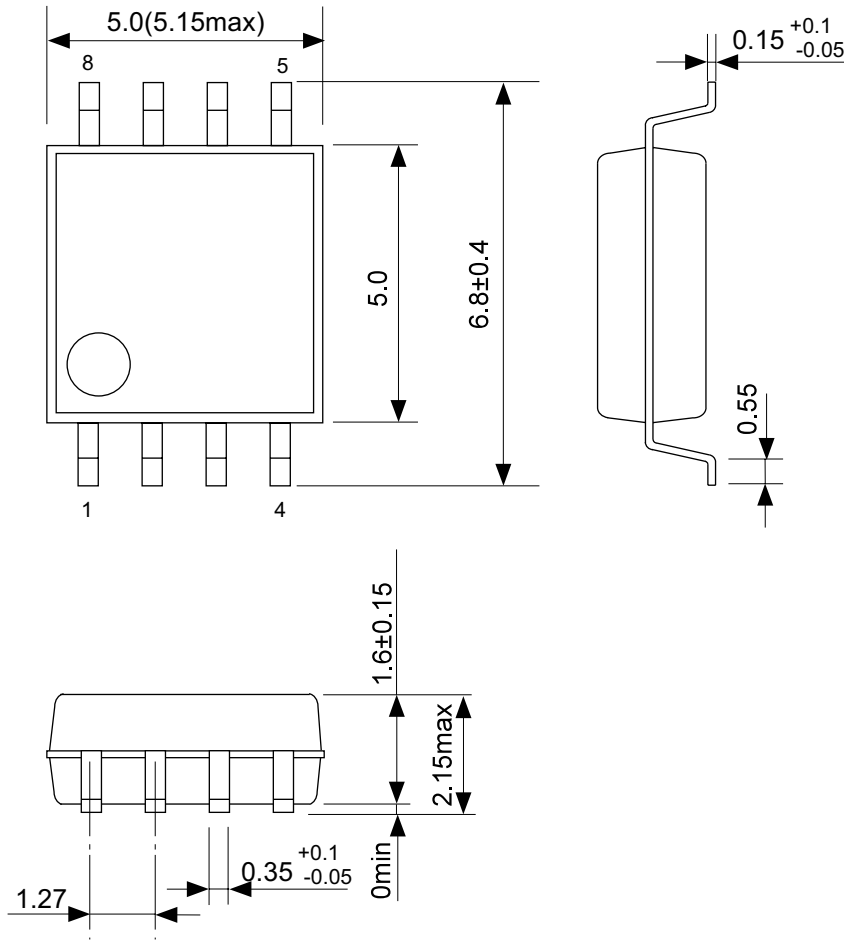


# 8-pin SOP

FE008-B 990531

## Dimensions

Unit:mm



No. : FE008-B-P-SD-1.0

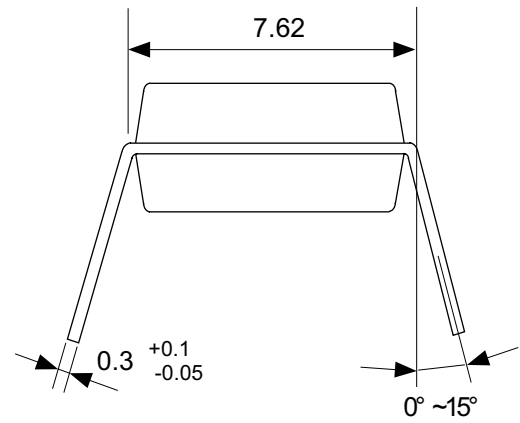
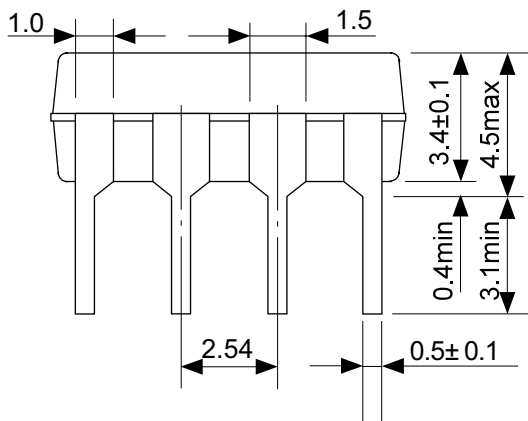
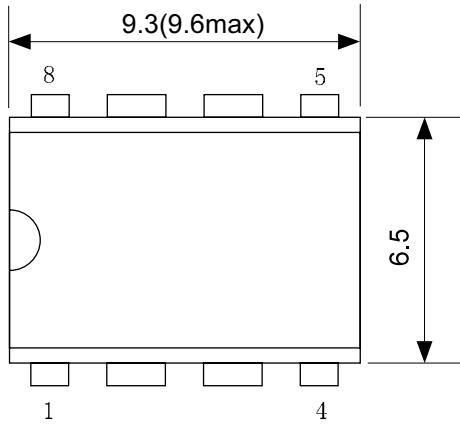


# 8-pin DIP

DP008-A 990531

## Dimensions

Unit:mm



No. : DP008-A-P-SD-1.0

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