APLUS INTEGRATED CIRCUITS INC.

APR48000

Voice Recording & Playback Device
8 Minute Duration

Features

- Multi-level analog storage
  - High quality audio recording and playback
- Dual mode storage of analog and/or digital data
  - Eliminates the need for separate digital memory
- Advanced, non-volatile Flash memory technology
  - No battery backup required
- SPI interface
  - Allows any commercial microcontroller to control the device
- Programmable Sampling Clock
  - Allows user to choose quality and duration levels
- Single 3V power supply
- Low power consumption
  - Playback operating current: 15 mA typical
  - Standby current: 1 A maximum
  - Automatic power-down
- Multiple package options available
  - CSP, TSOP, PDIP, Bare Die
- On-board clock prescaler
  - Eliminates the need for external clock dividers
- Automatic squelch circuit
  - Reduces background noise during quiet passages

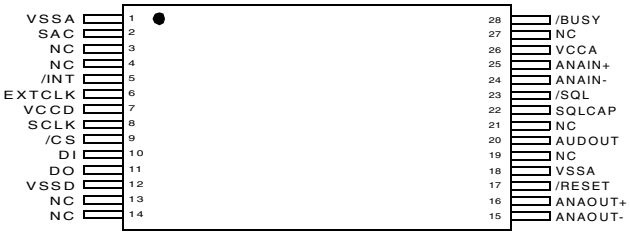
General Description

The APR48000 offers non-volatile storage of voice and/or data in advanced Multi-Level Flash memory. Up to 8 minutes of audio recording and playback can be accommodated. A maximum of 30K bits of digital data can be stored. APR48000 devices can be cascaded for longer duration recording or greater digital storage. Device control is accomplished through an industry standard SPI interface that allows a microcontroller to manage message recording and playback. This flexible arrangement allows for the widest variety of messaging options. The APR48000 is ideal for use in cellular and cordless phones, telephone answering devices, personal digital assistants, personal voice recorders, and voice pagers.

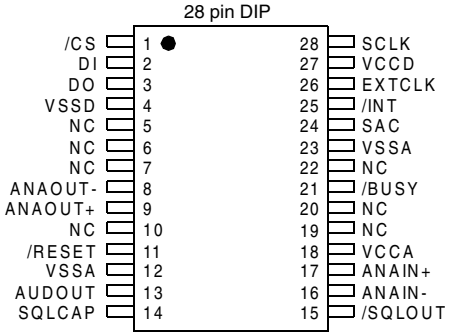
APLUS Integrated achieves this high level of storage capability by using a proprietary analog multi-level storage technology implemented in an advanced non-volatile Flash memory process. Each memory cell can typically store 256 voltage levels. This allows the APR48000 voice to reproduce audio signals in their natural form, eliminating the need for encoding and compression which can introduce distortion.

Figure 1 APR48000 Pinout Diagrams

28 pin TSOP



28 pin DIP



Functional Description

The EXTCLK pin allows the use of an external sampling clock. This input can accept a wide range of frequencies depending on the divider ratio programmed into the divider that follows the clock. Alternatively, the programmable internal oscillator can be used to supply the sampling clock. The Mux following both signals automatically selects the EXTCLK signal if a clock is present, otherwise the internal oscillator source is chosen. Detailed information on how to program the divider and internal oscillator can be found in the explanation of the *PWRUP* command, which appears in the *OpCode Command Description* section. Guidance on how to choose the appropriate sample clock frequency can be found in the *Sampling Rate & Voice Quality* section.

The audio signal containing the content you wish to record should be fed into the differential inputs ANAIN-, and ANAIN+. After pre-amplification the signal is routed into the anti-aliasing filter. The anti-aliasing filter automatically adapts its response based on the sample rate being used. No external anti-aliasing filter is therefore required.

After passing through the anti-alias filter, the signal is fed into the sample and hold circuit which works in conjunction with the Analog Write Circuit to store each analog sample in a flash memory cell.

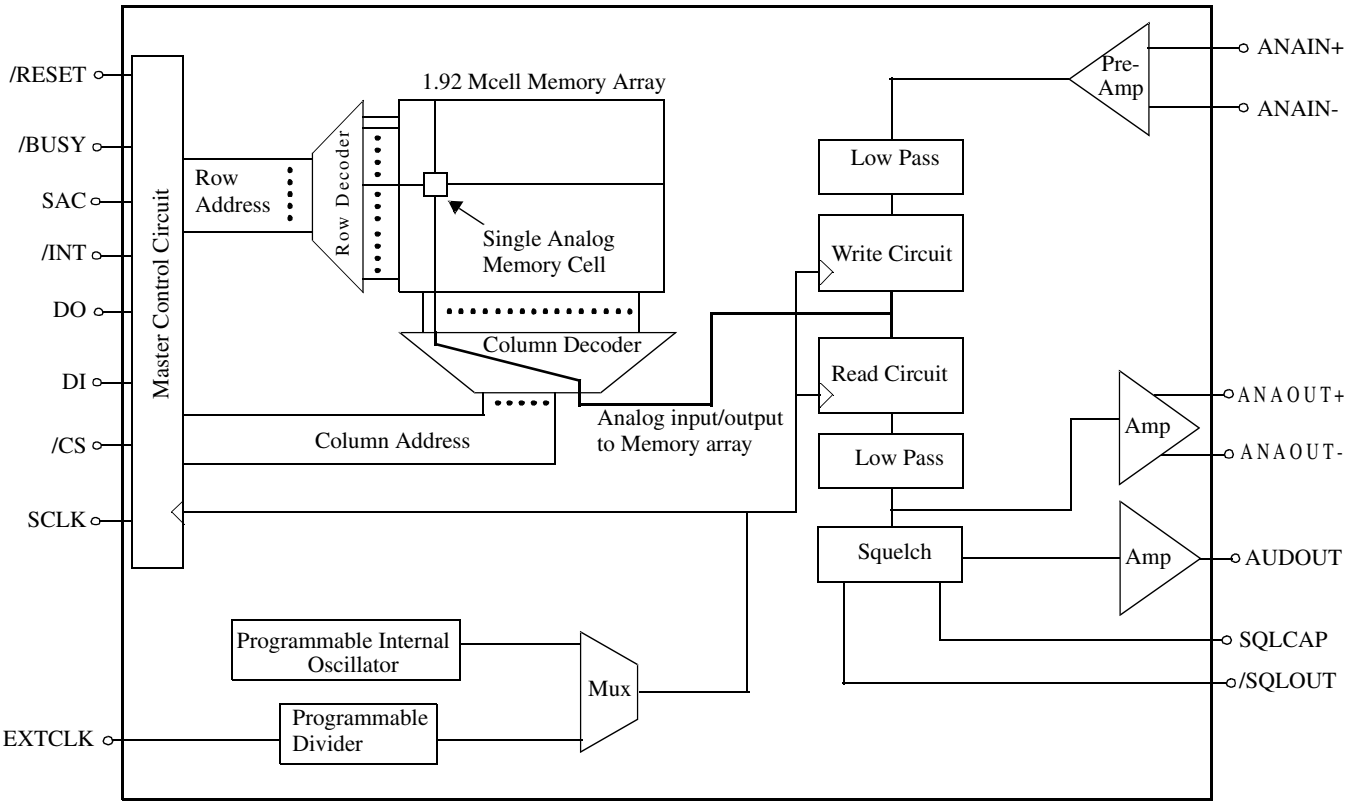
When a read operation is desired the Analog Read Circuit extracts the analog data from the memory array and feeds the signal to the Internal Low Pass Filter. The low pass filter converts the individual samples into a continuous output. The output signal then goes to the squelch control circuit and differential output driver. The differential output driver feeds the ANAOUT+ and ANAOUT- pins. Both differential output pins swing around a 1.23V potential.

The squelch control circuit automatically reduces the output signal by 6 dB during quiet passages. A copy of the squelch control signal is present on the SQLOUT pin to facilitate reducing gain in the external amplifier as well. For more information, refer to the *Squelch* section.

After passing through the squelch circuit the output signal goes to the output amplifier. The output amplifier drives a single ended output on the AUDOUT pin. The single ended output swings around a 1.23V potential.

All SPI control and hand shaking signals are routed to the Master Control Circuit. This circuit decodes all the SPI signals and generates all the internal control signals. It also contains the status register used for examining the current status of the APR48000.

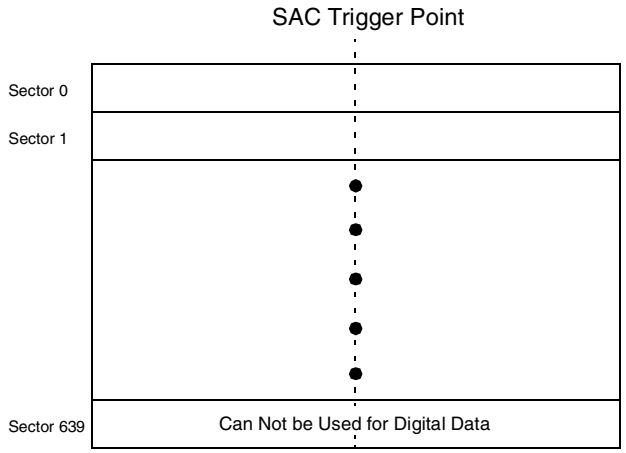
Figure 2 APR48000 Block Diagram



Memory Organization

The APR48000 memory array is organized to allow the greatest flexibility in message management and digital storage. The smallest addressable memory unit is called a “sector”. The APR48000 contains 640 sectors.

Figure 3 Memory Map.



Sectors 0 through 639 can be used for analog storage. During audio recording one memory cell is used per sample clock cycle. When recording is stopped an end of data (EOD) bit is programed into the memory. This prevents playback of silence when partial sectors are used. Unused memory that exists between the EOD bit and the end of the sector can not be used.

Sectors 0 through 9 are tested and guaranteed for digital storage. Other sectors, with the exception of sector 639, can store data but have not been tested, and are thus not guaranteed to provide 100% good bits. This can be managed with error correction or forward check-before-store methods. Once a write cycle is initiated all previously written data in the chosen sector is lost.

Mixing audio signals and digital data within the same sector is not possible.

Note: There are a total of 15bits reserved for addressing. The APR48000 only requires 10 bits. The additional 5 bits are used for larger devices within the APR48XXX family.

SPI Interface

All memory management is handled by an external host processor. The host processor communicates with the APR48000 through a simple Serial Peripheral Interface (SPI) Port. The SPI port can run on as little as three wires or as many as seven depending on the amount of control necessary. This section will describe how to manage memory using the APR48000 SPI Port and associated OpCode commands. This topic is broken down into the following sections:

- Sending Commands to the Device
  - OpCode Command Description
- Receiving Device Information
  - Current Device Status (CDS)
  - Reading the Silicon Identification (SID)
- Writing Digital Data
- Reading Digital Data
- Recording Audio Data
- Playing Back Audio Data
- Handshaking Signals

Sending Commands to the Device

This section describes the process of sending OpCodes to the APR48000 All Opcodes are sent in the same way with the exception of the *DIG_WRITE* and *DIG_READ* commands. The *DIG_WRITE and DIG_READ* commands *are* described in the *Writing Digital Data* and *Reading Digital Data* sections that follow. The minimum SPI configuration needed to send commands uses the DI, /CS, and SCLK pins. The device will accept inputs on the DI pin whenever the /CS pin is low. OpCode commands are clocked in on the rising edge of the SPI clock. Figure 4 shows the timing diagram for shifting OpCode commands into the device. Figure 5 is a description of the OpCode stream.

You must wait for a command to finish executing before sending a new command. This is accomplished by monitoring the /BUSY pin. You can substitute monitoring of the busy pin by inserting a fixed delay between commands. The required delay is specified as T_{next1},T_{next2},T_{next3} or T_{next4}. Figure 6 shows the timing diagram for sending consecutive commands. Table 1 describes which T_{next} specification to use.

Figure 4 Sending SPI Commands

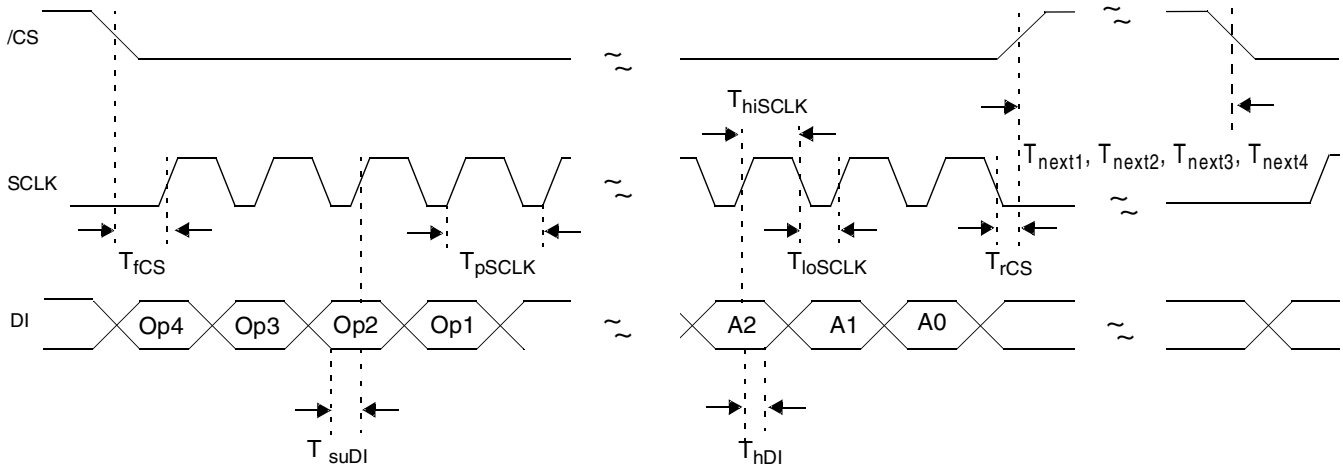


Figure 5 OpCode Format

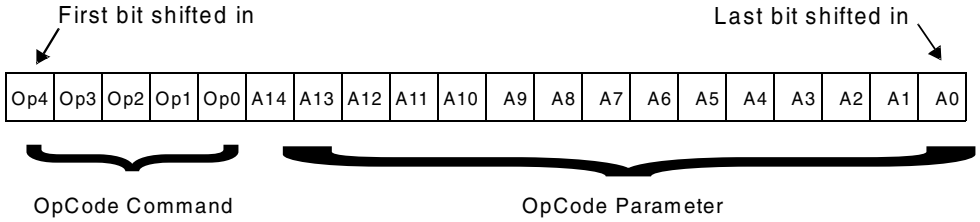


Figure 6 Opcode Stream Timing

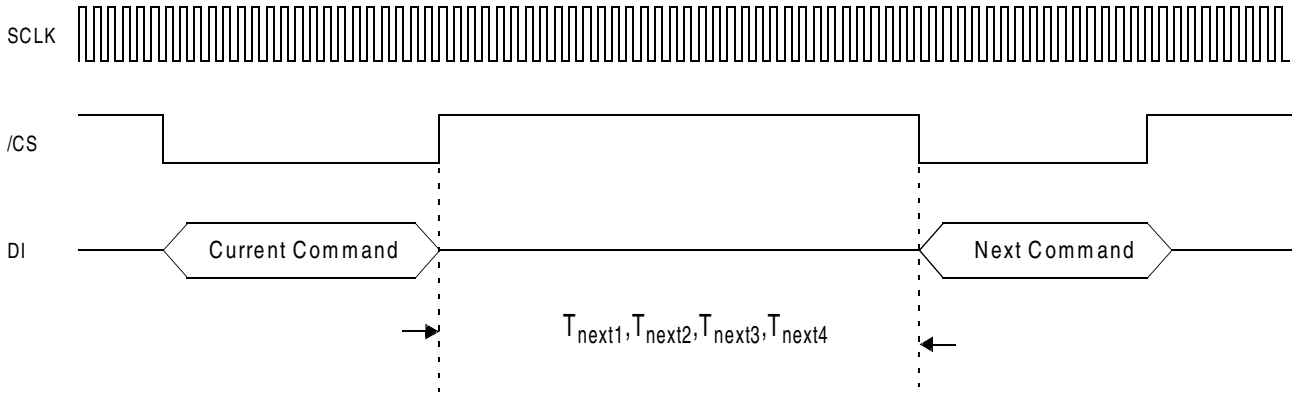


Table 1 Sequential Command Timing

Current Command	Next command	Timing Symbol
NOP *SID*	Any Command	T_{next1}
PWRUP	Any Command	T_{next2}
STOP_PWDN	*PWRUP*	T_{next2}
SET_REC *REC*	*STOP, STOP_PWDN, SET_REC, REC,NOP*	Within SAC Low Time
SET_PLAY *PLAY*	*STOP, STOP_PWDN, SET_FWD, FWD, SET_PLAY,PLAY, NOP*	
SET_FWD *FWD*	*SET_FWD, FWD, STOP, STOP_PWDN*	
DIG_WRITE *DIG_READ* *DIG_ERASE*	Any Digital Command, *STOP, STOP_PWDN* *Note: For partial DIG_READ T_{next2} is measured from the extra clock low that follows the rise of /CS, not from the rise of /CS*	T_{next3}
STOP	Any Command	T_{next4}

OpCode Command Description

Designers have access to a total of 14 OpCodes. These OpCodes are listed in Table 2. The name of the Opcode appears in the left hand column. The following two columns represent the actual binary information contained in the 20 bit data stream. Some commands have limits on which command can follow them. These limits are shown in the "*Allowable Follow on Commands*" column. The last column summarizes each command.

Combinations of OpCodes can be used to accommodate almost any memory management scheme.

Table 2 APR48000 Operational Codes

Instruction Name	OpCode (5 bits)	Opcode Parameters (15bits)	Allowable Follow on Commands	Summary
	[Op4 - Op0]	*[Address MSB - Address LSB]* *[Address 14 - Address 0]*		
NOP	[00000]	[Don't Care]	All Commands	No Operation
SID	[00001]	[Don't care]	All Commands	Causes the silicon ID to be read.
SET_FWD	[00010]	Sector Address [A14 - A0]	SET_FWD, FWD, STOP, STOP_PWDN	Starts a fast forward operation from the sector address specified.
FWD	[00011]	[Don't care]	SET_FWD, FWD, STOP, STOP_PWDN	Starts a fast forward operation from the current sector address.
PWRUP	[00100]	[A14-A10]: all zeros [A9-A2]: EXTCLK divider ratio [A1-A0]: Sample Rate Frequency	All Commands	Resets the device to initial conditions. Sets the sample frequency and divider ratios.
STOP	[00110]	[Don't care]	All Commands	Stops the current operation.
STOP_PWDN	[00111]	[Don't care]	PWRUP	Stops the current operation. Causes the device to enter power down mode.

Instruction Name	OpCode (5 bits)	Opcode Parameters (15bits)	Allowable Follow on Commands	Summary
	[Op4 - Op0]	*[Address MSB - Address LSB] [Address 14 - Address 0]*		
SET_REC	[01000]	Sector Address [A14 - A0]	STOP, STOP_PWDN, SET_REC, REC,NOP	Starts a record operation from the sector address specified.
REC	[01001]	[Don't care]	STOP, STOP_PWDN, SET_REC, REC,NOP	Starts a record operation from the current sector address.
DIG_ERASE	[01010]	Sector Address [A14 - A0]	All Commands	Erases all data contained in specified sector. You must not erase a sector before recording voice signals into it. You must erase a sector before storing digital data in it.
DIG_WRITE	[01011]	[A14 - A0][XXXX][D0 - D3004][XXXX]	All Commands	This command writes data bits D0 - D3003 starting at the specified address. All 3004 bits must be written.
DIG_READ	[01111]	Sector Address [A14 - A0]	All Commands	This command reads data bits D0 - D3003 starting at the specified address.
SET_PLAY	[01100]	Sector Address [A14 - A0]	STOP, STOP_PWDN, SET_FWD, FWD, SET_PLAY,PLAY, NOP	Starts a play operation from the sector address specified.
PLAY	[01101]	[Don't care]	STOP, STOP_PWDN, SET_FWD, FWD, SET_PLAY,PLAY, NOP	Starts a play operation from the current sector address.

The ***NOP*** command performs no operation in the device. It is most often used when reading the current device status. For more information on reading device status see the *Current Device Status* section.

THE ***SID*** operation instructs the device to return the contents of its silicon ID register. For more information see the *Reading the SID* section.

The ***SET_FWD*** command instructs the device to fast forward from the beginning of the sector specified in the OpCode parameter field. The device will fast forward until either an EOD bit, or the end of the sector is reached. If no EOD bit or forthcoming command has been received when the end of the sector is reached, the device will loop back to the beginning of the same sector and begin the same process again. If an EOD bit is found the device will stop and generate an interrupt on the /INT pin. The output amplifiers are muted during this operation.

The ***FWD*** command instructs the device to fast forward from the start of the current sector to the next EOD marker. If no EOD marker is found within the current sector the device will increment to the next sequential sector and continue looking. The device will continue to fast forward in this manner until either an EOD is reached, a new command is sent, or the end of the memory array is reached. When an EOD is reached the device will stop and generate an interrupt on the /INT pin. The output amplifiers are muted during this operation.

The ***PWRUP*** command causes the device to enter power up mode and set the internal clock frequency and EXTCLK divider ratio. To select an Internal oscillator frequency set the [A1 - A0] bits according to the following binary values:

A1	A0	Sample rate
0	0	6.4 kHz
0	1	4.0 kHz
1	0	8.0 kHz
1	1	5.3 kHz

If you are using an external sample clock signal you must also set the EXTCLK divider ratio. This divider ratio is equal to N:1 where N is an integer between 1 and 256, excluding 2. The N value should be selected to satisfy the following equa-

tion as closely as possible:

EXTCLK freq = (N) * (128) * (selected sampling frequency)

Example:

Suppose that 8.0 KHz sampling is desired. Assume that the frequency of the signal present on EXTCLK = 8MHz.

$$N = \frac{8000000}{128(8000)} = 7.8125$$

Rounding up, N = 8

The Op Code Parameter bit stream, composed of bits [A9 - A2][A1 - A0], therefore becomes binary [00001000][10].

The ***STOP*** Command causes the device to stop the current operation.

The ***STOP_PWDN*** command causes the device to stop the current command and enter power down mode. During power down the device consumes significantly less power. The PWRUP command must be used to force the device into power up mode before any commands can be executed.

The ***SET_REC*** command instructs the device to begin recording at the sector address specified. The device will continue to record until the end of the current sector is reached. If no forthcoming command has been received when the end of the sector is reached the device will loop back to the beginning of the same sector and overwrite the previously recorded material. If the next command is another *SET_REC* or *REC* command the device will execute the command immediately following the end of the current sector so that no audio information is lost. For more information see the section entitled *Recording Audio Data*.

The ***REC*** command instructs the device to begin recording in the current sector. If no new command is received before the device reaches the end of the sector the device will automatically increment to the next sequential sector and continue recording. The device will continue to record in this manner until the memory is exhausted or a *STOP* or *STOP_PWDN* command is received. For more information see the section entitled *Recording Audio Data*.

The ***DIG_ERASE*** command erases all data contained in the sector specified. Erase should not be done before recording voice signals into a sector. Erase must be done before storing digital data in a sector.

The ***DIG_WRITE*** command stores 3K bits of digital data in the specified sector. All 3K bits must be written, no partial usage of the sector is possible. The memory acts as a FIFO, the first data bit shifted in will be the first data bit shifted out. A sector must be erased using the *DIG_ERASE* command **BEFORE** data can be written to the sector. For more information on storing digital data, see the section entitled *Writing Digital Data*.

The ***DIG_READ*** command instructs the device to retrieve digital data that was previously written to the specified sector. The first bit shifted out is the first bit that was written. The last bit shifted out is the last bit that was written. For more information on reading digital data see the section entitled *Reading Digital Data.*

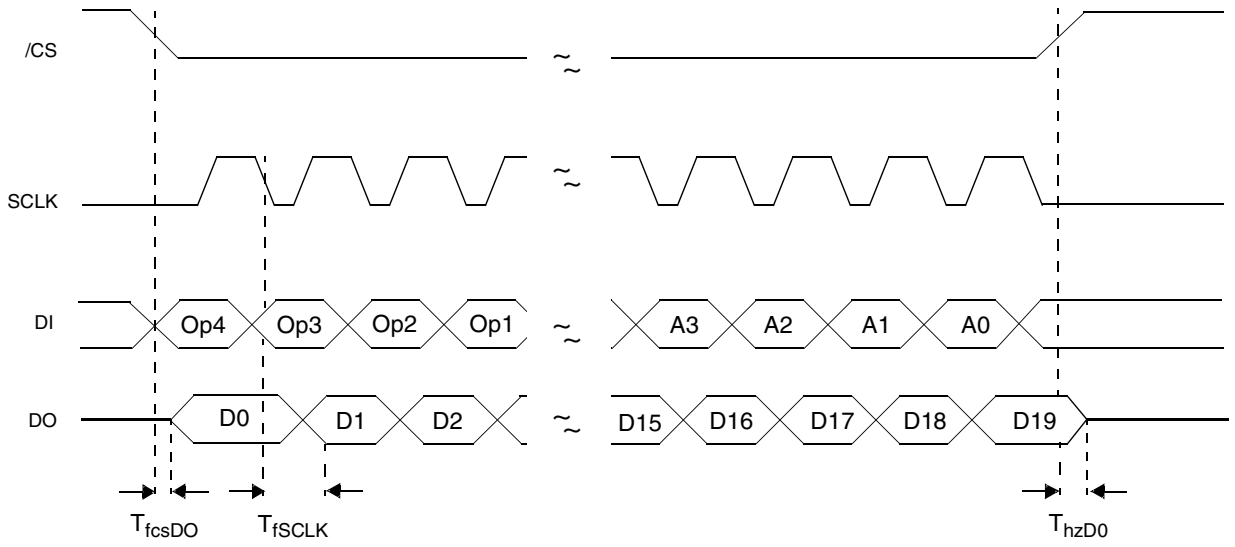
The ***SET_PLAY*** command instructs the device to begin playback at the specified sector. If no forthcoming command is received, or EOD bit encountered, before the end of the sector is reached the device will loop back to the beginning of the same sector and continue playback with no noticeable gap in the audio output. If the next command is another *SET_PLAY* or *PLAY* command the device will execute the command immediately following the end of the current sector so that no gap in playback is present. For more information see the section entitled *Playing Back Audio Data.*

The ***PLAY*** command instructs the device to begin playback at the current sector. If no forthcoming command is received, or EOD bit encountered, before the device reaches the end of the sector the device will automatically increment to the next sequential sector and continue playing. The device will continue to play in this manner until the memory is exhausted or a *STOP* or *STOP_PWDN* command is received. For more information see the section entitled *Playing Back Audio Data.*

Receiving Device Information

The device communicates data to the user by shifting out data on the DO pin. The device will shift out data according to the timing parameters given in figure 7. The device can shift out three different types of data streams: Device status, Silicon ID, and user stored data. Device status and silicon ID are described in the next two sections. Retrieval of user data is described in the *Reading Digital Data* section.

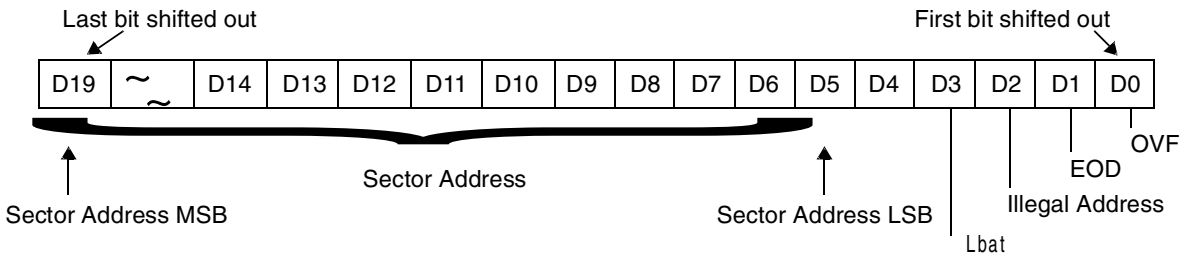
Figure 7 Data Out Timing



Current Device Status (CDS)

As described in the previous section, three different types of data streams are shifted out on the DO pin as data is shifted in on the DI pin. One of these steams is the current device status. The CDS will be shifted out unless the previous command is SID command. Figure 8 shows the format of the CDS bit stream. The first bit shifted out, D0, is the Overflow flag. The Overflow flag is set to a binary 1 if an attempt was made to record beyond the available memory. The Overflow flag is set to a 0 if an overflow has not occurred. This flag is cleared after it has been read. The D1 bit is the End of Data flag. The EOD flag is set when the device stops playing, or fast forwarding as a result of an EOD bit in memory. The EOD flag is cleared after it has been read. The D2 bit is the Illegal Address flag. The Illegal Address flag is set whenever an illegal address is sent to the device. The D3 bit is the Lbat flag. This flag is set when the device senses a supply voltage below specification. The D4 bit is not used and should be ignored. The last fifteen bits represent the address of the current or last active sector.

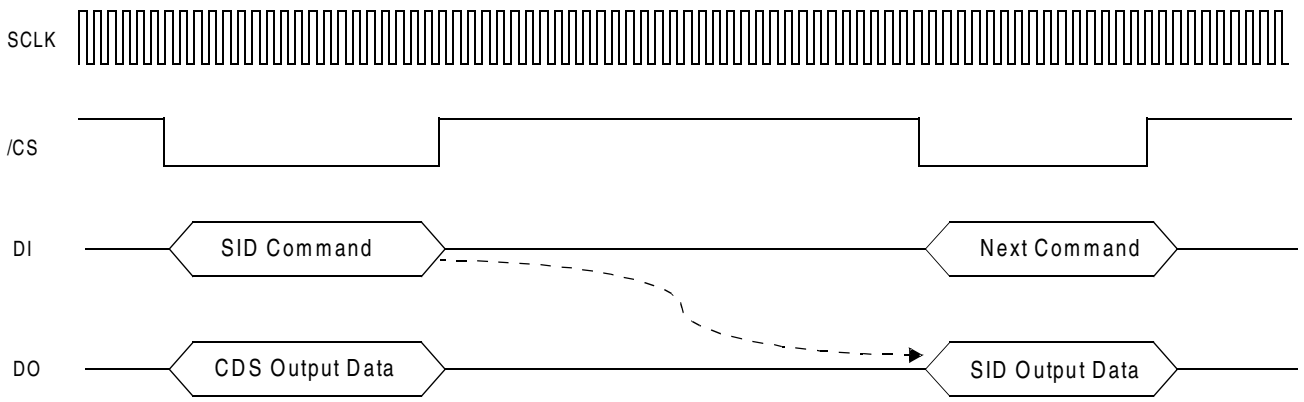
Figure 8 Format for CDS Bit Stream



Reading the SID

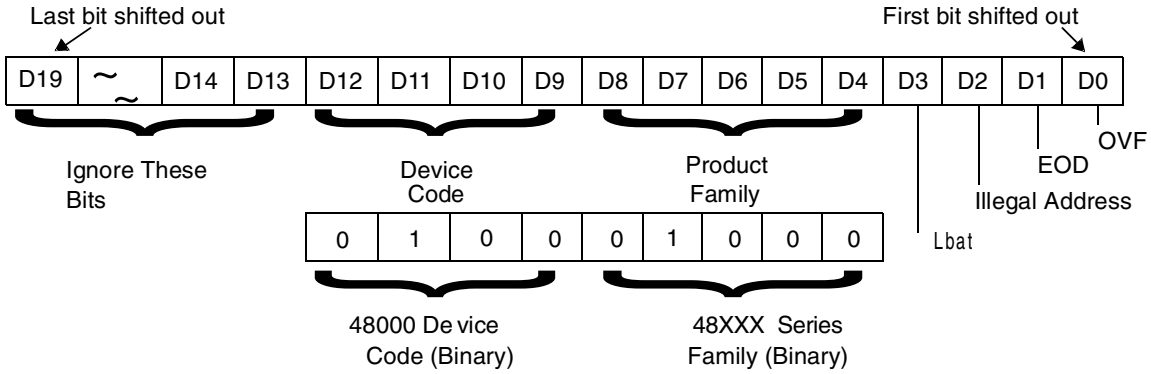
Each device in the APR48XX series family contains an embedded Silicon Identification (SID). The SID can be read by the host processor to identify which family / family member is being used. Reading the device SID requires issuing two OpCode commands; a SID command followed by any other command, usually a NOP command. The device will clock the SID data out on the DO pin as the command that follows the SID command is clocked in. Figure 9 is a diagram that describes the process necessary for reading SID information.

Figure 9 SID Timing



The SID information follows the format given in Figure 10. The first bit shifted out, D0, is the Overflow bit. The Overflow bit is set to a binary 1 if an attempt was made to record beyond the available memory. The Overflow bit is set to a 0 if an overflow has not occurred. This bit is cleared after it has been read. The D1 bit is the End Of Data (EOD) bit. The EOD bit is set when the device stops playing or fast forwarding as a result of EOD bit in memory. The EOD bit is cleared after it has been read. The D2 bit is the Illegal Address Bit. The Illegal Address Bit is set whenever an illegal address is sent to the device. The D3 bit is the Lbat bit. This bit is set when the device senses a supply voltage below specification. The following five bits represent the product family. The APR48XX product family code is binary 01000 as shown in Figure 10. The next four bits represent the device code. The APR48000 device code is binary 0100 as shown in Figure 10 The last seven bits are random data and should be ignored.

Figure 10 SID Bit Stream



Writing Digital Data

Digital data is written into the device using the *DIG_WRITE* command. No mixing of analog data and digital data within a sector is possible. Sectors 0 through 9 are tested and guaranteed for digital storage. Other sectors, with the exception of sector 639, can store data but have not been tested, and are thus not guaranteed to provide 100% good bits. This can be managed with error correction or forward check-before-store methods. Issuing a *DIG_ERASE* command on sector 639 will cause data throughout all sectors to be lost.

A sector must be erased, using the *DIG_ERASE* command, before digital data can be written to it. This requirement is necessary whether analog data or digital data was previously stored in the sector. A sector should not be erased more than once between analog or digital write operations. Executing multiple erase operations on a sector will permanently damage the sector. A sector can be reallocated to either analog storage or digital storage at any time.

The process of storing digital data begins by sending a *DIG_WRITE* command. The *DIG_WRITE* command is followed immediately by four buffer bits. These bits will not be stored in the array and must be considered don't care bits. Immediately following the four buffer bits should be the data that you wish to store. All 3004 bits must be stored. Four additional buffer bits must be clocked into the device following the stored data. These bits will not be stored in the array and must be considered don't care bits. Ending a digital write command early will permanently damage the sector.

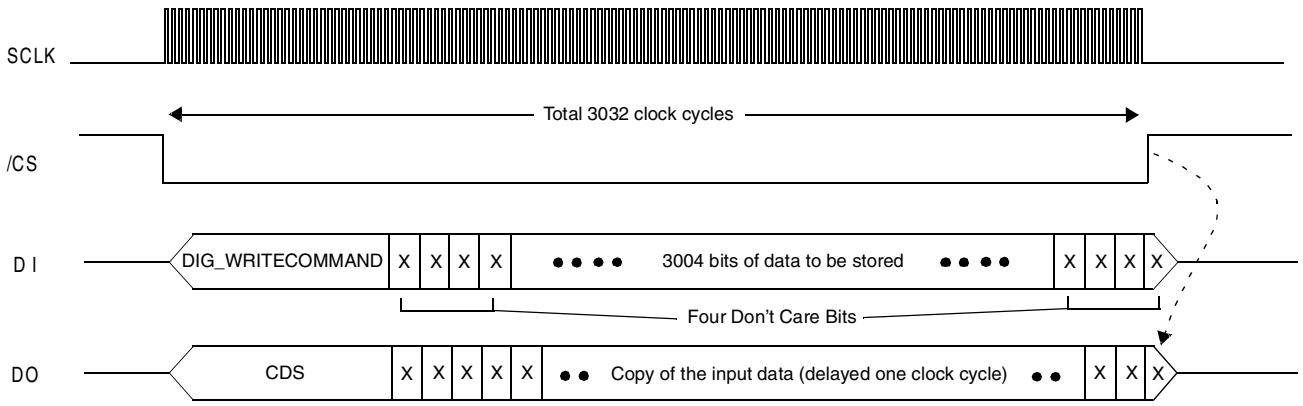
The DO pin will clock out the normal 20 bit CDS followed by five don't care bits, a copy of the 3004 data bits, and finally three don't care bits.

Figure 11 shows a timing diagram which describes the digital storage process. All timing with the exception of T_{pSCLK} should adhere to the specifications given in Figure 4 and Figure 7. The T_{pSCLK} specification is replaced by the DT_{pSCLK} when storing digital data.

Note: The DIG_ERASE command should not be used before storing analog data. The device will perform its own internal erase before analog storage.

Figure 11 does not show the DIG_ERASE command which must be executed on a sector before digital data can be stored.

Figure 11 Writing Digital Data



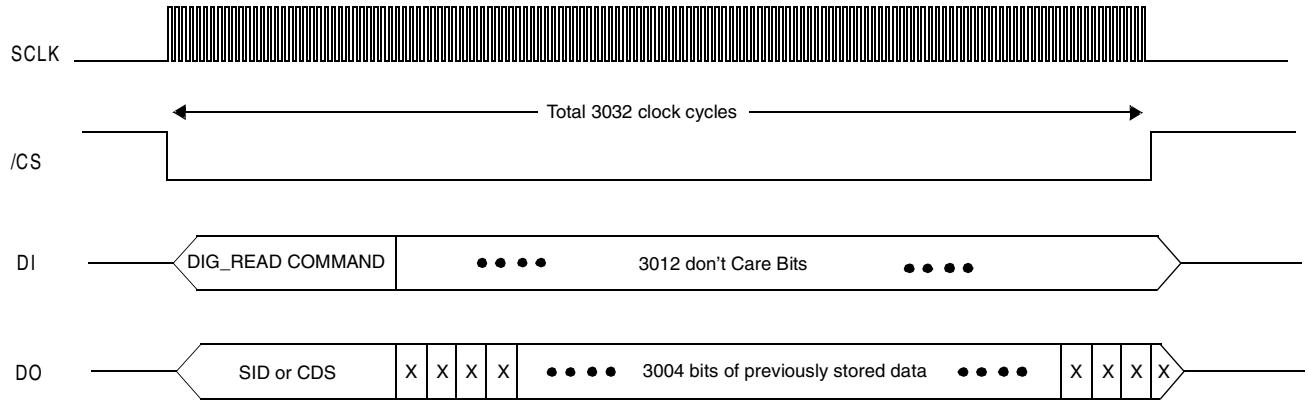
Reading Digital Data

Digital data is read from the device using the *DIG_READ* command. To read data you must send a *DIG_READ* command immediately followed by 3012 don't care bits during the same /CS cycle. The data previously stored in the specified sector will begin to appear on the DO pin after the current device status or SID and four buffer bits. The next 3004 bits are the previously stored data. The first bit shifted out is the first bit that was written. The last bit shifted out is the last bit that was written. There are four random don't care bits following the 3004 bits of user data.

An incomplete read of the sector is allowed. An incomplete read is defined a a read with less than 3032 clock cycles. All incomplete read cycles require one extra SCLK cycle after the /CS signal returns high.

Figure 12 shows a timing diagram which describes the entire process for a complete sector read. All timing with the exception of T_{pSCLK} should adhere to the specifications given in Figure 4 and Figure 7. The T_{pSCLK} specification is replaced by the DT_{pSCLK} when reading digital data.

Figure 12 Reading Digital Data

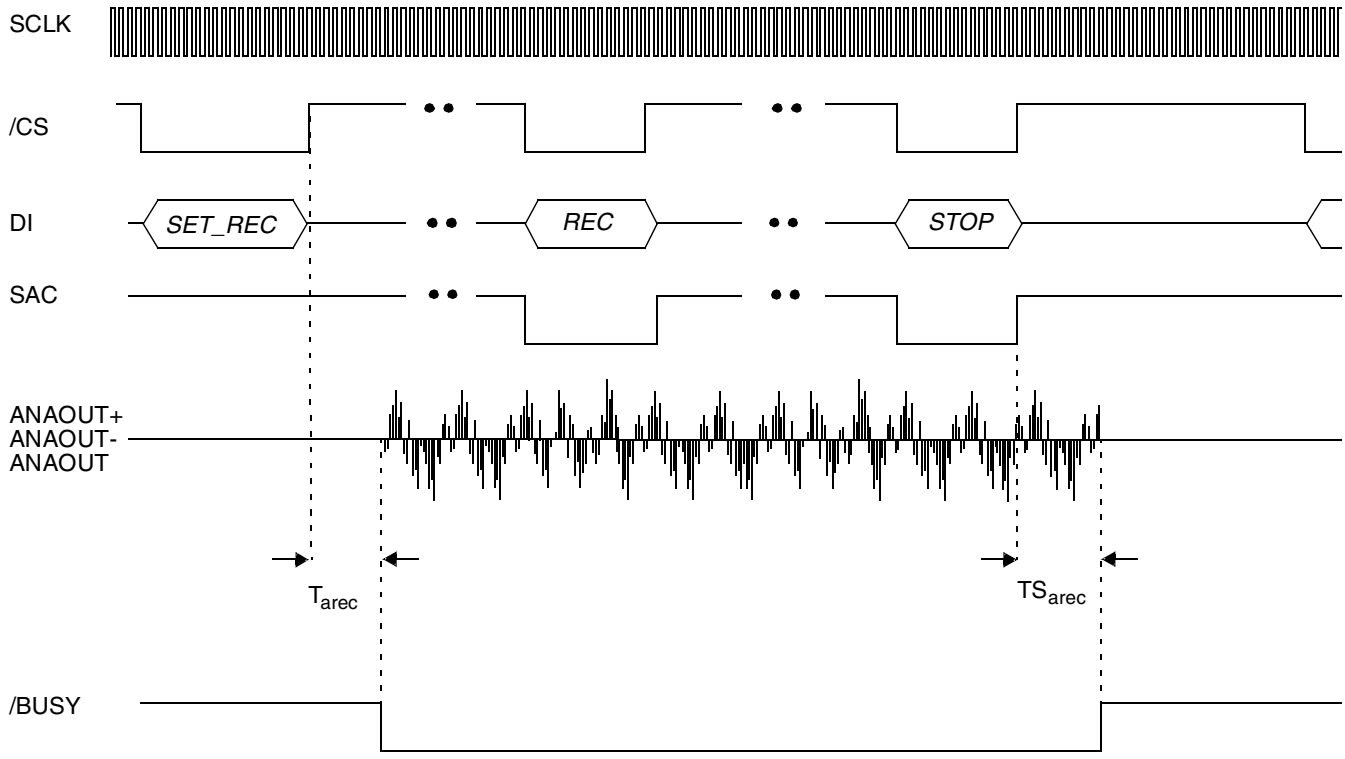


Recording Audio Data

When a *SET_REC* or *REC* command is issued the device will begin sampling and storing the data present on ANAIN+ and ANAIN- to the specified sector. After half the sector is used the SAC pin will drop low to indicate that a new command can be accepted. The device will accept commands as long as the SAC pin remains low. Any command received after the SAC returns high will be queued up and executed during the next SAC cycle.

Figure 13 shows a typical timing diagram and OpCode sequence for a recording operation. In this example the *SET_REC* command begins recording at the specified memory location after T_{arec} time has passed. Some time later the low going edge on the SAC pin alerts the host processor that the first sector is nearly full. The host processor responds by issuing a *REC* command before the SAC pin returns high. The *REC* command instructs the APR48000 to continue recording in the sector immediately following the current sector. When the first sector is full the device automatically jumps to the next sector and returns the SAC signal to a high state to indicate that the second sector is now being used. At this point the host processor decides to issue a *STOP* command during the next SAC cycle. The device follows the *STOP* command and terminates recording after TS_{arec}.The /BUSY pin indicates when actual recording is taking place.

Figure 13 Typical Recording Sequence

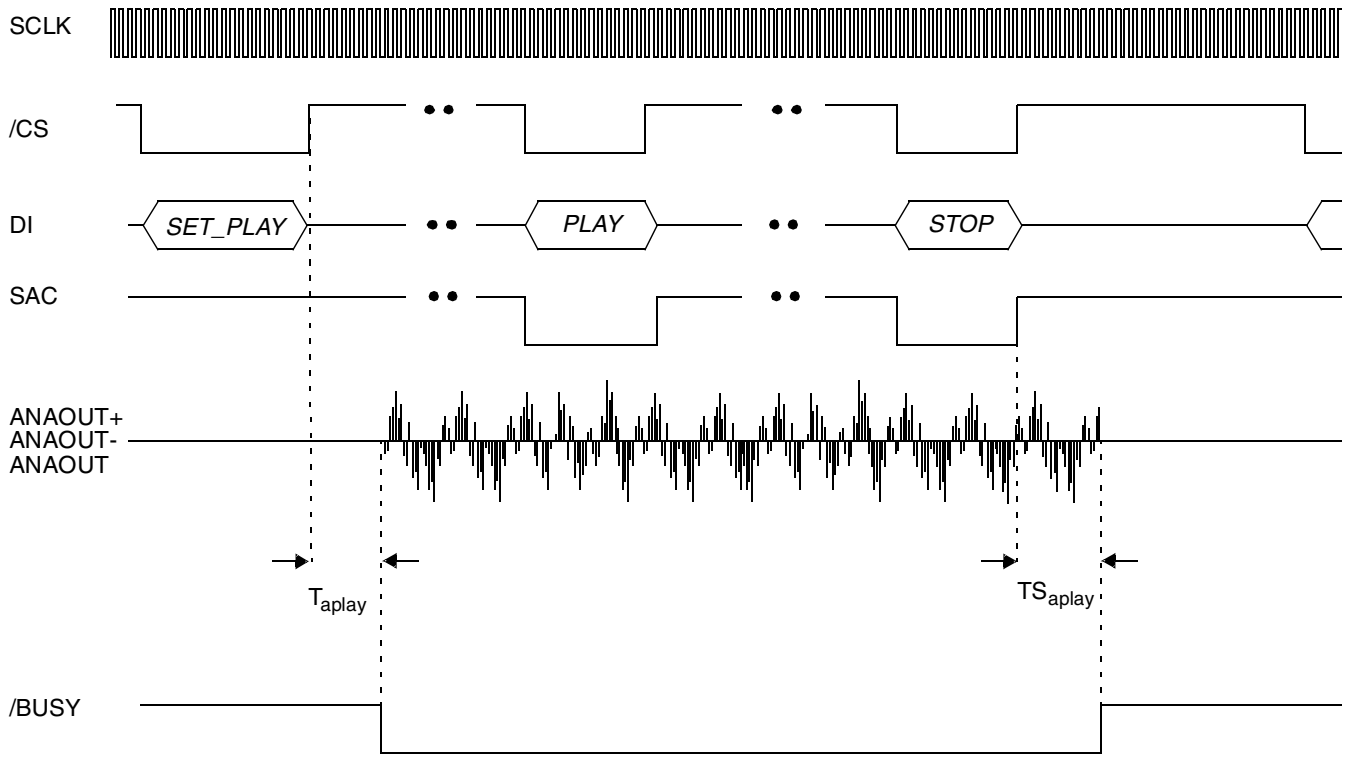


Playing Back Audio Data

When a *SET_PLAY* or *PLAY* command is issued the device will begin sampling the data in the specified sector and produce a resultant output on the AUDOUT, ANAOUT-, and ANAOUT+ pins. After half the sector is used the SAC pin will drop low to indicate that a new command can be accepted. The device will accept commands as long as the SAC pin remains low. Any command received after the SAC returns high will be queued up and executed during the next SAC cycle.

Figure 14 shows a typical timing diagram and OpCode sequence for a playback operation. The *SET_PLAY* command begins playback at the specified memory location after T_{aplay} time has passed. Some time later the low going edge on the SAC pin alerts the host processor that half of the first sector has been played back. The host processor responds by issuing a *PLAY* command during the SAC low time. The *PLAY* command instructs the APR48000 to continue playback of the sector immediately following the current sector. When the first sector has been played back the device jumps to the next sector and returns the SAC signal to a high state to indicate that the second sector is now being played. At this point the host processor decides to issue a *STOP* command during the next available SAC low time. The device follows the *STOP* command and terminates playback after TS_{aplay}. The /BUSY pin indicates when actual playback is taking place.

Figure 14 Typical Playback Sequence



Note: Command timing is not scale

Handshaking signals

Several signals are included in the device that allow for handshaking. These signals can simplify message management significantly depending on the message management scheme used.

The /INT signal can be used to generate interrupts to the processor when attention is required by the APR48000 This pin is normally high and goes low when an interrupt is requested. An interrupt is generated whenever a EOD or Overflow occurs. An interrupt is also generated after a PWRUP command if a low battery VCC is sensed.

The SAC signal is used to determine when the device is nearing the end of the current memory segment during either a record, play or forward operation. The SAC signal is in a normally high state. The signal goes low after half the currently active segment has been played or recorded. The signal returns to a high state after the entire segment has been played or recorded. The microprocessor should sense the

low edge of the SAC signal as an indicator that the next segment needs to be selected, and do so before the SAC signal returns high. Failing to specify the next command before the current segment is exhausted (either during recording or playback) will result in a noticeable gap during playback.

The /BUSY pin indicates when the device is performing either a play, record or fast forward function. The host microprocessor can monitor the busy pin to confirm the status of these commands. The Busy pin is normally high and goes low while the device is busy. The low time is governed by the length of recording or playback specified by the user.

Sampling Rate and Voice Quality

The Nyquist Sampling Theorem requires that the highest frequency component a sampling system can accommodate without the introduction of aliasing errors is equal to half the sampling frequency. The APR48000 automatically filters its input, based on the selected sampling frequency, to meet this requirement.

Higher sampling rates increase recording bandwidth, and hence voice quality, but also use more memory cells for the same amount of recording time. The APR48000 accommodates sampling rates as high as 8kHz.

Lower sampling rates use less memory cells and effectively increase the duration capabilities of the device, but also reduce recording bandwidth. The APR48000 allows sampling rates as low as 4 kHz.

Designers can thus control the quality/duration trade-off by controlling the sampling frequency. Sampling frequency can be controlled by using the PWRUP command. This command can change sampling frequency regardless of whether the internal oscillator is used or an external clock is used.

The APR48000 derives its sampling clock from one of two sources; internal or external. If a clocking signal is present on the EXTCLK input the device will automatically use this signal as the sampling clock source. If no input is present on the EXTCLK input the device automatically defaults to the internal clock source. When the EXTCLK pin is not used it should be tied to GND.

An internal clock divider is provided so that external clock signals can be divided down to a desired sampling rate. This allows high frequency signals of up to 10 MHz to be fed into the EXTCLK pin. Using this feature simplifies designs by allowing use of a clock already present in the system, as opposed to having to generate or externally divide down a custom clock. Details for programing the clock divider are described in the SPI interface section under the PWRUP paragraph.

The default power up condition for the APR48000 is to use the internal oscillator at a sampling frequency of 6.4 kHz.

Storage Technology

The APR48000 stores voice signals by sampling incoming voice data and storing the sampled signals directly into FLASH memory cells. Each FLASH cell can support voltage ranges from 1 to 256 levels. These 256 discrete voltage levels are the equivalent of eight (2^8=256) bit binary encoded values. During playback the stored signals are retrieved from memory, smoothed to form a continuous signal and finally amplified before being fed to an external speaker amplifier.

Squelch

The APR48000 is equipped with an internal squelch feature. The Squelch circuit automatically attenuates the output signal by 6 db during quiet passages in the playback material. Muting the output signal during quiet passages helps eliminate background noise. Background noise may enter the system in a number of ways including: present in the original signal, natural noise present in some power amplifier designs, or induced through a poorly filtered power supply.

The response time of the squelch circuit is controlled by the time constant of the capacitor connected to the SQLCAP pin. The recommended value of this capacitor is 1.0 uF. The squelch feature can be disabled by connecting the SQLCAP pin to VCC.

The active low output /SQL goes low whenever the internal squelch activates. This signal can be used to squelch the output power amplifier. Squelching the output amplifier results in further reduction of noise; especially when the power amplifier is run at high gain & loud volumes.

Sample Application

Figure 15 shows a sample application utilizing a generic microcontroller and SPI interface for message management.

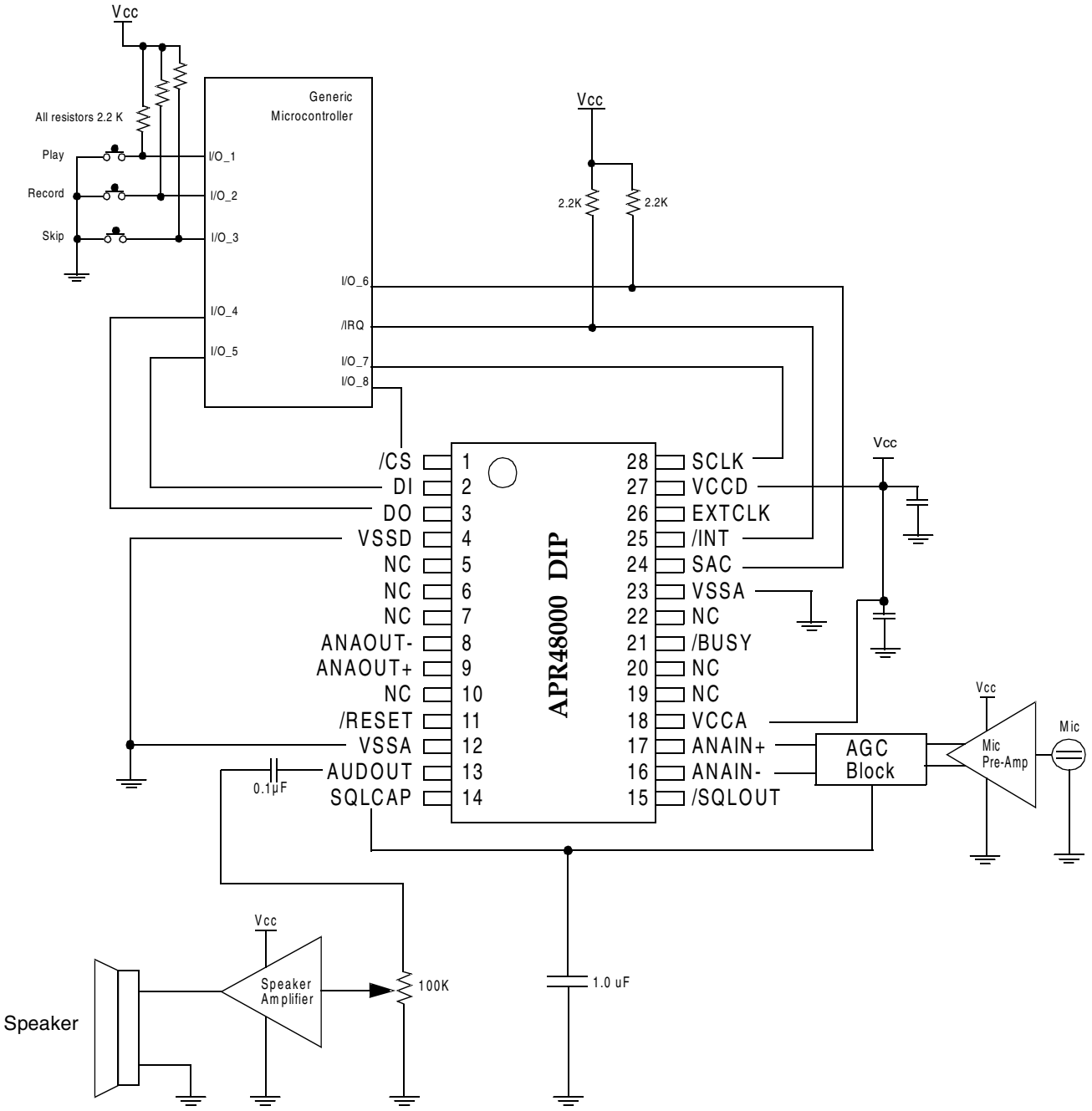
The microcontroller uses three general purpose inputs for the play, record and skip buttons. Five general purpose I/O signals are utilized in the SPI interface. The /RESET and /BUSY signal are not used in this design.

The output signal must be amplified in order to drive a speaker. Several vendors supply integrated speaker amplifiers that can be used for this purpose.

A microphone amplifier and AGC are recommended. Both blocks are optional. Several vendors supply integrated microphone/AGC amplifiers that can be used for this purpose.

Note that the AGC circuit can be simplified by using the SQLCAP signal as a peak detector signal.

Figure 15 Sample Schematic using DIP package



Pin Descriptions

Table three shows pin descriptions for the APR48000 device. All pins are listed in numerical order with the exception of VCC, VSS and NC pins which are listed at the end of the table.

Table 3 APR48000 28 Pin Number & Description

Pin Name	Pin No. 28 pin TSOP	Pin No. 28 pin DIP	Pad No. (Die) *Reference Figure 18*	Functionality
SAC	2	24	27	**Sector Address Control Output:** This active low output indicates when the device is nearing the end of the current segment.
/INT	5	25	28	**Interrupt Output:** This active low open drain output goes low whenever the device reaches the end of a message or the device overflows. When connected to the interrupt input of the host microcontroller this output can be used to implement powerful message management options.
EXTCLK	6	26	29	**External Clock Input:** This input can be used to feed the device an external sample clock instead of using the internal sampling clock. This pin should be connected to VSSA when not in use.
SCLK	8	28	33	**SPI Clock Input:** Data is clocked into the device through the DI pin upon the rising edge of this clock. Data is clocked out of the part through the DO pin on the falling edge.
/CS	9	1	2	**Chip Select Input:** This active low input selects the device as the currently active slave on the SPI interface. When this pin is high the device tri-states the DO pin and ignores data on the DI pin.
DI	10	2	3	**Data Input:** The DI input pin receives the digital data input from the SPI bus. Data is clocked on the rising edge of the SCLK input.
DO	11	3	4	**Data Output:** Data is available after the falling edge of the SCLK input.
ANAOUT-	15	8	9	**Negative Audio Output:** This is the negative audio output for playback of prerecorded messages. This output is usually fed to the negative input of a differential input power amplifier. The power amplifier drives an external speaker.
ANAOUT+	16	9	10	**Positive Audio Output:** This is the positive audio output for playback of prerecorded messages. This output is usually fed to the positive input of a differential input power amplifier. The power amplifier drives an external speaker.
/RESET	17	11	11	**Reset Input:** This active low input clears all internal address registers and restores the device to its power up defaults.
AUDOUT	20	13	15	**Single Ended Audio Output:** This is the audio output for playback of prerecorded messages. This output is usually fed to the input of a power amplifier for driving an external speaker.
SQLCAP	22	14	16	**Squelch Capacitor I/O:** This pin controls the attack time of the squelch circuitry. Connect his pin to GND through a 1.0 uf capacitor to enable the squelch feature. The capacitor's time constant will affect how quickly the squelch circuitry reacts. Connect this pin to VCCA to disable the squelch feature.
/SQL	23	15	17	**Squelch Output:** This active low output indicates when the internal squelch circuitry has activated. This signal can be used to automatically squelch the external power amplifier. Squelching the external power amplifier can result in an even greater reduction of background noise.
ANAIN-	24	16	18	**Inverting Analog Input:** This input is the inverting input for the analog signal that the user wishes to record. When the device is used in a differential input configuration this pin should receive a 16 mV peak to peak input coupled through a 0.1uF capacitor. When the device is used in a single ended input configuration this input should be tied to VSSA through a 0.1 uF capacitor.

Pin Name	Pin No. 28 pin TSOP	Pin No. 28 pin DIP	Pad No. (Die) *Reference Figure 18*	Functionality
ANAIN+	25	17	19	**Non-Inverting Analog Input:** This input is the non-inverting input for the analog signal that the user wishes to record. When the device is used in a differential input configuration this pin should receive a 16 mV peak to peak input coupled through a 0.1 uF capacitor. When the device is used in a single ended input configuration this pin should receive a 32 mV peak to peak input coupled through a 0.1 uF capacitor.
/BUSY	28	21	23	**Busy Output:** This active low output is low during either a record, playback or fast forward operation. The pin is tri-stated otherwise. This pin can be connected to an LED to indicate playback/record operation to the user. This pin can also be connected to an external microcontroller as an indication of the status of playback, record, forward, or digital operation.
VCCD	7	27	30, 31, 32	**Digital Power Supply:** This connection supplies power for all on-chip digital circuitry. This pin should be connected to the 3.0 V power plane through a via. This pin should also be connected to a 0.1 uF bypass cap as close to the pin as possible.
VCCA	26	18	20, 21	**Analog Power Supply:** This connection supplies power for all on-chip analog circuitry. This pin should be connected to the 3.0 V power plane through a via. This pin should also be connected to a 0.1 uF bypass cap as close to the pin as possible.
VSSA	1, 18	12,23	12, 13, 14, 24, 25, 26	**Analog Ground:** These pins should be connected to the ground plane through a via. The connection should be made as close to the pin as possible.
VSSD	12	4	5, 6	**Digital Ground:** This pin should be connected to the ground plane through a via. The connection should be made as close to the pin as possible.
NC	3, 4, 13, 14,19, 21, 27	5, 6, 7, 10, 19, 20, 22	1, 7, 8, 22	**No Connect:** These pins should not be connected to anything on the board. Connection of these pins to any signal, GND or VCC may result in incorrect device behavior or cause damage to the device.

Electrical Characteristics

The following tables list Absolute Maximum Ratings, Recommended DC Characteristics, and recommended AC Characteristics for the APR48000 device.

Absolute Maximum Ratings

Stresses greater than those listed in Table 4 may cause permanent damage to the device. These specifications represent a stress rating only. Operation of the device at these or any other conditions above those specified in the recommended DC Characteristics or recommended AC Characteristics of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Table 4 Absolute Maximum Ratings.

Item	Symbol	Condition	Min	Max	Unit
Power Supply voltage	V_{CC}	T_A = 25 C	-0.3	7.0	V
Input Voltage	V_{IN}	T_A = 25 C Device VCC = 3.0 V	-0.3	5.5	V
Storage Temperature	T_{STG}	-	-65	150	°C
Temperature Under Bias	T_{BS}	-	-65	125	°C
Lead Temperature	T_{LD}	<10s		300	°C

Table 5 DC Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VCCA VCCD		2.7	3.0	3.3	V
Operating Temperature	T_A		0		+70	°C
Input High Voltage	V_{IH}	VCC = 2.7V	2.4	3	5.5	V
Input Low Voltage	V_{IL}	VCC = 3.3V	V_{SS} - 0.3V	0	.4	V
Output High Voltage	V_{OH}	VCC = 2.7V I_{OH}=-1.6mA	VCCD - 0.5V			V
Output Low Voltage	V_{OL}	VCC = 2.7V I_{OL}=1.0mA			0.4	V
Input Leakage Current	I_{IH}	VCC = 3.3V V_{IH}=V_{CC}		0.3	1	A
Input Leakage Current	I_{IL}	VCC = 3.3V V_{IL}=V_{SS}		0	-1	A
Output Tristate Leakage Current	I_{OZ}	VCC = 3.3V V_{OUT}=V_{CC} *or* V_{OUT}=V_{ss}			±1	A
Operating Current Consumption	I_{CC}	VCC = 3.3V Recording Playback Idle		 25 15 2.5		 mA mA mA
Standby Current Consumption	I_{CCS}	VCC = 3.3V After 20 sec.			1	A

Table 6 AC Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
ANAIN+ or ANAIN- input voltage	V_{MI}			45	50	mV_{P-P}
ANAIN+ input resistance	R_{ANAIN}			3		k
ANAIN+/ANAIN- Gain	G_{ANAIN}			22	23	dB
ANAOUT Output Voltage	V_{ANOUT}			560	700	m_{VP-P}
Total Harmonic Distortion	THD	@ 1kHz & 45mV_{P-P} input		0.5	1	%
VCC ready to fall /CS	T_{pwrup}	90% of VCC min. specification	10			ms
/RESET low time	T_{loRST}		1			ms
Rise /RESET to fall /CS	T_{Rdone}		1			ms
/CS fall to clock edge	T_{fcs}		500			ns
SPI Data set-up time	T_{suDI}		200			ns
Period SPI clock	T_{pSCLK}		1000			ns
SPI data hold time	T_{hDI}		200			ns
SPI clock low time	T_{loSCLK}		400			ns

Item	Symbol	Condition	Min	Typ	Max	Unit
SPI clock high time	T_{hiSCLK}		400			ns
Clock to rising edge of /CS	T_{rCS}		200			ns
Fall of /CS to DO output	T_{fcsDO}				200	ns
Fall of SCLK to data out valid	T_{fSCLK}				1000	ns
Rise of /CS to DO high Z	T_{hzDO}				500	ns
Period SPI clock for digital read, write	DT_{pSCLK}	@4kHz Internal sample clock @8kHz Internal sample clock External sample clock	500 250 *Equation 1*			S S S
First SET_REC command to start recording	Tarec	@4kHz Internal sample clock @8kHz Internal sample clock External sample clock		376 188 *Equation 2*		ms ms S
Rise of SAC after STOP Command to end of recording	TSarec	@4kHz Internal sample clock @8kHz Internal sample clock External sample clock		376 188 *Equation 2*		ms ms S
First SET_PLAY command to audio output	Taplay	@4kHz Internal sample clock @8kHz Internal sample clock External sample clock		376 188 *Equation 2*		ms ms S
STOP after SET_PLAY or PLAY to end of audio output	TSaplay	@4kHz Internal sample clock @8kHz Internal sample clock External sample clock		376 188 *Equation 2*		ms ms S
SAC period	T_{pSAC}	REC, PLAY @4kHz REC, PLAY @8kHz REC, PLAY EXTCLK FWD @4kHz FWD @8kHz FWD @ EXTCLK		752 376 *Equation 3* 2 1 *Equation 4*		ms ms ms ms S
SAC low time	T_{loSAC}	REC, PLAY @4kHz REC, PLAY @8kHz REC, PLAY EXTCLK FWD @4kHz FWD @8kHz FWD @ EXTCLK		94 47 equation 5 0.25 0.125 *Equation 6*		ms ms ms ms S
See Figure 6 and Table 1	T_{next1}		5			S
See Figure 6 and Table 1	T_{next2}		5			ms
See Figure 6 and Table 1	T_{next3}	@4kHz Internal sample clock @8kHz Internal sample clock External sample clock		752 376 *Equation 3*		ms ms S

Item	Symbol	Condition	Min	Typ	Max	Unit
See Figure 6 and Table 1	T_{next4}	Previous command = *SET_REC, REC, SET_PLAY, PLAY* @4kHz Internal sample clock @8kHz Internal sample clock External sample clock		 470 235 *Equation 7*		 ms ms S
		Previous command = *SET_FWD, FWD* @4kHz Internal sample clock @8kHz Internal sample clock External sample clock		 1.25 0.625 *Equation 8*		 ms ms
		Previous command = All Others @4kHz Internal sample clock @8kHz Internal sample clock External sample clock		 5 5 *5*		 s s s

Notes:

$$Equation1 = \frac{ExternalClockPeriod}{2(PrescalerValue)}$$

$$Equation2 = \frac{1504(ExternalClockPeriod)}{PrescalerValue}$$

$$Equation3 = \frac{3008(ExternalClockPeriod)}{PrescalerValue}$$

$$Equation4 = \frac{8(ExternalClockPeriod)}{PrescalerValue}$$

$$Equation5 = \frac{376(ExternalClockPeriod)}{PrescalerValue}$$

$$Equation6 = \frac{ExternalClockPeriod}{PrescalerValue}$$

$$Equation7 = \frac{1880(ExternalClockPeriod)}{PrescalerValue}$$

$$Equation8 = \frac{5(ExternalClockPeriod)}{PrescalerValue}$$

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