微主控 IC

产品规格书

General Description

The DL7503 is an 8 bit RISC high performance microcontroller. It is equipped with 1Kx14bits OTP(One Time Programmable) ROM, 48 Bytes RAM, Timer/Counter, Interrupt, LVR(Low Voltage Reset) and I/O ports in a single chip.

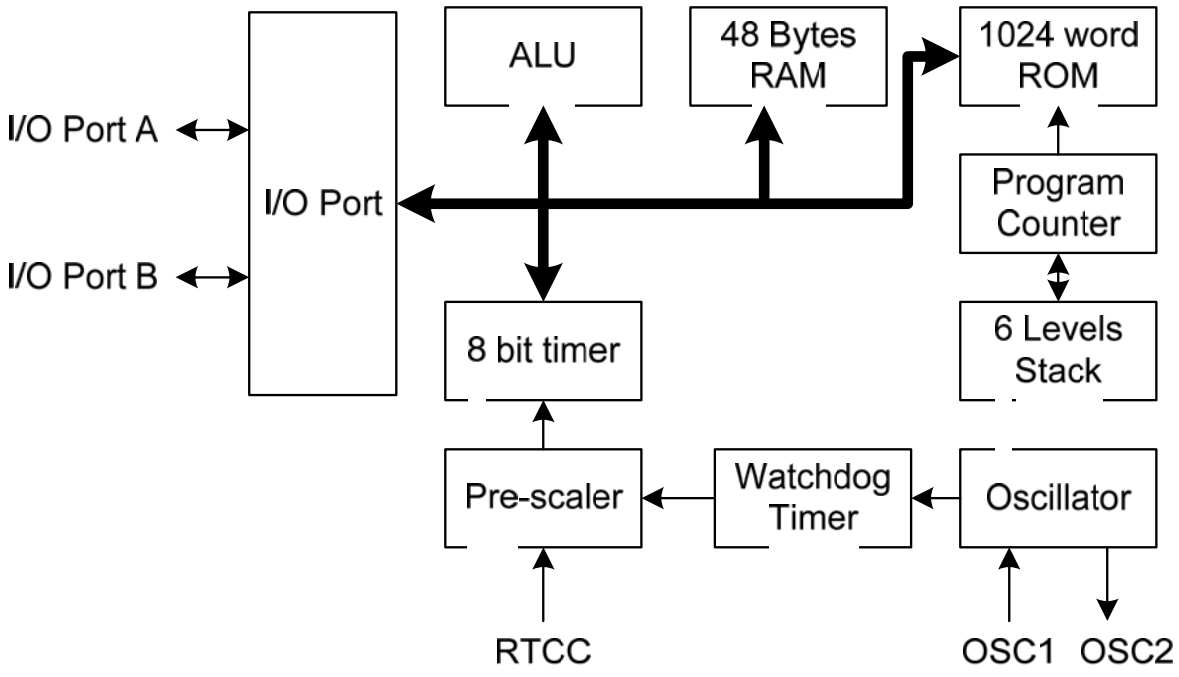
1. Feature

- ROM size: 1K x 14 bits
- RAM: 48 x 8 bits
- STACK: 6 Levels
- One instruction is built by 4 system clock.
- Reset mode:
  - Power-On reset
  - Low voltage reset
  - RESETB/PB3 (if set as reset pin) input a negative pulse.
  - Watchdog timer count overflow reset
- 5 oscillation mode can be selected
  - External RC, LS (Low Speed) Crystal, NS (Normal Speed) Crystal and HS (High Speed) Crystal
  - Internal 4MHz RC oscillator
- Timer/counter: 1 sets.
  - TMR0: 8 bit count down timer/counter with auto reload function
- Watchdog Timer: On chip WDT is based on an internal RC oscillator (for WDT used only). Have 8 period can be selected. User can extend the WDT overflow period by using prescaler.
- Interrupt events:
  - TM0 Internal timer/event counter interrupt
  - External INT pin
- I/O port: 12 pins
  - PA0~3: 4 normal I/O pins
  - PB0~7: 8 pull high I/O pins with pin wake up function
- Wake-up mode:
  A. Watch Dog timer wakeup
  B. Port B (PB0~7) pin change wakeup
  C. i_WDT wakeup
- Different Package Type:
  MK6A12PD14C: 14 pin DIP
  MK6A12PS14C: 14 pin SOP

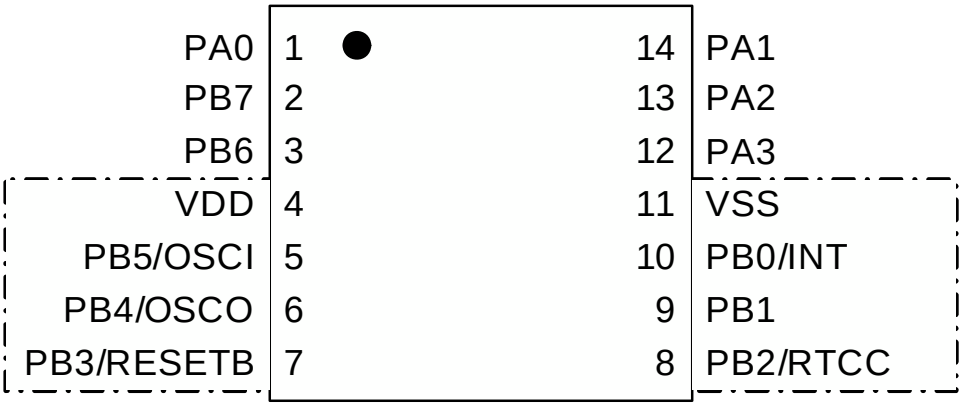
1.1 Features selection table :

MK6A12P	MK6A11EP
i_WDT set	i_WDT set
PB_PDM ($0DH) , bit4	Config , bit7

2. Block Diagram



3. Pin Definition & Pad Assignment



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4. Pin Description

Name	I/O	Pin type	Description
PA0~3	I/O	C	1. General purpose I/O port 2. With pull down resistor
PB0/INT	I/O	A	1. General purpose I/O port 2. With pull up/pull down/open drain functions by option 3. Pin change wake up from sleep mode 4. Interrupt active by rising edge trigger(option)
PB1	I/O	A	1. General purpose I/O port 2. With pull up/pull down/open drain functions by option 3. Pin change wake up from sleep mode
PB2/RTCC	I/O	A	1. General purpose I/O port 1. With pull up/pull down/open drain functions by option 2. Pin change wake up from sleep mode 3. Timer input (option)
PB3/RESETB	I	B	1. Input pin only 2. System reset signal (active low) 3. Pin change wake up from sleep mode
PB4/OSCO	I/O	E	1. General purpose I/O port 2. With pull up/open drain by option 3. Pin change wake up from sleep mode 4. Oscillator output pin (Crystal mode can not set pull high)
PB5/OSCI	I/O	E	1. General purpose I/O port 2. With pull up/open drain by option 3. Pin change wake up from sleep mode 4. Oscillator input pin (Crystal mode can not set pull high)
PB7~6	I/O	D	1. General purpose I/O port 2. With pull up/open drain by option 3. Pin change wake up from sleep mode
VDD	P		System Power Input
VSS	P		System Ground Input

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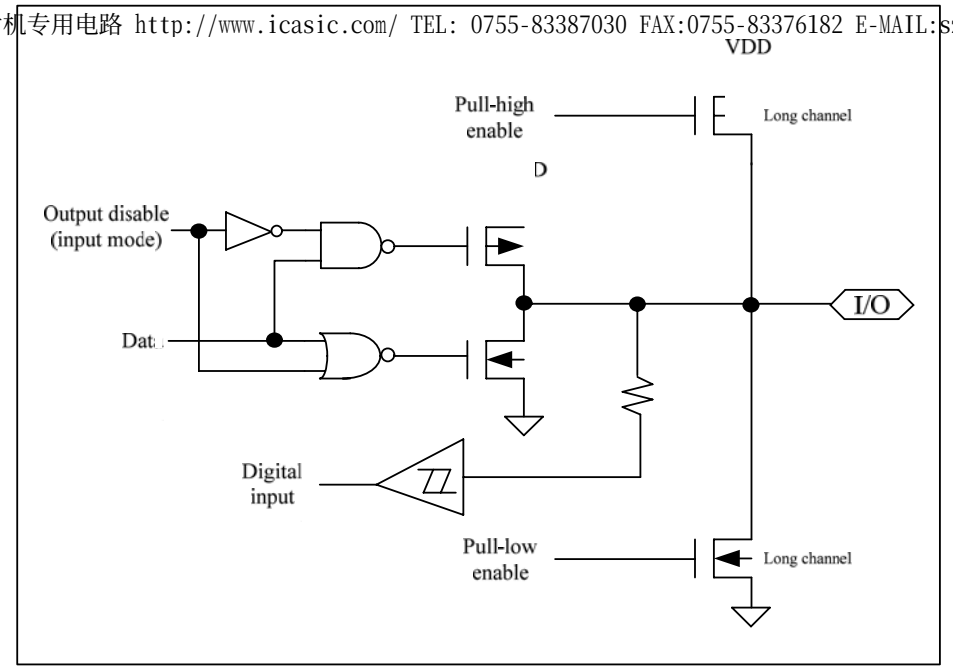
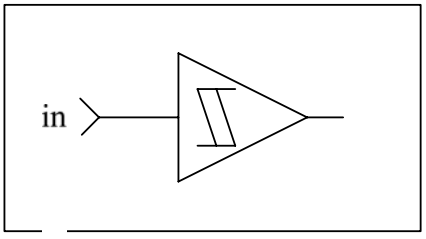
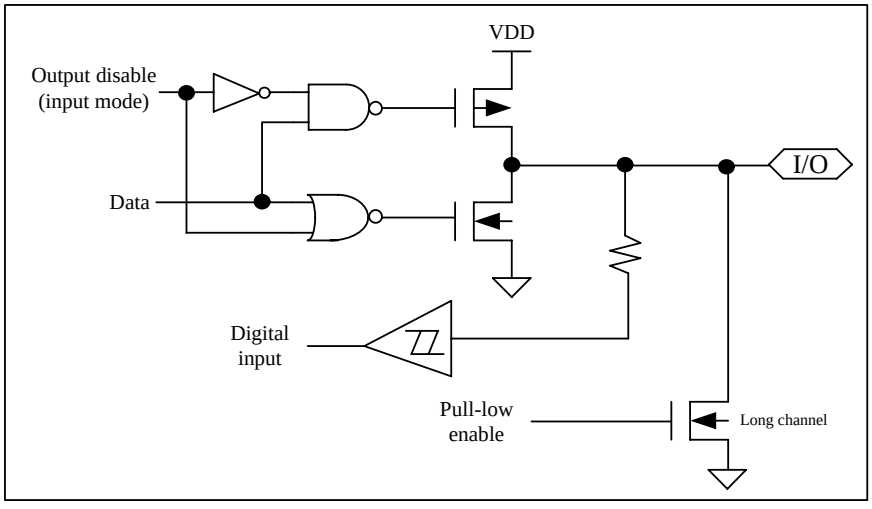


Pin circuit Type A



Pin circuit Type B



Pin circuit Type C

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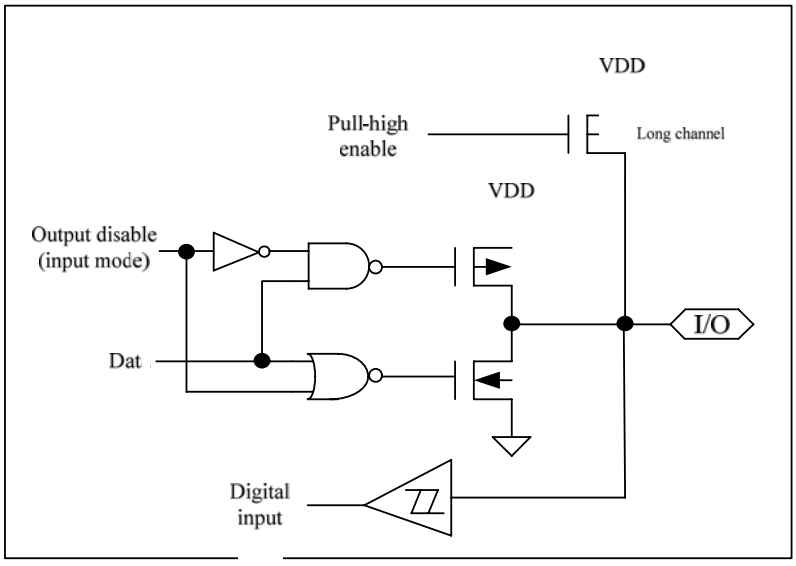
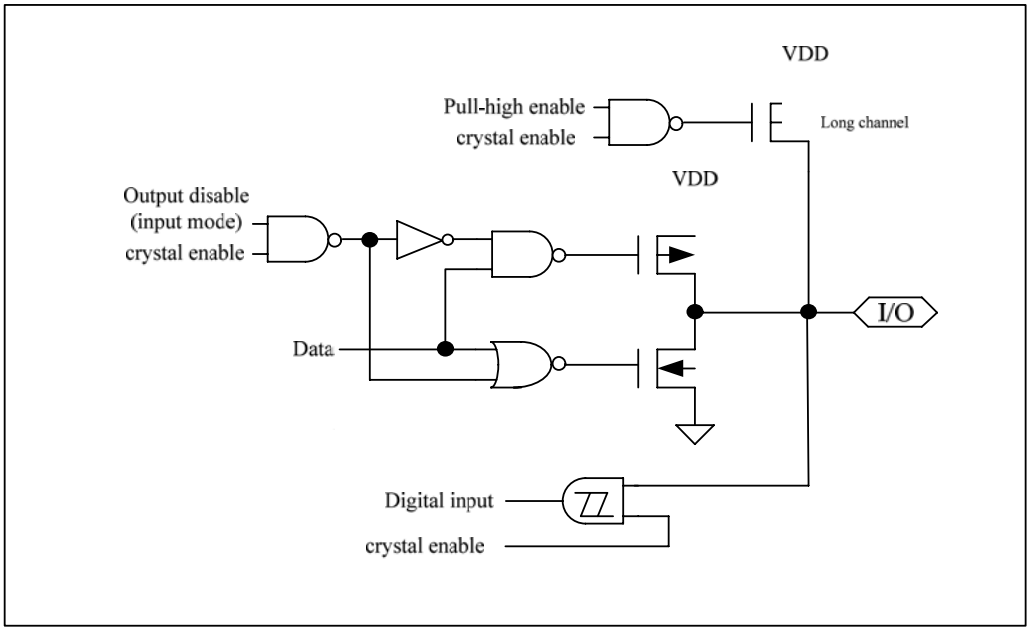


Pin circuit Type D



Pin circuit Type E

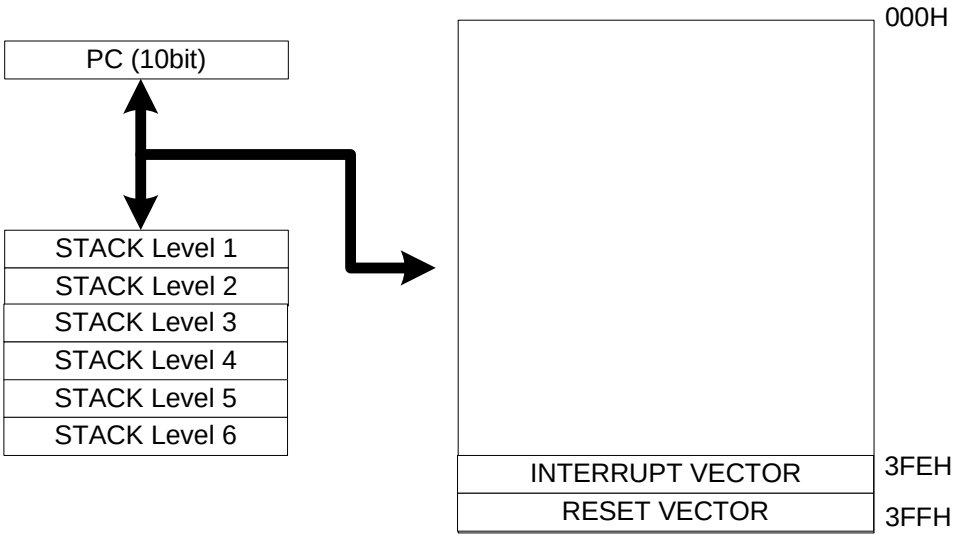
5. Memory Map

The DL7503 have two kinds of memory which are ROM (program memory) and RAM (data memory). The ROM is used to store the program, table and interrupt vectors. It is continuous 1024x14bits and don't need to switch bank. The RAM is 64(16+48)x8bits that include special function register and general-purpose RAM.

5.1 Program Memory (ROM)

Instruction and table are stored at this area. There is only one interrupt vector existed which means all the interrupt occurred would jump to the same vector. Programmer should use interrupt flag to judge what kind of interrupt is occurred. The program counter (PC) is 10 bit which can directly address all the 1024x16bits location. Look-up table can be put at anywhere of ROM.

The RESET vector is located at 3FFH and Interrupt vector is at 3FEH. The map is as below:

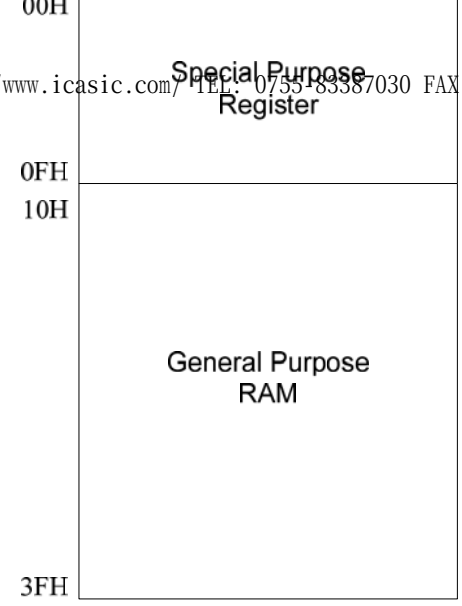


<Note> LCALL and LGOTO allow directly operate 1K word addressing

5.2 Data Memory (RAM)

The total RAM volumes are 48x8bits which includes two kinds of register group. One is 32x8bits general purpose RAM, the other is special purpose register that are 16x8bits. Every byte of special purpose register stored control's data or operation's data.

The data memory map is as below:



<Note> LCALL and LGOTO allow directly operate 1K word addressing

Special Purpose Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CONFIG	RES_T	RESETE	LV	WDTE	CPT	INRC	FOSC1	FOSC0
	Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit9**	**Bit8**
	--	--	ADJ5	ADJ4	ADJ3	ADJ2	ADJ1	ADJ0

<Note> CONFIG is a 14 bit special register

Name	Addr	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SELECT		TMR0_EN	WRT_CNT	SUR0	EDGE0	PSA	PS2	PS1	PS0
IAR	$00	A7	A6	A5	A4	A3	A2	A1	A0
TMR0	$01	D7	D6	D5	D4	D3	D2	D1	D0
PCL	$02	A7	A6	A5	A4	A3	A2	A1	A0
STATUS	$03	--	--	BS	$\overline{TO}$	$\overline{PD}$	Z	DC	C
BSR	$04	1	D6	D5	D4	D3	D2	D1	D0
PA	$05	--	--	--	--	PA3	PA2	PA1	PA0
PB	$06	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
IRQM	$09	INTM	--	--	--	--	--	PB0M	TM0M
IRQF	$0A	--	--	--	--	--	--	PB0F	TM0F

* PB_PUP	$0C	UB7	UB6	UB5	UB4	--	UB2	UB1	UB0
* PB_PDM	$0D	RTCCE	INTE	i_STAB	I_WDT	--	DB2	DB1	DB0
* PB_POD	$0E	OB7	OB6	OB5	OB4	--	OB2	OB1	OB0
WAKEUP	$0F	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0

<Note> "—" : mean no use.

" * " : mean write only .

<Note> PA_PDM($0B), PB_PUP($0C), PB_PDM($0D), PB_POD($0E) are write only register which can only use below instructions to write data :

```
MOVLA     REG_Value
MOVAM     PB_PDM
```

Configure Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CONFIG	RES_T	RESETE	LV	WDTE	CPT	INRC	FOSC1	FOSC0
	Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit9**	**Bit8**
	--	--	ADJ5	ADJ4	ADJ3	ADJ2	ADJ1	ADJ0

- Bit13~8 (ADJ5~0): Used to calibrated internal RC oscillator.
- Bit7(RES_T) : Power On reset time select .
  0 : Power On reset time=600us .
  1 : Power On reset time=20ms(init) .
- Bit6 (RESETE): RESETB pin define
  0: RESETB is normal input pin
  1: RESETB is system reset pin
- Bit5 (LV): Set reset voltage level of Low Voltage Reset (LVR)
  0: Low Voltage Reset ON
  1: Low Voltage Reset OFF
- Bit4 (WDTE): Watchdog timer enable/disable
  0: WDT disable
  1: WDT enable
- Bit3 (CPT): ROM Code Protection bit
  0: ON
  1: OFF

- Bit2~0 (INRC, FOSC1~0): OSC type and system clock select

Bit2	Bit1	Bit0	OSC Type	Resonance Frequency
INRC	FOSC1	FOSC0		
0	0	0	LS (low speed)	System clock=32~200KHz
0	0	1	NS (Normal speed)	System clock=200K~10MHz
0	1	0	HS (high speed)	System clock=10~20MHz
0	1	1	External RC	System clock=32K ~ 10MHz
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Internal RC	System clock=4MHz

4.2.3 **SELECT Register**

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SELECT	TMR0_EN	WRT_CNT	SUR0	EDGE0	PSA	PS2	PS1	PS0

Select register is used to control WDT and TM0. There is no specific data memory, it can only be set by SELECT instruction. It is a write-only register. The content of accumulator will be sent to SELECT register by executing the SELECT instruction. If SELECT register has never been set by program, its default value is 40H. The below table will explain each bit of select register.

Bit	Symbol	Description				
		PS2	PS1	PS0	TMR0 rate	WDT rate
2~0	PS2~PS0	0	0	0	1:2	1:1
		0	0	1	1:4	1:2
		0	1	0	1:8	1:4
		0	1	1	1:16	1:8
		1	0	0	1:32	1:16
		1	0	1	1:64	1:32
		1	1	0	1:128	1:64
		1	1	1	1:256	1:128
3	PSA	PSA: Prescaler assignment bit 1: Prescaler assigned to WDT 0: Prescaler assigned to TMR0				

4	EDGE0	1:increment when H→L transition on external clock 0: increment when L→H transition on external clock
5	SUR0	SUR0: TMR0 clock source bit 1: External clock input (> system clock / 8) 0: (System clock) / 4
6	WRT_CNT	WRT_CNT : Auto pre-load TMR0 data 1: enable 0: disable
7	TMR0_EN	TMR0_EN: TMR0 enable/disable 0: disable 1: enable

6. Function Deceptions

This device provide many functions that are I/O ports, Timer, WDT, Interrupt, Table location, Reset, Program Counter and STATUS register. We would like to describe in detail.

6.1 I/O Port

There are 2 I/O ports (A & B) to input or output data, each port has different function. The port A are general purpose I/O port with pull down resistor. The port B have multiple functions which can be used as general purpose I/O port with pull up resistor and pin wake up function. And some of them have another function by option.

6.1.1 Port A

A. PA($05H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA		--	--	--	PA3	PA2	PA1	PA0

- Bit3~0 (IOA3~0): Data of I/O ports A

B. PA_PDM($0BH):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA_PDM	--	--	--	--	DA3	DA2	DA1	DA0

- Bit3~0 (DA3~0): Pull down resistor enables/disable
  0: Pull down resistor disable.
  1: Pull down resistor enable.

6.1.2 Port B

A. PB($06H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0

- Bit7~0 (PB7~0): Data of I/O Ports B

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PB_PUP	UB7	UB6	UB5	UB4	--	UB2	UB1	UB0

- Bit7~0 (UB7~0): Pull up resistor enable/disable.
  0: Pull up resistor disable.
  1: Pull up resistor enable.

<Note> 1. PB3 is shared with RESETB and only can be used as input port. If used as PB3 then there is no pull up resistor. If used as RESETB, then there is pull up resistor.

1. UB4 and UB5 is used in RC oscillation mode only. If user use Crystal mode, then these two bits are useless and can not be set to pull up. Otherwise, it will cause malfunction.

C. PB_PDM($0DH):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PB_PDM	RTCCE	INTE	i_STAB	i_WDT	--	DB2	DB1	DB0

- Bit7: This bit has two functions, one is to select PB2/RTCC function, another is to enable TMR0 external clock source.
  0: PB2 pin is PB2
  1: PB2 pin is RTCC input and TMR0 external clock source from RTCC is enable

<Note> The method to count RTCC input are:

1. Use SELECT instruction to set SUR0 to 1.
2. Set RTCCE bit to 1 to set PB2 pin as RTCC and enable the RTCC clock in.

- Bit6: Select PB0/INT function
  0: PB0 pin is PB0
  1: PB0 pin is INT
- Bit5: i_STAB (i_WDT mode) wakeup times set .
  0: 1.25ms (init) .
  1: 625us (Low power consumption)
- Bit4(i_WDT) : Internal Watch_Dog timer wakeup .
  0 : i_WDT wakeup disable(init).
  1 : i_WDT wakeup enable(must set WDTE=1, enable).

- Bit2~0 (PB2~0): Pull down resistor enable/disable
  0: Pull down resistor disable
  1: Pull down resistor enable

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PB_POD	OB7	OB6	OB5	OB4	-	OB2	OB1	OB0

- Bit7~0 (OD7~0): Open drain enable/disable
  - 0: Open drain disable
  - 1: Open drain enable

<Note> PA_PDM($0B), PB_PUP($0C), PB_PDM($0D), PB_POD($0E) are write only register which can only use below instructions to write data :

```
MOVLA    REG_Value
MOVAM    PB_PDM
```

E. WAKEUP($0FH):

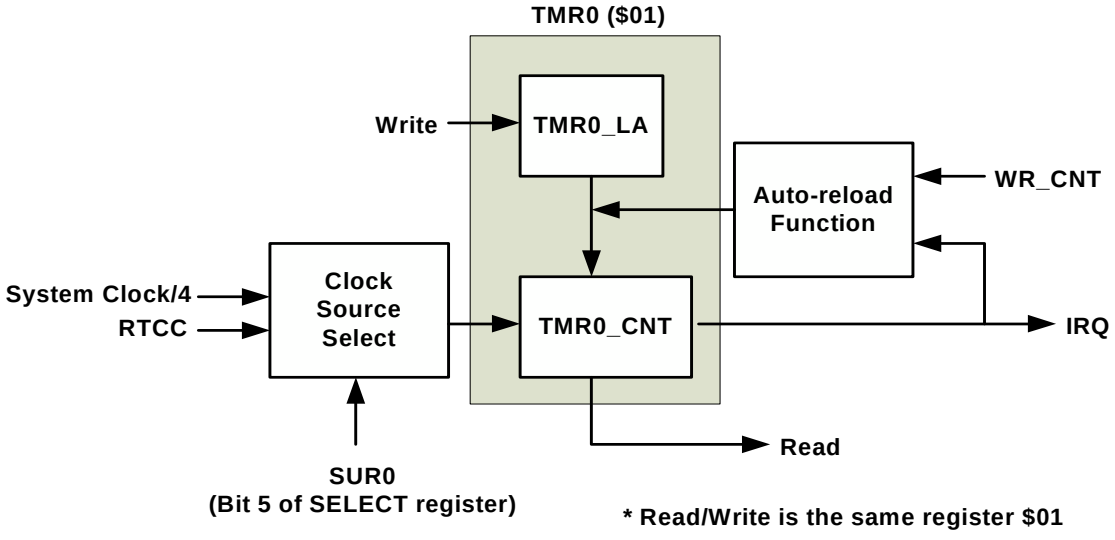
Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WAKEUP	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0

- Bit7~0 (EN7~0): Port B wakeup enable/disable
  - 0: Port B wakeup disable
  - 1: Port B wakeup enable

<Note> If i_WDT mode was enabled, bit 7(EN7) will be inhibited automatically.

6.2 Timer/Counter(TMR0)

The DL7503 provide one countdown timers/counters and 1 watchdog timer. Clock source of counters can be system clock or external clock by setting each timer control register. The detailed registers setting and block diagram are as below.



Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR0	D7	D6	D5	D4	D3	D2	D1	D0

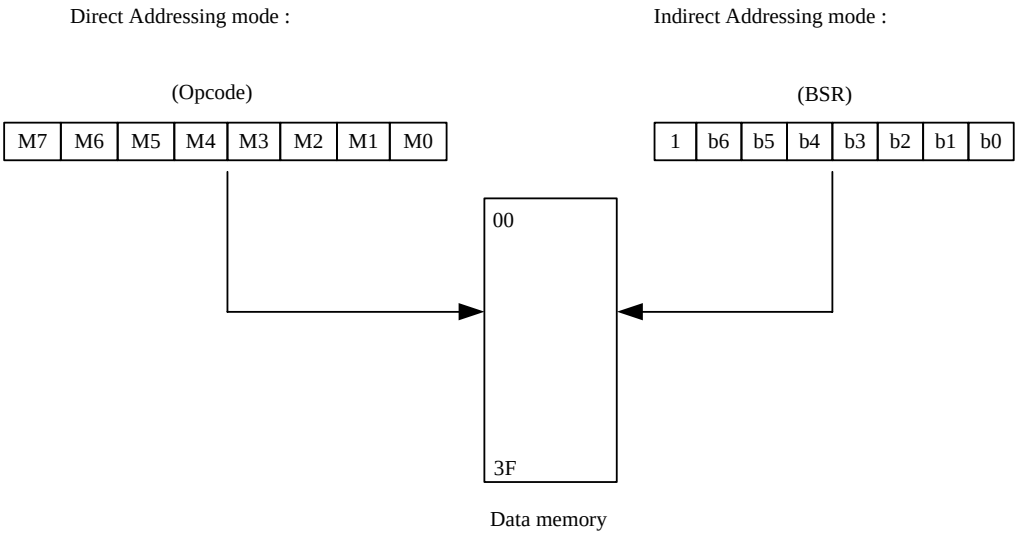
- Bit7~0 (TMR0): Timer0(TMR0) Data

<Note> The timer is down counter timer. When it down counts to 00 that will occur underflow and TM0F will be set to “1”. At this moment, the zero flag will not be affected. So, please read TM0F to judge whether it underflow or not.

```
MOVLA     81H
MOVAM     IRQM ; set Tmr0 irq enable ;
MOVLA     FFH
MOVAM     TMR0 ; Tmr0 from ffh down count to 00h ;
MOVLA     C1H ; b7:tmr0 enable, b6: pre-load enable,
                b5: sys-clk/4, b3: pre-scaler assign to Tmr0,
                b2-b0: pre-scaler=4
SELECT
```

6.3 Indirect Addressing

Register IAR($00) and BSR($04) will be used to address indirectly. BSR (Bank Select Register) allows 5-bit wide operand to directly access the whole data (00~3F) memory. The method is as below map:



WDT is a timer to prevent software from malfunction or jumping to an unknown location with unpredictable result. The source clock of WDT is an independent internal RC oscillator. This timer would be affected by temperature, voltage and different production lot. The minimum time is around 20ms. Programmer can use SELECT instruction to set prescaler and get the different duration.

6.5 Reset

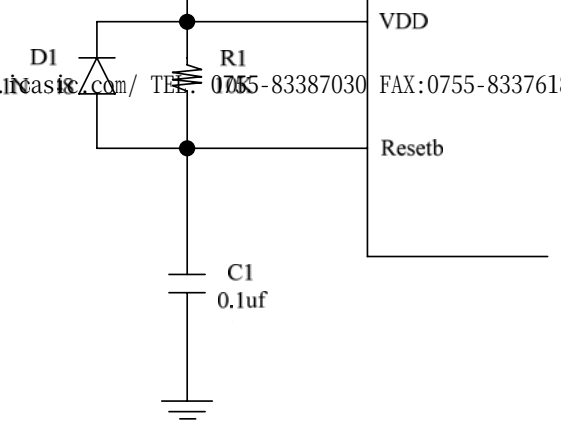
There are 4 events will cause reset which is listed as below. The power-down event will cause DL7503 reset. This condition is used to protect chip in deficient power environment. The last two cases are called warm reset. Different reset events will affect registers and RAM. The $\overline{TO}$ and $\overline{PD}$ bits can be used to determine the type of reset.

(1) Power-on reset.

(2) Low voltage reset (LVR).

(3) RESETB pin reset (input a negative pulse).

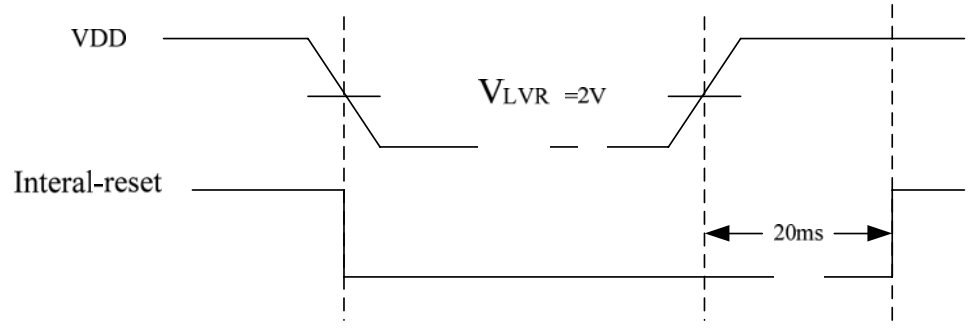
(4) WDT timer overflow reset.



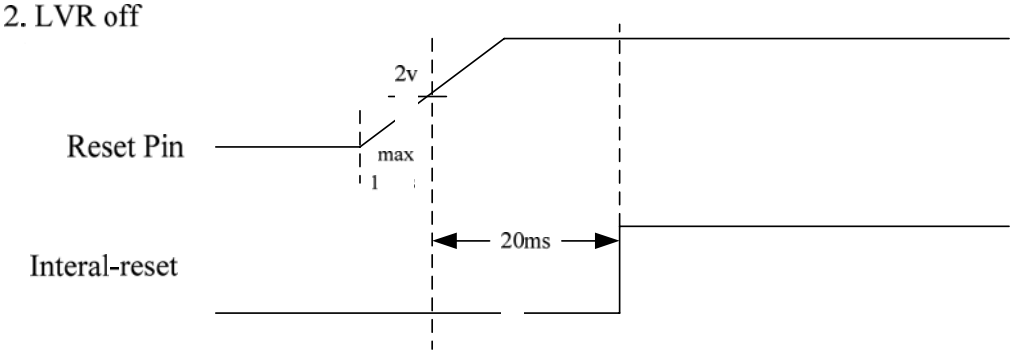
Reset Circuit

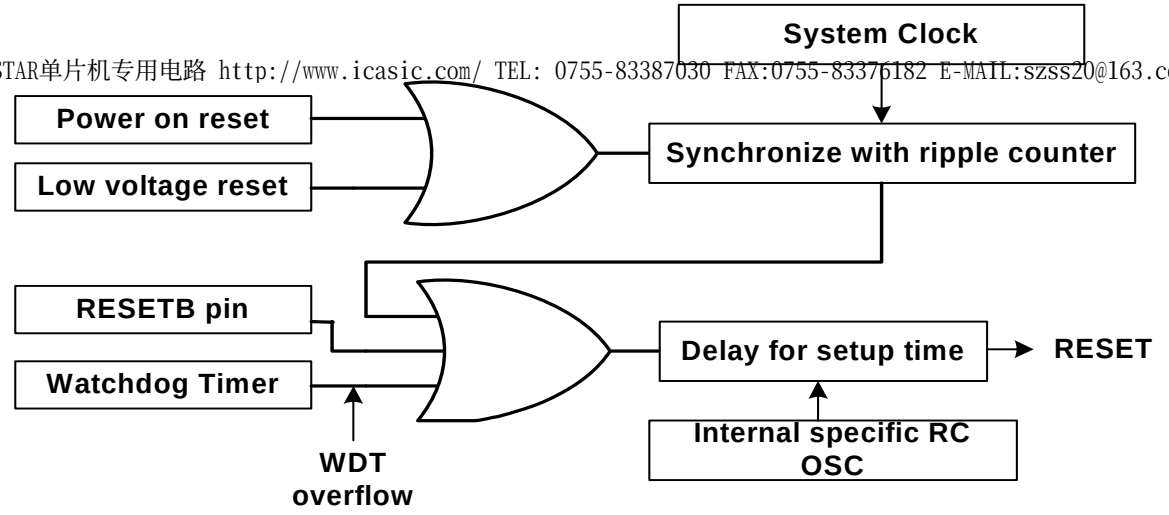
Timming :

1. LVR on



2. LVR off





System Reset Block

<Note>: the watchdog setup time is approximately 20ms that will has some tolerance due to power voltage, process and temperature variations.

Address	Name		Cold Reset	Warm Reset
N/A	Accumulator		xxxx xxxx	pppp pppp
N/A	IODIR	PB	1111 1111	1111 1111
		PA	1111	1111
N/A	SELECT		0100 0000	0100 0000
00h	IAR		---- ----	---- ----
01h	TMR0		xxxx xxxx	pppp pppp
02h	PCL		11 1111 1111	11 1111 1111
03h	STATUS		0001 1xxx	#00# #ppp
04h	BSR		1xxx xxxx	1ppp pppp
09h	IRQM		0000 0000	0000 0000
0Ah	IRQF		0000 0000	0000 0000
0Bh	PA_PDM		xxxx 0000	xxxx 0000
0Ch	PB_PUP		0000 x000	0000 x000
0Dh	PB_PDM		00xx x000	00xx x000
0Eh	PB_POD		0000 x000	0000 x000
0Fh	WAKEUP		0000 x000	0000 x000
10h~3Fh	General Purpose RAM		xxxx xxxx	pppp pppp

<Note> x: unknown; p: keep as previous data ; #: value depends on condition

-:unimplemented and read as"0".

6.5.1 Reset condition of STATUS register

Condition	Status Register	
	$\overline{TO}$	$\overline{PD}$
1.Power-on reset	1	1
2.RESETB reset during normal operation<Note 3>	U	U
3.RESETB reset during sleep <Note 3>	1	0
4.WDT reset during sleep	0	0
5.WDT reset during normal operation	0	1
6.Wake up by pin changed	1	0

<Note> 1. If execute CLRWDT then the content of item 4,5 would not be as the above.

2. U: Unchanged

3. The data of $\overline{TO}$ and $\overline{PD}$ is as the table only when reset and PSA bit (SELECT register) was set to "1". If PSA doesn't set to "1", the data after reset is not as table.

6.6 Interrupt

The DL7503 provides 2 interrupts which are TMR0 and external INT. IRQM and IRQF registers are used to control or declare request state of all interrupts. IRQM is used to enable/disable interrupt and IRQF is used to indicate which interrupt is occurred. If the specific IRQM doesn't enable then the hardware interrupt would not occurred. But the IRQF will response the status no matter how IRQM enable or not. For example, user enable TMR0 to start counting. If IRQM bit 0 is enabled, the hardware interrupt would generate when timer overflow and IRQF bit 1 will be set. At the same time, program will jump to interrupt vector. User should clear IRQF in interrupt service routine, otherwise the interrupt would not work properly. Another condition is if IRQM bit 0 is disabled, the interrupt would not generate when timer overflow, but IRQF bit 1 still will be set. Program would not jump to interrupt vector.

A. IRQM ($09H)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQM	INTM	--	--	--	--	--	PB0M	TM0M

- Bit7 (INTM): Global enable bit.

  0: Disable. All interrupts are mask.

  1: Enable. All interrupt are unmask

  When interrupt is serving, the INTM will reset to "0" to prevent the other interrupt happen. After served, the IRETI instruction will set INTM as '1'.

- Bit1 (PB0M): external INT pin interrupt enable/disable

  0: Disable Interrupt

- Bit0 (TM0M): TMR0 interrupt enable/disable

  0: Disable Interrupt

  1: Enable Interrupt

B. IRQF ($0AH)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQF	--	--	--	--	--	--	PB0F	TM0F

- Bit1 (PB0F): external INT pin interrupt flag

  0: Interrupt signal doesn't occurred

  1: Interrupt signal occurred

- Bit0 (TM0F): TMR0 interrupt flag

  0: Timer overflow doesn't occurred

  1: Timer overflow occurred

6.7 STATUS Register

The STATUS register is an 8-bit register that contains the zero flag (Z), carry flag (C), Nibble carry flag (DC), power down flag ($\overline{PD}$), and watchdog timer overflow flag ($\overline{TO}$). It records the status information.

A. STATUS($03H)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STATUS	**--**	**--**	**BS**	$\overline{TO}$	$\overline{PD}$	**Z**	**DC**	**C**

- Bit5 (BS) : Bank select

  0 (init) : Bank0 (000H ~ 1FFH).

  1 : Bank1 (200H ~ 3FFH).

- Bit4 ($\overline{TO}$): Timer overflow flag bit
- Bit3 ($\overline{PD}$):Power down flag bit

$\overline{TO}$	$\overline{PD}$	Description
0	0	WDT timer overflow from sleep mode
0	1	WDT timer overflow from normal mode
1	0	Input a 'low" at RESETB from sleep mode
1	1	Power on reset
Unchanged	Unchanged	Input a "low" at RESETB from normal mode

- Bit2 (Z): zero flag bit

  0: the result of a logic operation is not zero

  1: the result of a logic operation is zero

- Bit1 (DC): Nibble Carry and Nibble $\overline{Borrow}$ flag bit

  ADD instruction:

  0: no carry

  1: a carry from the low nibble bits of the result occurred

  SUB instruction

1: no borrow

- Bit0 (C): Carry and $\overline{Borrow}$ flag bit

ADD instruction:

0: no carry

1: a carry occurred from the MSB

SUB instruction

0: a borrow occurred from the MSB

1: no borrow

6.8 Wake up function

a. pin change wake_up

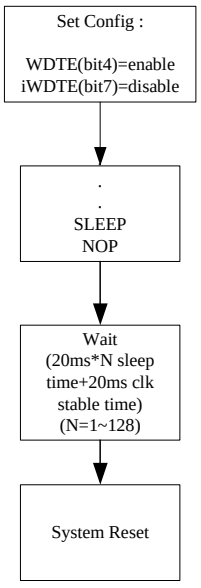
The chip provide pin signal toggle wake up function. It will return from sleep mode when signal toggle in input port. In order to safely wake up from sleep mode, we suggest to read the input pin to store data before entering sleep mode. The sample program is as below:

```
MOVLA       FFh
IODIR       PORTB       ;// set bit0~7 of port B as input. Only input pin can be wake up
……          ……..
MOV         PORTB,a     ;//Store the data of input pin before sleep
BS          WAKEUP,0    ;//Set PB0 is wakeup pin
SLEEP                   ;// if doesn't perform the read instruction, then can not enter
                        ;// SLEEP mode
NOP                     ;//Add NOP instruction to delay a while when chi
```

b. i_WDT wake_up

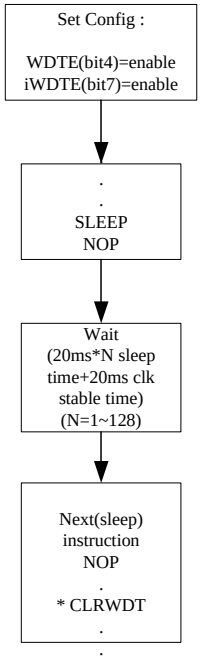
The chip provide internal watch dog (i_WDT) wake up function. It will return from sleep mode when watch dog timer overflow. In order to safely wake up from sleep mode, this wake up mode must set two config bit enable i_WDT (bit7), WDTE(bit4). At this stage, bit 7 (EN7) of register WAKEUP ($0FH) will be inhibited. The setting flow of i_WDT is as below:

WDT-Wakeup :
(Watch-dog timer wake-up)




```
start
        clrwdt
        movla   0Fh
        select  ;set prescaler for WDT
                & prescaler=128
          .
          .
          .
        Sleep
         nop
System reset
```

I_WDT-Wakeup :
(Internal watch-dog timer wake-up)



*When wakeup must CLRWDT, otherwise watch-dog timer will keep operation

```
start
        clrwdt
        movla   0fh
        select  ;set prescaler for WDT
                & prescaler=128
          .
          .
          .
        Sleep
         nop
        clrwdt
          .
          .
          .
```

<Note> Instruction cycle is system clock/4

Mnemonic Operands	Instruction Code (Advance)	Cycles	Status Affected	**OP-code**
ADD M, m	(M)+(acc) → (M)	1	C, DC, Z	01 0101 1MMM MMMM
ADD M, a	(M)+(acc) → (acc)	1	C, DC, Z	01 0101 0MMM MMMM
AND M, m	(M) · (acc) → (M)	1	Z	01 0100 1MMM MMMM
AND M, a	(M) · (acc) → (acc)	1	Z	01 0100 0MMM MMMM
ANDLA I	Literal · (acc) → (acc)	1	Z	11 1001 iiii iiii
BC M, b0	Clear bit0 of (M)	1	None	00 1100 0MMM MMMM
BC M, b1	Clear bit1 of (M)	1	None	00 1100 1MMM MMMM
BC M, b2	Clear bit2 of (M)	1	None	00 1101 0MMM MMMM
BC M, b3	Clear bit3 of (M)	1	None	00 1101 1MMM MMMM
BC M, b4	Clear bit4 of (M)	1	None	00 1110 0MMM MMMM
BC M, b5	Clear bit5 of (M)	1	None	00 1110 1MMM MMMM
BC M, b6	Clear bit6 of (M)	1	None	00 1111 0MMM MMMM
BC M, b7	Clear bit7 of (M)	1	None	00 1111 1MMM MMMM
BS M, b0	Set bit0 of (M)	1	None	00 1000 0MMM MMMM
BS M, b1	Set bit1 of (M)	1	None	00 1000 1MMM MMMM
BS M, b2	Set bit2 of (M)	1	None	00 1001 0MMM MMMM
BS M, b3	Set bit3 of (M)	1	None	00 1001 1MMM MMMM
BS M, b4	Set bit4 of (M)	1	None	00 1010 0MMM MMMM
BS M, b5	Set bit5 of (M)	1	None	00 1010 1MMM MMMM
BS M, b6	Set bit6 of (M)	1	None	00 1011 0MMM MMMM
BS M, b7	Set bit7 of (M)	1	None	00 1011 1MMM MMMM
BTSC M, b0	If bit0 of (M) = 0, skip next instruction	1 + (skip)	None	00 0100 0MMM MMMM
BTSC M, b1	If bit1 of (M) = 0, skip next instruction	1 + (skip)	None	00 0100 1MMM MMMM
BTSC M, b2	If bit2 of (M) = 0, skip next instruction	1 + (skip)	None	00 0101 0MMM MMMM
BTSC M, b3	If bit3 of (M) = 0, skip next instruction	1 + (skip)	None	00 0101 1MMM MMMM
BTSC M, b4	If bit4 of (M) = 0, skip next instruction	1 + (skip)	None	00 0110 0MMM MMMM
BTSC M, b5	If bit5 of (M) = 0, skip next instruction	1 + (skip)	None	00 0110 1MMM MMMM

BTSC M, b7	If bit7 of (M) = 0, skip next instruction	1 + (skip)	None	00 0111 1MMM MMMM
BTSS M, b0	If bit0 of (M) = 1, skip next instruction	1 + (skip)	None	00 0000 0MMM MMMM
BTSS M, b1	If bit1 of (M) = 1, skip next instruction	1 + (skip)	None	00 0000 1MMM MMMM
BTSS M, b2	If bit2 of (M) = 1, skip next instruction	1 + (skip)	None	00 0001 0MMM MMMM
BTSS M, b3	If bit3 of (M) = 1, skip next instruction	1 + (skip)	None	00 0001 1MMM MMMM
BTSS M, b4	If bit4 of (M) = 1, skip next instruction	1 + (skip)	None	00 0010 0MMM MMMM
BTSS M, b5	If bit5 of (M) = 1, skip next instruction	1 + (skip)	None	00 0010 1MMM MMMM
BTSS M, b6	If bit6 of (M) = 1, skip next instruction	1 + (skip)	None	00 0011 0MMM MMMM
BTSS M, b7	If bit7 of (M) = 1, skip next instruction	1 + (skip)	None	00 0011 1MMM MMMM
CLRA	Clear accumulator	1	Z	01 0001 0000 0000
CLR M	Clear memory M	1	Z	01 0001 1MMM MMMM
CLRWDT	Clear watch-dog register	1	TO, PO	01 0000 0000 0001
COM M, m	~(M) → (M)	1	Z	01 0010 1MMM MMMM
COM M, a	~(M) → (acc)	1	Z	01 0010 0MMM MMMM
DEC M, m	Decrement M to M	1	Z	01 0110 1MMM MMMM
DEC M, a	(M) - 1 → (acc)	1	Z	01 0110 0MMM MMMM
DECSZ M, m	(M) - 1 → (M), skip if (M) = 0	1 + (skip)	None	01 0111 1MMM MMMM
DECSZ M, a	(M) - 1 → (acc), skip if (M) = 0	1 + (skip)	None	01 0111 0MMM MMMM
INC M, m	(M) + 1 → (M)	1	Z	01 1000 1MMM MMMM
INC M, a	(M) + 1 → (acc)	1	Z	01 1000 0MMM MMMM
INCSZ M, m	(M) + 1 → (M), skip if (M) = 0	1 + (skip)	None	01 1001 1MMM MMMM
INCSZ M, a	(M) + 1 → (acc), skip if (M) = 0	1 + (skip)	None	01 1001 0MMM MMMM
IODIR M	Set i/o direction	1	None	01 0000 0000 0MMM
IOR M, m	(M) ior (acc) → (M)	1	Z	01 1111 1MMM MMMM
IOR M, a	(M) ior (acc) → (acc)	1	Z	01 1111 0MMM MMMM
IORLA I	Literal ior (acc) → (acc)	1	Z	11 0011 iiii iiii
LCALL I	Call subroutine. However, LCALL can addressing 1K address	2	None	10 0iii iiii iiii
LGOTO I	Go branch to any address	2	None	10 1iii iiii iiii

MOVAM m	Move data form acc to memory	1	None	01 0000 1MMM MMMM
MOVLA I	Move literal to accumulator	1	None	11 0001 iiii iiii
MOV M, m	(M) → (M)	1	Z	01 0011 1MMM MMMM
MOV M, a	(M) → (acc)	1	Z	01 0011 0MMM MMMM
NOP	No operation	1	None	01 0000 0000 0000
RET	Return	2	None	11 1111 0111 1111
RETI	Return and enable INTM	2	None	11 1111 1111 1111
RETLA I	Return and move literal to accumulator	2	None	11 1100 iiii iiii
RL M, m	Rotate left from m to itself	1	C	01 1100 1MMM MMMM
RL M, a	Rotate left from m to acc	1	C	01 1100 0MMM MMMM
RR M, m	Rotate right from m to itself	1	C	01 1110 1MMM MMMM
RR M, a	Rotate right from m to acc	1	C	01 1110 0MMM MMMM
SELECT	Set select register	1	None	01 0000 0000 0010
SLEEP	Enter sleep (saving) mode	1	TO, PO	01 0000 0000 0011
SUB M, m	(M)–(acc) → (M)	1	C, DC, Z	01 1010 1MMM MMMM
SUB M, a	(M) –(acc) → (acc)	1	C, DC, Z	01 1010 0MMM MMMM
SWAP M, m	Swap data from m to itself	1	None	01 1101 1MMM MMMM
SWAP M, a	Swap data from m to acc	1	None	01 1101 0MMM MMMM
XOR M, m	(M) xor (acc) → (M)	1	Z	01 1011 1MMM MMMM
XOR M, a	(M) xor (acc) → (acc)	1	Z	01 1011 0MMM MMMM
XORLA I	Literal xor (acc) → (acc)	1	Z	11 1000 iiii iiii

<Note> After SLEEP instruction, please add a NOP instruction to perform transient.

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Supply Voltage …. Vss-0.3V to Vss+5.5V Storage Temperature ……. –40℃ to 125℃

Input Voltage …… Vss-0.3V to VDD+0.3V Operating Temperature …. 0℃ to 70℃

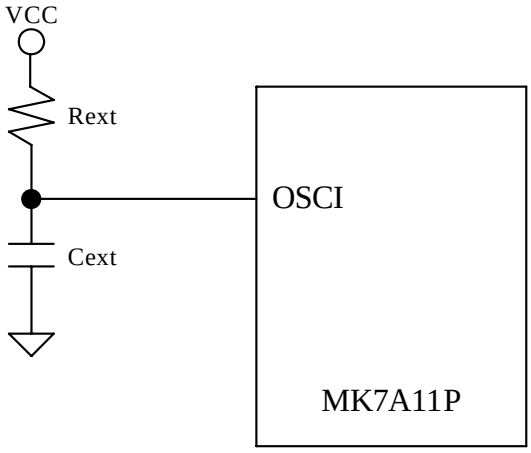
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD	Conditions				
VDD	Operating Voltage	---		2.2		5.5	V
V_{IH}	Input HighVoltage	5V	I/O Port	0.7VDD		VDD	V
V_{IL}	Input Low Voltage	5V	I/O Port	0		0.3VDD	V
I_{DD1}	Standby Current	5V	WDT disable,(LV ON)			3	μA
			WDT disable,(LV OFF)			1	
			WDT enable,(LV ON)			11	
			WDT enable, (LV OFF)			9	
		3V	WDT disable,(LV ON)			1	
			WDT disable,(LV OFF)			1	
			WDT enable,(LV ON)			2	
			WDT enable,(LV OFF)			2	
I_{DD1}	operating current	5V	reset=hi, Fosc=4MHZ, No Load		2		mA
I_{IL}	Input Leakage Current	5V	Vin=VDD, VSS			1	μA
I_{OH}	output high driving current	5V	Voh=0.9V_{DD}		-9		mA
		3V	Voh=0.9V_{DD}		-4		mA
I_{OL}	output low sink current	5V	Vol=0.1V_{DD}		20		mA
		3V	Vol=0.1V_{DD}		8		mA
V_{LV}	Low Voltage reset (LVR)			1.9	2.1	2.2	V

R_{PH}	Pull-high Resistance	3V		80	100	120	KΩ
		5V		30	50	70	KΩ
R_{PL}	Pull-low Resistance	3V		50	65	80	KΩ
		5V		25	35	45	KΩ

7.3 AC Characteristics

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
		Conditions	VDD				
f_{sys1}	System Clock	LP Crystal mode	5V	32		200	Khz
			3V	32		200	
f_{sys2}	System Clock	NT Crystal mode	5V	0.2		10	Mhz
			3V	0.2		10	
f_{sys3}	System Clock	HS Crystal mode	5V	10		20	Mhz
f_{sys4}	System Clock	RC mode	5V	3.4	4	4.6	Mhz
			3V	3.4	4	4.6	
T_{wdt}	Watchdog Timer		5V		20		MS
			3V		24		MS
T_{PRT1}	Power On Reset Time	RES_T=1 (config b7)	5V		20		MS
			3V		24		MS
T_{PRT2}	Power On Reset Time	RES_T=0 (config b7)	5V		650		us
			3V		800		us

7.4 EXT RC Oscillator Frequencies



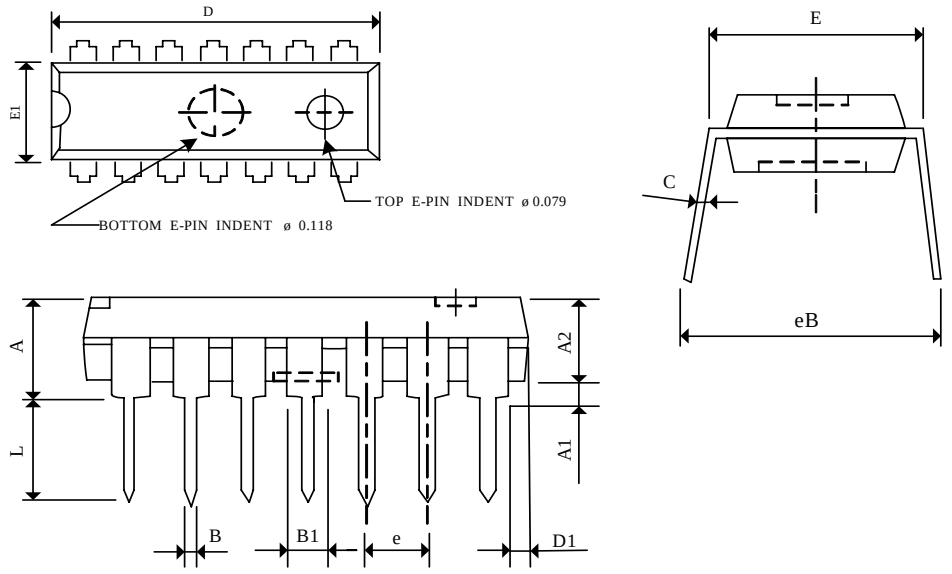
The typical external RC oscillation frequency is as below table

When Cext = 0.01uf (103)

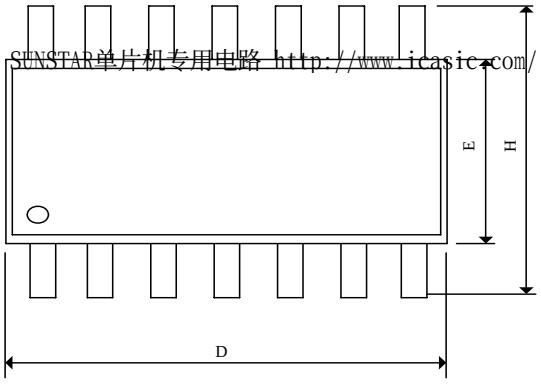
Rext	5V	3V
215K	500 KHZ	435 KHZ
105K	1.0 MHZ	0.95 MHZ
55K	2.0 MHZ	1.9 MHZ
30K	4.0 MHZ	3.95 MHZ
16K	8.0 MHZ	7.7 MHZ
14K	10.0 MHZ	9.0 MHZ

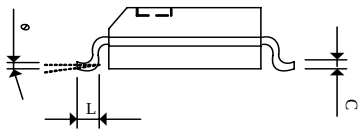
8. Package Dimension

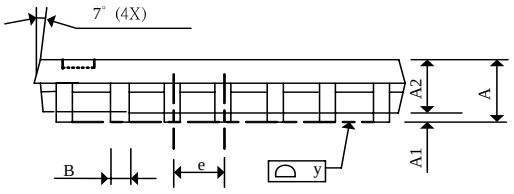
(a) 14 Pin DIP



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	4.57	—	—	0.180
A1	0.38	—	—	0.015	—	—
A2	3.25	3.30	3.45	0.128	0.130	0.136
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.27	1.52	1.78	0.050	0.060	0.070
C	0.20	0.25	0.33	0.008	0.010	0.013
D	18.90	19.15	19.30	0.744	0.754	0.760
D1	1.07	1.19	1.32	0.042	0.047	0.052
E	7.62	—	8.26	0.300	—	0.325
E1	6.35	6.50	6.65	0.250	0.256	0.262
e	—	2.54	—	—	0.100	—
L	3.18	—	—	0.125	—	—
eB	8.64	—	9.65	0.340	—	0.380







SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.60	1.75	0.053	0.063	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
B	0.33	—	0.51	0.013	—	0.020
C	0.19	—	0.25	0.007	—	0.010
D	8.55	—	8.75	0.337	—	0.344
E	3.80	—	4.00	0.150	—	0.157
e	—	1.27	—	—	0.050	—
H	5.80	—	6.20	0.228	—	0.244
L	0.40	—	1.27	0.016	—	0.050
Y	—	—	0.10	—	—	0.004
θ	0°	—	8°	0°	—	8°

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