ISD1900

SINGLE-CHIP, MULTIPLE-MESSAGE

VOICE RECORD/PLAYBACK DEVICE

TABLE OF CONTENTS

1. GENERAL DESCRIPTION

Nuvoton's ISD1900 ChipCorder® Series is a single-chip multiple-message record/playback device with dual operating modes and wide operating voltage ranging from 2.4V to 5.5V. The sampling frequency can be selected from 4 to 12 kHz via an external resistor, which also determines the duration. The device is designed for mostly standalone applications, and of course, it can be manipulated by a microcontroller, if necessary.

The two operating modes are Address Mode and Direct Mode. While in Address Mode, both record and playback operations are manipulated according to the start address and end address specified through the start address and end address pins. In Direct Mode, the device can configure the memory up to as many as eight similar duration messages, pending upon the fixed message configuration settings. With the record or playback feature being pre-selected, each message can be randomly accessed via its message control pin.

The device has a selectable differential microphone input with AGC feature or single-ended analog input, AnaIn, under feed-through mode. The audio output is either a differential Class-D PWM direct-drive or a single-ended voltage output (AUX out), depending on the derivative selected.

2. FEATURES

The ISD1900 is a multiple messages record/playback device with two operational modes: Address Mode and Direct Mode.

- Supply voltage: 2.4V to 5.5V.
- External resistor, Rosc, selects sampling frequency and duration.

Sampling Frequency	12 kHz	8 kHz	6.4 kHz	5.3 kHz	4 kHz
Rosc	53.3 KΩ	80 KΩ	100 KΩ	120 KΩ	160 KΩ
ISD1916	10.6 sec	16 sec	20 sec	24 sec	32 sec
ISD1932	21.3 sec	32 sec	40 sec	48 sec	64 sec
ISD1964	42.6 sec	64 sec	80 sec	96 sec	128 sec

- Mic+/Mic-: differential microphone inputs.
- AGC: automatic gain control for microphone preamp circuit.
- $\overline{FT}$: feed-through the AnaIn signal to the speaker outputs while AnaIn is converted from MIC+.
- When both $\overline{FT}$ and recording are active, device will record AnaIn signal into memory with AnaIn signal output to speaker simultaneously.
- SP+/SP-: Class-D PWM differential speaker drivers or single-ended voltage output, depending on the derivative selected.
- $\overline{LED}$: LED is on during recording.
- Automatically power down after each operation cycle.
- Playback takes precedence over the recording operation.
- Temperature option: -40°C to +85°C (Industrial)
- Packaging: available in SOIC only

2.1. ADDRESS MODE

- While in Address Mode, flexible message duration is defined by start address and end address.
- Utilize four start address pins (S0, S1, S2 & S3) and four end address pins (E0, E1, E2 & E3) to specify the message duration.
- $\overline{\text{REC}}$: Level-hold or Edge-trigger (toggle on-off) recording from start to end addresses.
- $\overline{\text{PlayE}}$: Edge-trigger playback from start to end address and stops at EOM marker, if EOM is prior to end address. Toggle on-off.
- $\overline{\text{PlayL}}$: Level-hold playback from start to end address. Also, if constantly Low, device will loop playback from start to end address.

2.2. DIRECT MODE

- While Direct Mode is active, utilizing the configuration pins, FMC1**,** FMC2 & FMC3, to define up to eight similar duration messages for random access.
- The control pins are: $\overline{\text{M1}}$ ~ $\overline{\text{M8}}$ (message activation) and $\overline{\text{R}}$/P (record or playback selection).
- The record or playback operation is pre-defined by the $\overline{\text{R}}$/P pin.
- Each message can be randomly accessed via its message control pin ($\overline{\text{M1}}$ ~ $\overline{\text{M8}}$) and the desired operation is facilitated accordingly.

3. BLOCK DIAGRAM

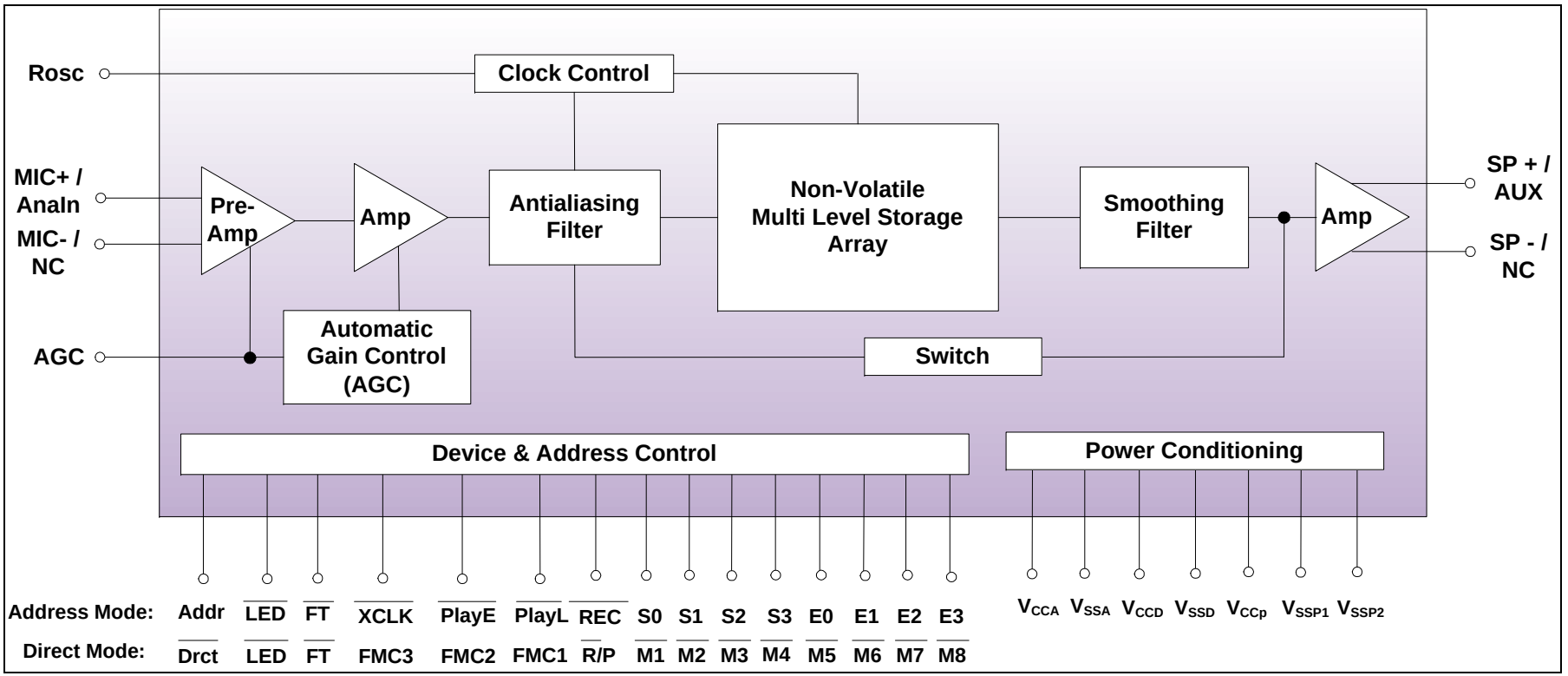


Figure 3-1 Block Diagram

4. PIN CONFIGURATION

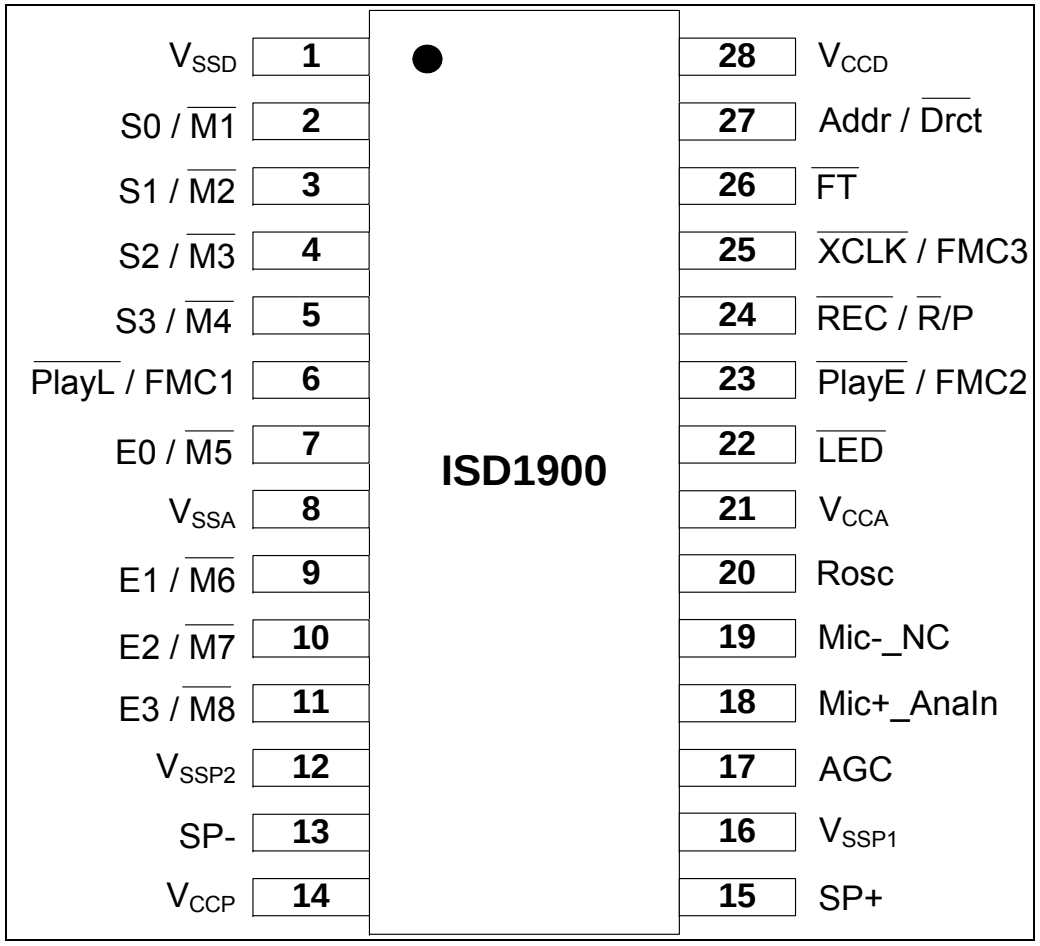


Figure 4-1 Pin Configuration

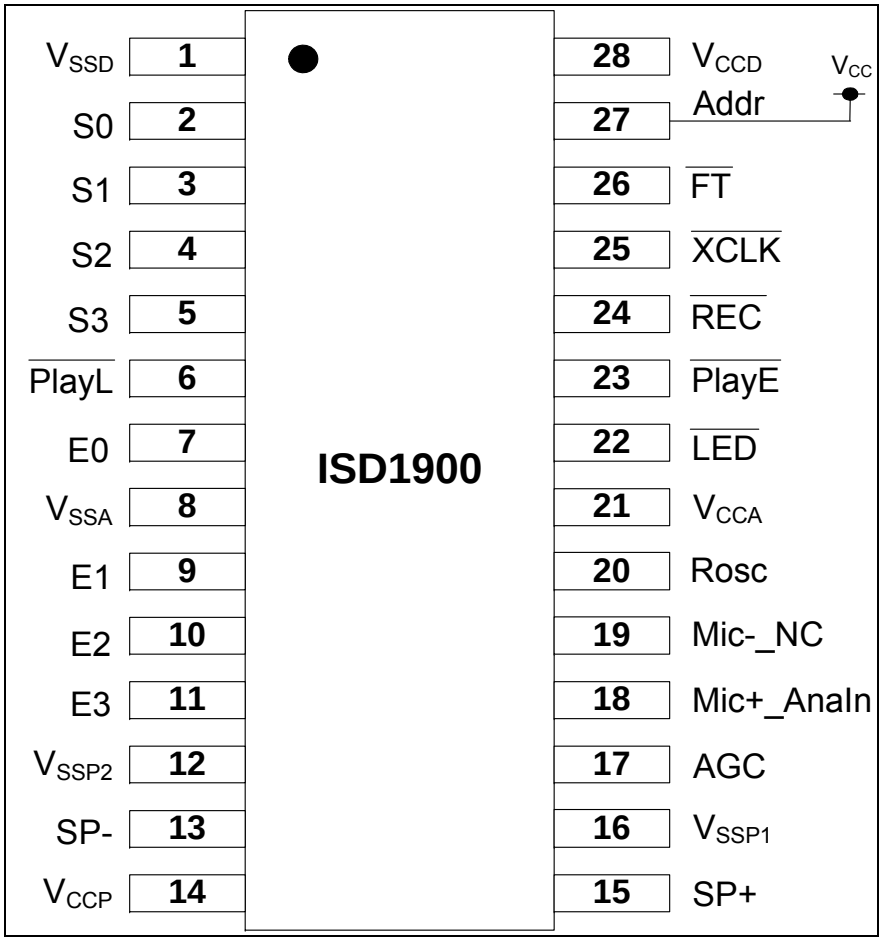


Figure 4-2 Pin Configuration – Address Mode

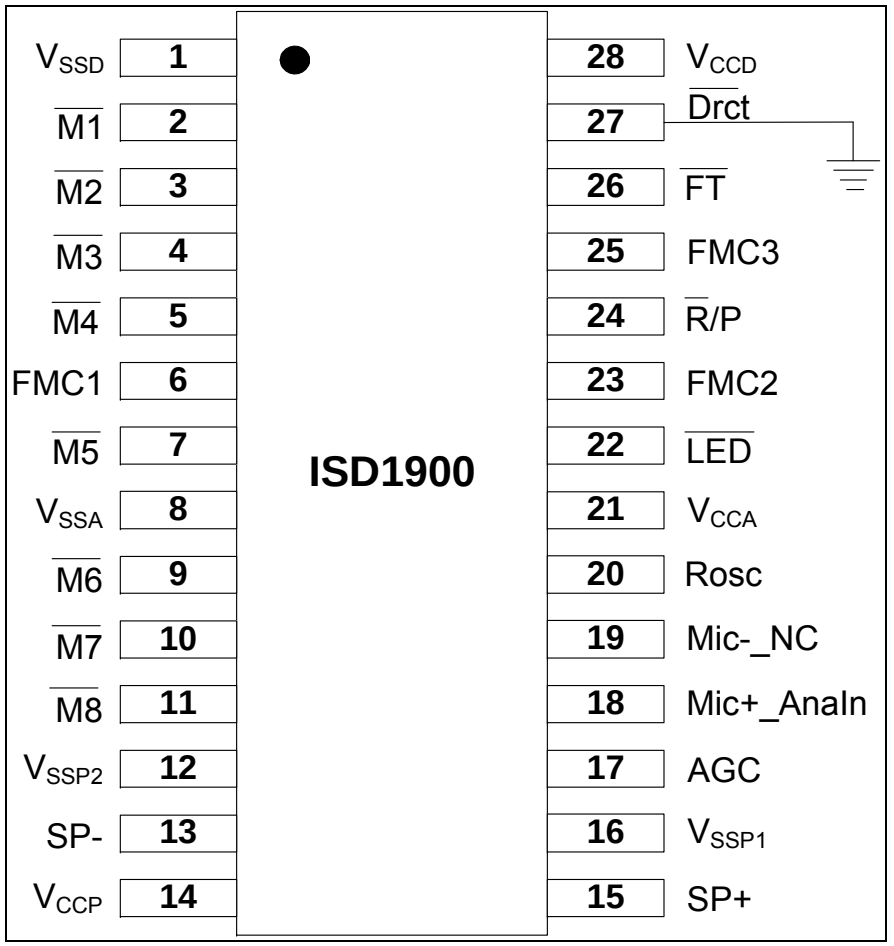


Figure 4-3 Pin Configuration – Direct Mode

5. PIN DESCRIPTION

PIN NAME	PIN #	I / O	FUNCTION
V_{SSD}	1	I	Digital Ground: Ground path for digital circuits.
S0/$\overline{M1}$	2	I	S0[1]: In Address Mode, Start Address Bit 0. $\overline{M1}$: When Direct Mode is active, low active operation on 1st Message. Internal pull-up & debounce existed.
S1/$\overline{M2}$	3	I	S1[1]: In Address Mode, Start Address Bit 1. $\overline{M2}$: When Direct Mode is active, low active operation on 2nd Message. Internal pull-up & debounce existed.
S2/$\overline{M3}$	4	I	S2[1]: In Address Mode, Start Address Bit 2. $\overline{M3}$: When Direct Mode is active, low active operation on 3rd Message. Internal pull-up & debounce existed.
S3/$\overline{M4}$	5	I	S3[1]: In Address Mode, Start Address Bit 3. $\overline{M4}$: When Direct Mode is active, low active operation on 4th Message. Internal pull-up & debounce existed.
$\overline{PlayL}$/FMC1	6	I	$\overline{PlayL}$: In Address Mode, low active input, Level-hold playback start to end addresses, debounce & internal pull-up existed. Holding $\overline{PlayL}$ Low constantly will perform looping playback function from start to end addresses with insignificant dead time between messages regardless of sampling frequencies. FMC1: When Direct Mode is active, FMC1, together with FMC2 & FMC3, setup various fixed-message configurations.
E0/$\overline{M5}$	7	I	E0[1]: In Address Mode, End Address Bit 0. $\overline{M5}$: When Direct Mode is active, low active operation on 5th Message. Internal pull-up & debounce existed.
V_{SSA}	8	I	Analog Ground: Ground path for analog circuits.
E1/$\overline{M6}$	9	I	E1[1]: In Address Mode, End Address Bit 1. $\overline{M6}$: When Direct Mode is active, low active operation on 6th Message. Internal pull-up & debounce existed.
E2/$\overline{M7}$	10	I	E2[1]: In Address Mode, End Address Bit 2. $\overline{M7}$: When Direct Mode is active, low active operation on 7th Message. Internal pull-up & debounce existed.
E3/$\overline{M8}$	11	I	E3[1]: In Address Mode, End Address Bit 3. $\overline{M8}$: When Direct Mode is active, low active operation on 8th Message. Internal pull-up & debounce existed.
V_{SSP2}	12	I	Ground: Ground for negative PWM speaker driver.
SP-	13	O	SP-: Negative signal of the differential Class-D PWM speaker outputs. This output, together with the SP+, is used to drive an 8Ω speaker directly.
V_{CCP}	14	I	Speaker Power Supply: Power supply for PWM speaker drivers.

PIN NAME	PIN #	I / O	FUNCTION
SP+	15	O	Depending on the derivative selected, it could be: SP+: Positive signal of the differential Class-D PWM speaker outputs. This output, together with the SP-, is used to drive an 8Ω speaker directly. Or, AUX out: single-ended voltage output.
V_{SSP1}	16	I	Ground: Ground for positive PWM speaker driver.
AGC	17	I	Automatic Gain Control (AGC): The AGC adjusts the gain of the preamplifier dynamically to compensate for the wide range of microphone input levels. The AGC allows the full range of signals to be recorded with minimal distortion. The AGC is designed to operate with a nominal capacitor of 4.7 µF connected to this pin. Connecting this pin to ground (V_{SSA}) provides maximum gain to the preamplifier circuitry. Conversely, connecting this pin to the power supply (V_{CCA}) provides minimum gain to the preamplifier circuitry.
MIC+ / AnaIn	18	I	MIC+: Non-inverting input of the differential microphone signal. AnaIn: When $\overline{FT}$ is selected, the MIC+ input is configured to a single-ended input with 1Vp-p maximum input amplitude and feed-through to the speaker outputs.
MIC- / NC	19	I	MIC-: Inverting input of the differential microphone signal. While $\overline{FT}$ is enabled, MIC- pin is disabled and must be floated.
Rosc	20	I	Oscillator Resistor: Connect an external resistor from this pin to V_{SSA} to select the internal sampling frequency.
V_{CCA}	21	I	Analog Power Supply: Power supply for analog circuits.
$\overline{LED}$	22	O	LED output: During recording, this output is Low. Also, $\overline{LED}$ pulses Low momentarily at the end of playback.
$\overline{PlayE}$/FMC2	23	I	$\overline{PlayE}$: In Address Mode, low active input, edge-trigger playback from start to end addresses & toggle on-off. Debounce & internal pull-up existed. FMC2: When Direct Mode is active, FMC2, together with FMC1 & FMC3**,** setup various fixed-message configurations.
$\overline{REC}$/$\overline{R}$/P	24	I	$\overline{REC}$: In Address Mode, level-hold (after 1 sec holding) or edge-trigger (toggle on-off), low active, recording from start to end addresses. Debounce & internal pull-up existed. $\overline{R}$/P (When Direct Mode is active): • When $\overline{R}$/P is set to Low, level-hold record operation is selected. When $\overline{R}$/P is set to High, edge-trigger & toggle on-off playback operation is selected.
$\overline{XCLK}$/FMC3	25	I	External Clock: In Address Mode, low active and level-hold input. As $\overline{XCLK}$ activated, Rosc pin accepts external clock input signal, provided resistor at Rosc must be removed. Connecting this pin to High enables device running on internal clock via Rosc resistor. If not used, $\overline{XCLK}$ must be at high level. When Direct Mode is active, FMC3, together with FMC1 & FMC2**,** setup various fixed-message configurations.
$\overline{FT}$	26	I	Feed-Through: Low active input, Level-hold, debounce & Internal pull-up required. When $\overline{FT}$ is selected, the MIC+ input is configured to a single-ended input with 1Vp-p maximum input amplitude and feed-through to the speaker outputs.

<table>
<tr><th>PIN NAME</th><th>PIN #</th><th>I / O</th><th>FUNCTION</th></tr>
<tr><td>Addr/$\overline{\text{Drct}}$</td><td>27</td><td>I</td><td>Level-hold input.
Addr: When set to High, the device operates under Address Mode.

Level-hold input.
$\overline{\text{Drct}}$: When set to Low, the device operates under Direct Mode. The device reconfigures its pin definitions to fit various fixed-message configurations utilizing FMC1 , FMC2 & FMC3 pins as below table.
<table>
<tr><th>FMC3</th><th>FMC2</th><th>FMC1</th><th># of fixed messages</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>7</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>8</td></tr>
</table>
</td></tr>
<tr><td>V_{CCD}</td><td>28</td><td>I</td><td>Digital Power Supply: Power supply for digital circuits.</td></tr>
</table>

Notes: [1] : Address bits S0, S1, S2, S3, E0, E1, E2 & E3 are used to access the memory location.

6. FUNCTIONAL DESCRIPTION

There are two operational modes: Address Mode and Direct Mode. After a new condition is selected on Addr/$\overline{\text{Drct}}$, the power must be cycled to enable it.

6.1. ADDRESS MODE

The start address pins (S0, S1, S2 & S3) and end address pins (E0, E1, E2 & E3) are used to access the memory location and they can divide the memory into a maximum of 16 slots. They are defined as follows:

S3 (E3)	S2 (E2)	S1 (E1)	S0 (E0)	Row #	I1916 Duration [s]
0	0	0	0	0	0
0	0	0	1	8	1.0
0	0	1	0	16	2.0
0	0	1	1	24	3.0
0	1	0	0	32	4.0
0	1	0	1	40	5.0
0	1	1	0	48	6.0
0	1	1	1	56	7.0
1	0	0	0	64	8.0
1	0	0	1	72	9.0
1	0	1	0	80	10.0
1	0	1	1	88	11.0
1	1	0	0	96	12.0
1	1	0	1	104	13.0
1	1	1	0	112	14.0
1	1	1	1	120	15.0

S3 (E3)	S2 (E2)	S1 (E1)	S0 (E0)	Row #	I1932 Duration [s]
0	0	0	0	0	0
0	0	0	1	16	2.0
0	0	1	0	32	4.0
0	0	1	1	48	6.0
0	1	0	0	64	8.0
0	1	0	1	80	10.0
0	1	1	0	96	12.0
0	1	1	1	112	14.0
1	0	0	0	128	16.0
1	0	0	1	144	18.0
1	0	1	0	160	20.0
1	0	1	1	176	22.0
1	1	0	0	192	24.0
1	1	0	1	208	26.0
1	1	1	0	232	28.0
1	1	1	1	240	30.0

S3 (E3)	S2 (E2)	S1 (E1)	S0 (E0)	Row #	I1964 Duration [s]
0	0	0	0	0	0
0	0	0	1	32	4.0
0	0	1	0	64	8.0
0	0	1	1	96	12.0
0	1	0	0	128	16.0
0	1	0	1	160	20.0
0	1	1	0	192	24.0
0	1	1	1	224	28.0
1	0	0	0	256	32.0
1	0	0	1	288	36.0
1	0	1	0	320	40.0
1	0	1	1	352	44.0
1	1	0	0	384	48.0
1	1	0	1	416	52.0
1	1	1	0	464	56.0
1	1	1	1	480	60.0

Below is an example:

Given sampling rate set to 6.4 kHz, using the ISD1916 to record four messages: three messages of 2.5 seconds and one message of 12.5 seconds, then the memory can be assigned as follows:

	S3, S2, S1, S0	E3, E2, E1, E0
Message 1 (2.5 seconds)	0 0 0 0	0 0 0 1
Message 2 (2.5 seconds)	0 0 1 0	0 0 1 1
Message 3 (2.5 seconds)	0 1 0 0	0 1 0 1
Message 4 (12.5 seconds)	0 1 1 0	1 1 1 1

6.1.1 Record ($\overline{\text{REC}}$) Operation

- Low active input:
  - level-hold for level-trigger or
  - falling edge for edge-trigger with debounce required.
- For 8kHz sampling frequency, if $\overline{\text{REC}}$ is held at Low for a period equal to 1 sec or more, then level recording is activated. However, if $\overline{\text{REC}}$ is pulsed Low for less than 1 sec, then edge-trigger recording is initiated.
- For 6.4kHz sampling frequency, if $\overline{\text{REC}}$ is held at Low for a period equal to 1.25 sec or more, then level recording is activated. However, if $\overline{\text{REC}}$ is pulsed Low for less than 1.25 sec, then edge-trigger recording is initiated.
- Recording begins from the start address to end address and $\overline{\text{LED}}$ is on.
- Recording ceases whenever:
  - $\overline{\text{REC}}$ returns to High in level-hold mode or
  - a subsequent low-pulse appears while in edge-trigger mode or
  - when end address is reached.

- Then an EOM marker is written at the end of message. And $\overline{LED}$ is off.
- Then the device will automatically power down.

- This pin has an internal pull-up device.
- Once $\overline{REC}$ is active, input on $\overline{FT}$, Addr/$\overline{Drct}$, S0, S1, S2, S3, E0, E1, E2 or E3 is illegal.

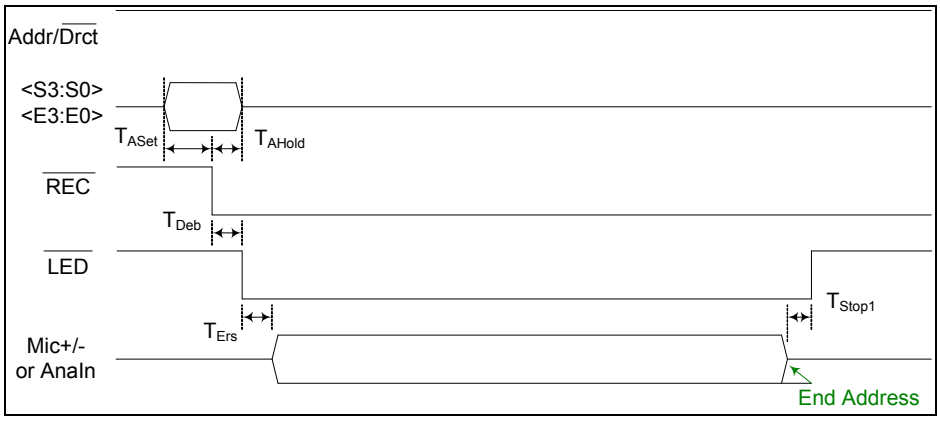


Figure 6-1 Record–Level ($\overline{REC}$) function till end address

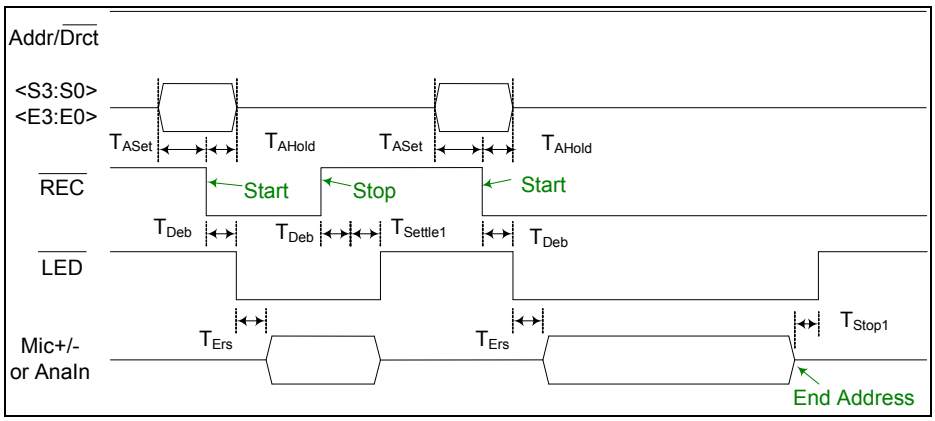


Figure 6-2 Record–Level ($\overline{REC}$) function with start and stop actions

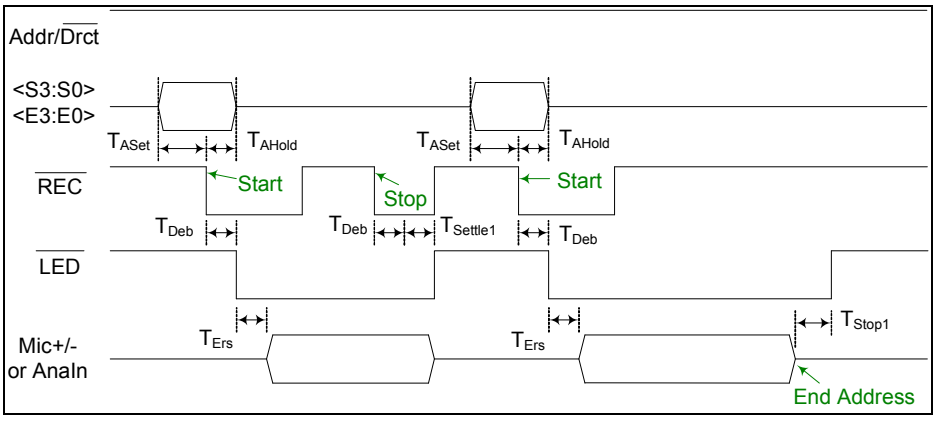


Figure 6-3 Record–Edge ($\overline{REC}$) function with on-off

6.1.2 Edge-triggered Playback (PlayE) Operation

- Low active input, edge-trigger, toggle on-off, debounce required.
- Playback begins from the start address to end address or EOM, whichever occurrs first.
- At the end of message, LED pulses Low momentarily.
  - Then device will automatically power down.
- During playback, a subsequent trigger terminates the playback operation. If EOM marker is not encountered, then LED will not pulses Low momentarily.
- This pin has an internal pull-up device.
- Once PlayE is active, input on PlayL, REC, FT, Addr/Drct, S0, S1, S2, S3, E0, E1, E2 or E3 is banned.

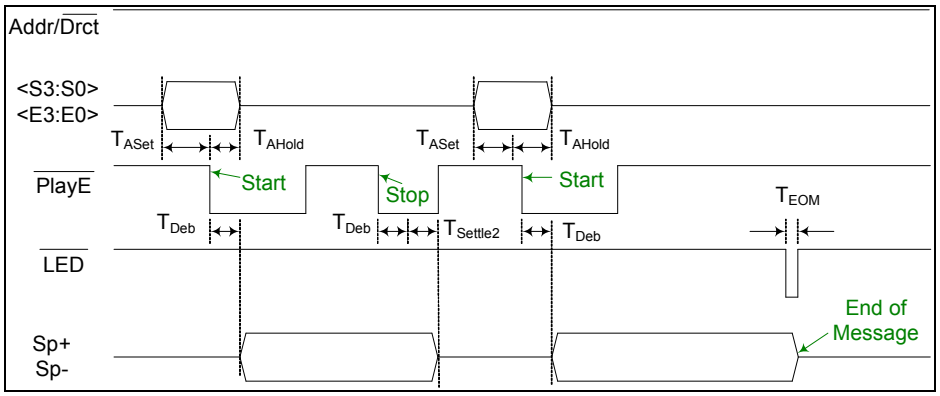


Figure 6-4 Playback–Edge (PlayE) function

6.1.3 Level-triggered Playback (PlayL) Operation

- Low active input, Level-hold, debounce required.
- Once active, playback begins from the start address and stops whenever PlayL returns to High. When an EOM is encountered, LED pulses Low momentarily.
  - Then device will automatically power down.
- This pin has an internal pull-up device.
- Once PlayL is active, input on PlayE, REC, FT, Addr/Drct, S0, S1, S2, S3, E0, E1, E2 or E3 is prohibited.

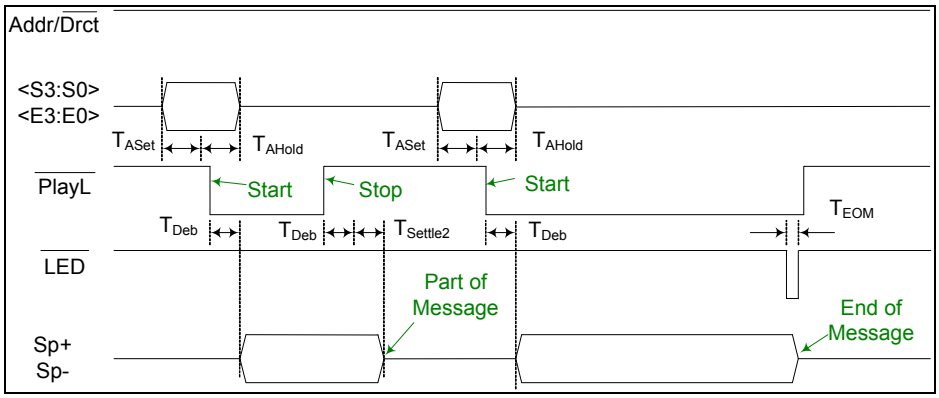


Figure 6-5 Playback–Level ($\overline{\text{PlayL}}$) function

- Holding $\overline{\text{PlayL}}$ Low constantly will perform looping playback function, without power down, from start address to end address.

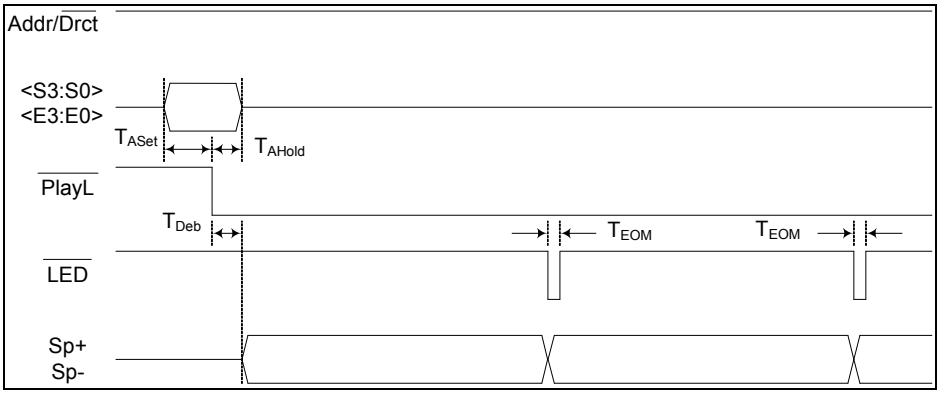


Figure 6-6 Looping playback function via $\overline{\text{PlayL}}$

6.1.4 Playback (Supersedes Record) Operation

- Playback takes precedence over the Recording operation.
- If either $\overline{\text{PlayE}}$ or $\overline{\text{PlayL}}$ is activated during a recording cycle, the recording immediately ceases with an EOM marker attached, and without power down, playback of the just-recorded message performs accordingly. Then device powers down.

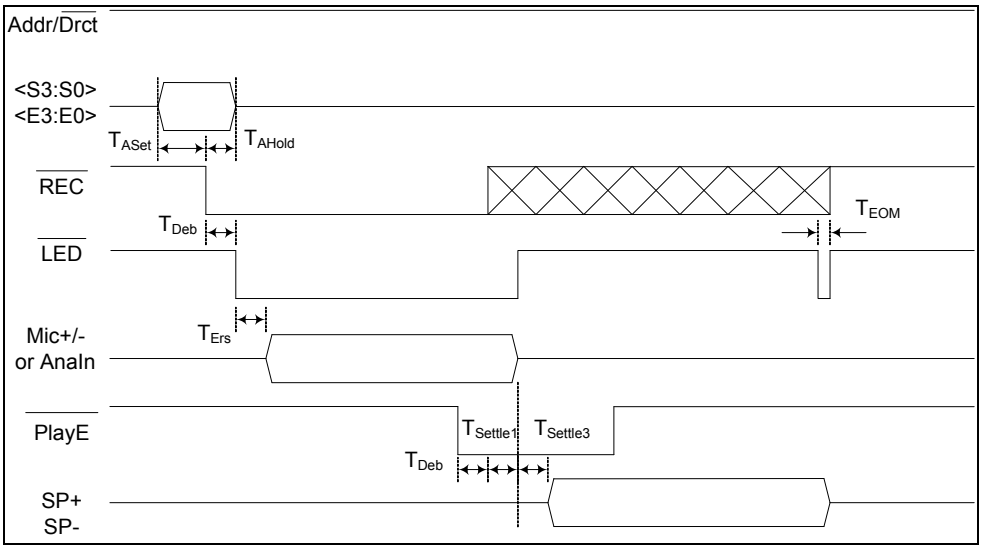


Figure 6-7 An example of Playback supersedes Record

6.1.5 XCLK Feature

- When precision sampling frequency is required, external clock mode can be activated by setting $\overline{XCLK}$ to Low. Under such condition, the resistor at Rosc pin must be removed and the external clock signal must be applied to the Rosc pin. These conditions must be satisfied prior to any operations.
- However, when internal clock is used, $\overline{XCLK}$ must be linked to High.
- The external clock frequencies required for various sampling frequencies are listed in below table.

Sampling Freq [kHz]	12	8	6.4	5.3	4
$\overline{XCLK}$ [MHz]	3.072	2.048	1.638	1.356	1.024

6.2. DIRECT MODE

- The Direct Mode is selected by the $\overline{Drct}$ pin. Once chosen, the supply voltage must be reset to allow the device to construct itself to the appropriate configuration by re-defining the function on the related control pins. Also, the mode change is only allowed while the device is in power down state and is inhibited when an operation is in progress.
- Once Direct Mode is activated, FMC1, FMC2 & FMC3 are utilized to select various (1 to 8) fixed message configurations [1]. Pending upon the arrangement on FMC1, FMC2 & FMC3, each divided message has approximate equal length of duration, which is related to the number of rows assigned as in tables below.
- The record or playback operation is pre-defined by the $\overline{R}$/P pin. Setting this pin to Low allows record operation while setting it to High enables playback operation.
- Each message can be randomly accessed via its message control pin ($\overline{M1}$ ~ $\overline{M8}$) and the desired operations are facilitated accordingly. Non-configured pins are automatically disabled and must be floated.

Notes: [1] : Number of fixed message arrangement with respect to FMC1, FMC2 & FMC3.

FMC3	FMC2	FMC1	**# of fixed messages [1]**
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

[2] : Number of memory **row arrangement** with respect to different number of fixed messages for ISD1916 (128 Rows). The non-configured Message control pins (Mx) will be disabled.

# of Msg	**M1**	**M2**	**M3**	**M4**	**M5**	**M6**	**M7**	**M8**
1	128							
2	64	64						
3	44	42	42					
4	32	32	32	32				
5	26	26	26	26	24			
6	23	21	21	21	21	21		
7	20	18	18	18	18	18	18	
8	16	16	16	16	16	16	16	16

for ISD1932 (256 Rows)

# of Msg	**M1**	**M2**	**M3**	**M4**	**M5**	**M6**	**M7**	**M8**
1	256							
2	128	128						
3	86	85	85					
4	64	64	64	64				
5	52	51	51	51	51			
6	43	43	43	43	42	42		
7	37	37	37	37	36	36	36	
8	32	32	32	32	32	32	32	32

for ISD1964 (512 Rows)

# of Msg	**M1**	**M2**	**M3**	**M4**	**M5**	**M6**	**M7**	**M8**
1	512							
2	256	256						
3	172	170	170					
4	128	128	128	128				
5	103	103	102	102	102			
6	86	86	85	85	85	85		
7	74	73	73	73	73	73	73	
8	64	64	64	64	64	64	64	64

[3] : The **durations** for various fixed message configurations on I1916 device at 8 kHz sampling frequency are shown in below table.

# of Msg	M1	M2	M3	M4	M5	M6	M7	M8
1	16							
2	8	8						
3	5.5	5.25	5.25					
4	4.0	4.0	4.0	4.0				
5	3.25	3.25	3.25	3.25	3.0			
6	2.875	2.625	2.625	2.625	2.625	2.625		
7	2.50	2.25	2.25	2.25	2.25	2.25	2.25	
8	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0

for ISD1932 (256 Rows)

# of Msg	M1	M2	M3	M4	M5	M6	M7	M8
1	32							
2	16	16						
3	10.75	10.625	10.625					
4	8.0	8.0	8.0	8.0				
5	6.5	6.375	6.375	6.375	6.375			
6	5.375	5.375	5.375	5.375	5.25	5.25		
7	4.625	4.625	4.625	4.625	4.5	4.5	4.5	
8	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.0

for ISD1964 (512 Rows)

# of Msg	M1	M2	M3	M4	M5	M6	M7	M8
1	64							
2	32	32						
3	21.5	21.25	21.25					
4	16.0	16.0	16.0	16.0				
5	12.875	12.875	12.75	12.75	12.75			
6	10.75	10.75	10.625	10.625	10.625	10.625		
7	9.25	9.125	9.125	9.125	9.125	9.125	9.125	
8	8.0	8.0	8.0	8.0	8.0	8.0	8.0	8.0

Example of four Fixed-Message Configuration:

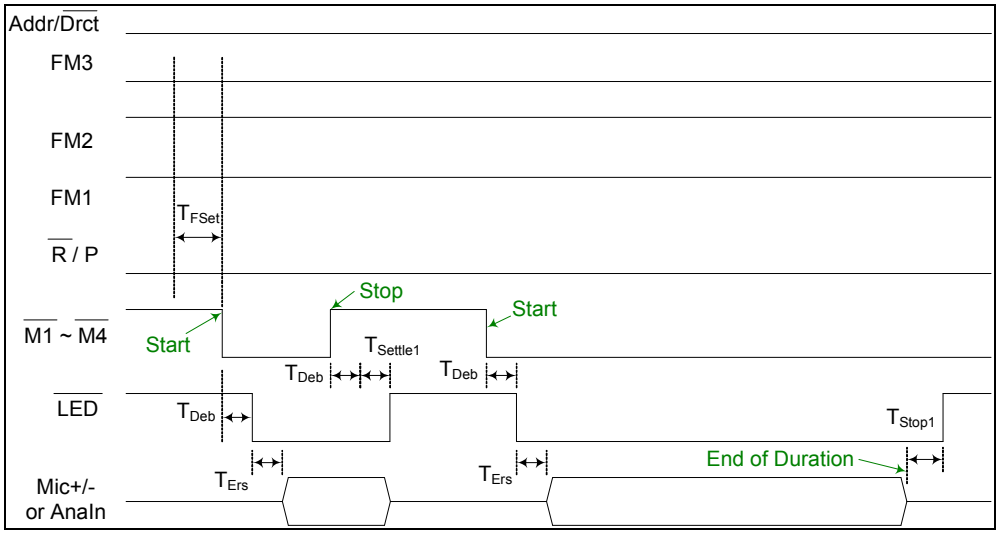


Figure 6-8 Record Operation under FMC mode

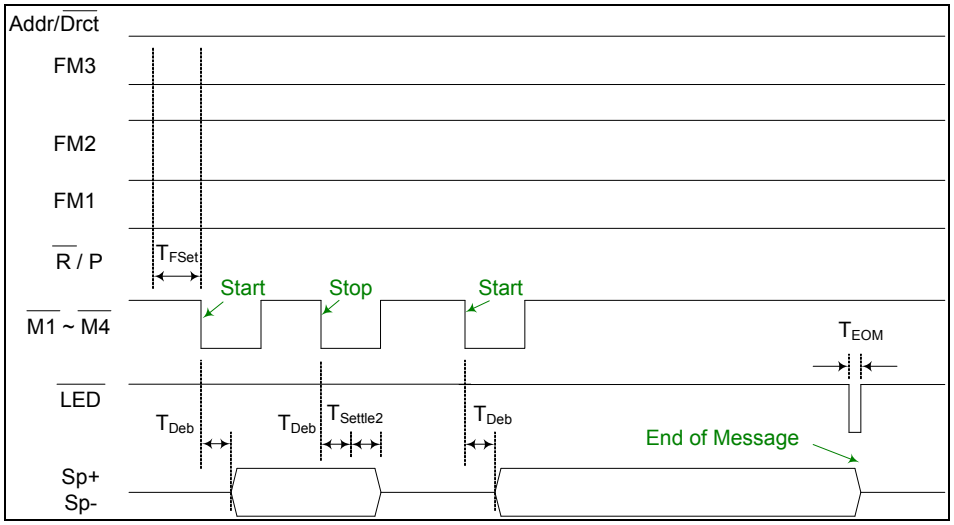


Figure 6-9 Playback Operation under FMC mode

6.3. OTHER OPERATIONS

6.3.1 Rosc Operation

- When the R_{OSC} varies from 53.3 KΩ to 160 KΩ, the sampling frequency changes from 12 to 4 kHz accordingly.
- When R_{OSC} resistor value is changed during playback, the tone of a recorded message will alter either faster or slower.
- If the ground side of R_{OSC} resistor is floated or tied to V_{CC}, then the current operation will be freezed.
- The operation will resume when the resistor is connected back to ground.

6.3.2 LED Operation

- $\overline{\text{LED}}$ turns on during recording. Also, $\overline{\text{LED}}$ pulses Low at the end of message. The Low period must be sufficiently greater than debounce time.

6.3.3 Feed-Through mode Operation

- As $\overline{\text{FT}}$ is held Low, the Mic+ pin will be reconfigured as AnaIn input, and the AnaIn signal will be transmitted to the speaker outputs. Under this mode, Mic- pin is not used (must be floated).
- After $\overline{\text{FT}}$ is enabled, If $\overline{\text{REC}}$ is triggered, then AnaIn signal will be recorded into memory while the Feed-Through path remains on.
- If $\overline{\text{FT}}$ is already enabled, activating either $\overline{\text{PlayE}}$ or $\overline{\text{PlayL}}$ will first disable the FT path and then play the recorded message. Once playback completes, FT path will be resumed.
- During an operation, activating the $\overline{\text{FT}}$ pin is not allowed.

6.3.4 Power-On Playback Operation

- If $\overline{\text{PlayE}}$ is kept at Low during power turns on, the device plays message once, then powers down.
- If $\overline{\text{PlayL}}$ is held at Low during power turns on and constantly maintained at Low, the device will play the message repeatedly, with insignificant dead time between messages regardless of sampling frequencies. This status will sustain unless power is turned off or $\overline{\text{PlayL}}$ somehow returns to High.

6.3.5 Automatic Single Message Playback

- If $\overline{\text{LED}}$ is connected to $\overline{\text{PlayE}}$, once $\overline{\text{PlayE}}$ is triggered, the device plays message repeatedly without power down between the looping playback. However, if $\overline{\text{PlayE}}$ is triggered again during playback, then playback will stop.

6.3.6 Power is interrupted Abruptly

- During the device is in operation, it is strongly recommended that the supply power cannot be interrupted. Otherwise, it may cause the device to become malfunctioning.

7. ABSOLUTE MAXIMUM RATINGS [1]

ABSOLUTE MAXIMUM RATINGS

CONDITION	VALUE
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pins	(V_{SS} – 0.3V) to (V_{CC} + 0.3V)
Voltage applied to Input pins (current limited to +/-20 mA)	(V_{SS} – 1.0V) to (V_{CC} + 1.0V)
Voltage applied to output pins (current limited to +/-20 mA)	(V_{SS} – 1.0V) to (V_{CC} + 1.0V)
V_{CC} – V_{SS}	-0.3V to +7.0V

[1] Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability and performance. Functional operation is not implied at these conditions.

7.1. OPERATING CONDITIONS

OPERATING CONDITIONS

CONDITION	VALUE
Operating temperature range	0°C to +50°C
Operating voltage (V_{CC}) [1]	+2.4V to +5.5V
Ground voltage (V_{SS}) [2]	0V

[1] $V_{CC} = V_{CCA} = V_{CCD}$

[2] $V_{SS} = V_{SSA} = V_{SSD}$

8. ELECTRICAL CHARACTERISTICS

8.1. DC PARAMETERS

PARAMETER	SYMBOL	MIN[2]	TYP[1]	MAX[2]	UNITS	CONDITIONS
Input Low Voltage	V_{IL}			0.3xVcc	V	
Input High Voltage	V_{IH}	0.7xVcc			V	
Output Low Voltage	V_{OL}			0.3xVcc	V	I_{OL} = 4.0 mA[3]
Output High Voltage	V_{OH}	0.7xVcc			V	I_{OH} = -1.6 mA[3]
Standby Current	I_{STBY}		1	10	µA	[4] [5]
Record Current	I_{REC}		20	30	mA	V_{CC} = 5.5V [4] [5]
Playback Current	I_{PLAY}		20	30	mA	V_{CC} = 5.5V, no load [4] [5]
Pull-up device for $\overline{REC}$, $\overline{PlayE}$, $\overline{PlayL}$, $\overline{FT}$ & $\overline{M1}$ ~ $\overline{M8}$ pins	R_{PU1}		600		kΩ	
MIC+ Input Resistance	R_{MICP}		18		KΩ	
MIC- Input Resistance	R_{MICN}		18		KΩ	
AnaIn Input Resistance	R_{ANAIN}		42		KΩ	
MIC Differential Input	V_{IN1}	15		300	mV	Peak-to-peak
AnaIn Input	V_{IN2}			1	V	Peak-to-peak
Gain from MIC to SP+/-	A_{MSP}	6		40	dB	V_{IN} = 15~300 mVp-p, AGC = 4.7 µF, V_{CC} = 2.4V~5.5V
Gain from AnaIn to SP+/-	A_{ASP}		0		dB	V_{CC} = 2.4V~5.5V
Output Load Impedance	R_{SPK}	8			Ω	Speaker load
Speaker Output Power	Pout		670		mW	V_{DD} = 5.5 V; 1Vp-p, 1 kHz sine wave at AnaIn. R_{SPK} = 8 Ω
			313		mW	V_{DD} = 4.4 V
			117		mW	V_{DD}= 3 V
			49		mW	V_{DD}= 2.4 V
Speaker Output Voltage	V_{OUT1}		V_{DD}		V	R_{SPK} = 8Ω Speaker, Typical buzzer
Total Harmonic Distortion	THD		1		%	15 mV p-p 1 kHz sine wave, Cmessage weighted

Notes: [1] Typical values @ V_{CC} = 5.5V, T_A = 25° and sampling frequency (Fs) at 8 kHz, unless stated.

[2] Not all specifications are 100 percent tested. All Min/Max limits are guaranteed by Nuvoton via design, electrical testing and/or characterization.

[3] LED output during recording.

[4] V_{CCA}, V_{CCD} and V_{CCP} are connected together. Also, V_{SSA}, V_{SSD}, V_{SSP1} and V_{SSP2} are linked together.

[5] All required control pins must be at appropriate status. External components are biased under a separated power supply.

8.2. AC PARAMETERS

CHARACTERISTIC [1]	SYMBOL	MIN[2]	TYP	MAX[2]	UNITS	CONDITIONS
Sampling Frequency	Fs	4		12	kHz	[3]
Record / Playback Duration (ISD1916)	T_{REC} / T_{PLAY}	10.6		32	sec	[3]
Record / Playback Duration (ISD1932)	T_{REC} / T_{PLAY}	21.3		64	sec	[3]
Record / Playback Duration (ISD1964)	T_{REC} / T_{PLAY}	42.6		128	sec	[3]
Debounce Time	T_{Deb}	225k/Fs			msec	[3] [4]
Address Setup Time	T_{ASet}	30			nsec	
Address Hold Time	T_{Ahold}	225k/Fs			msec	[3] [4]
Erase Time	T_{Ers}	1.25MRN			msec	MRN = message row #
FMC Setup Time	T_{Fset}	30			nsec	
Record Settle Time	$T_{Settle1}$		32k/Fs		msec	[3] [4]
Play Settle Time	$T_{Settle2}$		256k/Fs		msec	[3] [4]
Delay from Record to Play	$T_{Settle3}$		128k/Fs		msec	[3] [4]
Record Stop Time	T_{Stop1}	30			nsec	
LED Pulse Low Time	T_{EOM}		256k/Fs		msec	[3] [4]

Notes:

[1] Conditions are V_{CC} = 5.5V, T_A = 25°C and sampling frequency (F_S) at 8kHz, unless specified.

[2] Not all specifications are 100 percent tested. All Min/Max limits are guaranteed by Nuvoton via design, electrical testing and/or characterization.

[3] When different F_S is applied, the value will change accordingly. Also, stability of internal oscillator may vary as much as ±10% over the operating temperature and voltage ranges.

[4] k = 1000.

9. TYPICAL APPLICATION CIRCUIT

The following typical application examples on ISD1900 series are for references only. They make no representation or warranty that such applications shall be suitable for the use specified. It's customer's obligation to verify the design in its own system for the functionalities, voice quality, current consumption, and etc.

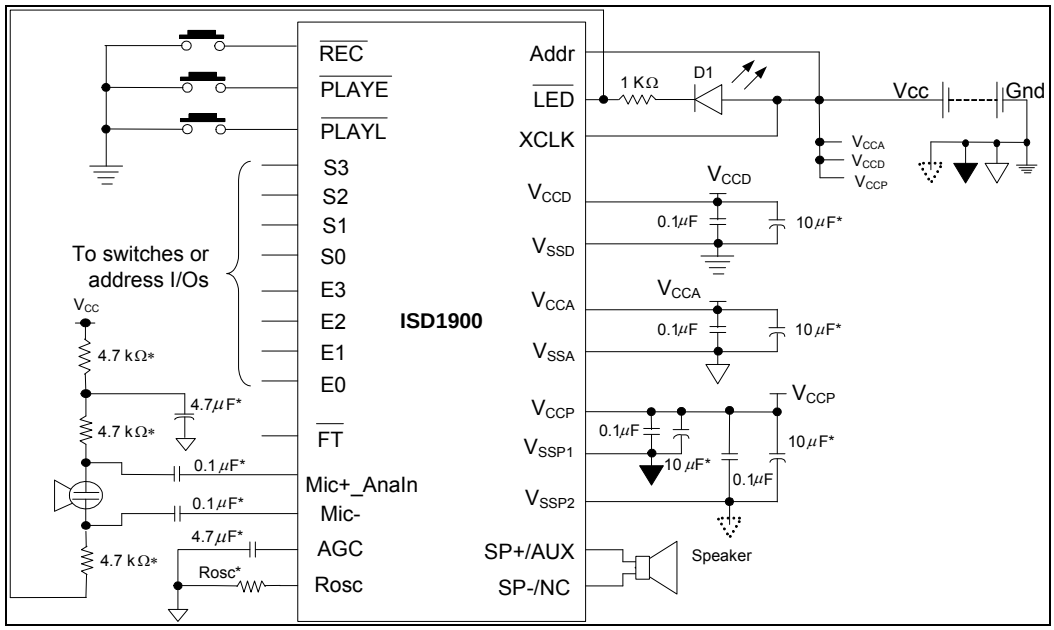
In addition, the below notes apply to the following application examples:

- The suggested values are for references only. Depending on system requirements, they can be adjusted for functionalities, voice quality and degree of performance.

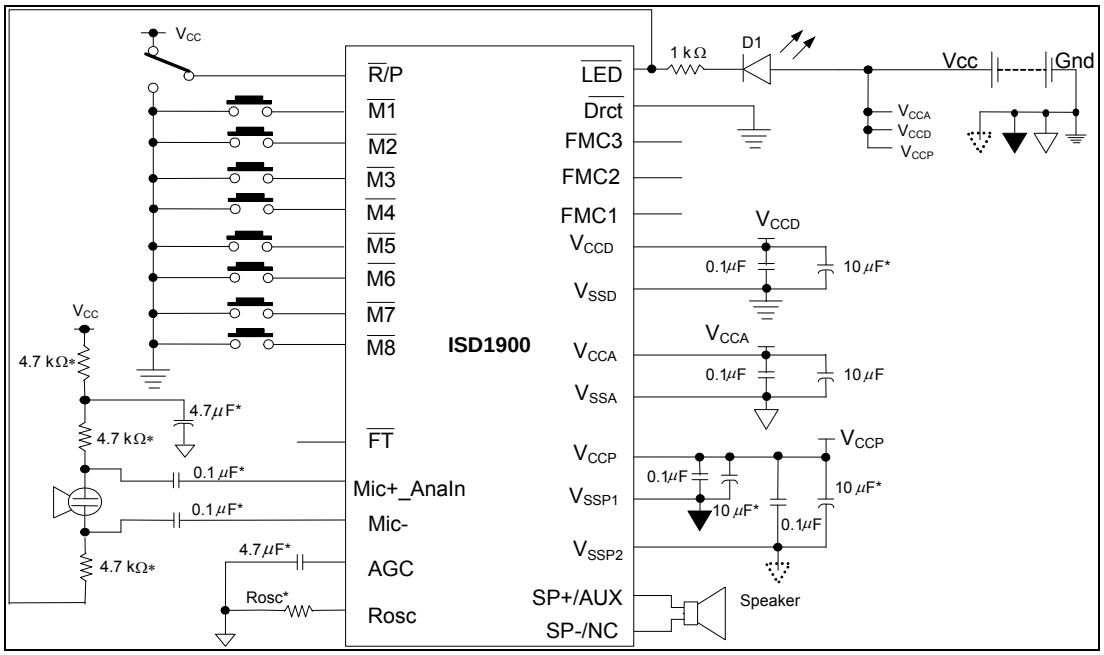
It is important to have a separate path for each ground and power back to the related terminals to minimize the noise. Besides, the power supplies should be decoupled as close to the device as possible.

Also, it is crucial to follow good audio design practices in layout and power supply decoupling. See recommendations in Application Notes from our websites.

Example #1: Operations via start and end address under Address Mode.



Example #2: Fixed Message Configuration Operations under Direct Mode.



Good Audio Design Practices

Nuvoton's ChipCorder are very high-quality single-chip voice recording and playback devices. To ensure the highest quality voice reproduction, it is important that good audio design practices on layout and power supply decoupling are followed. See Application Information links below for details.

Good Audio Design Practices

http://www.Nuvoton-usa.com/products/isd_products/chipcorder/applicationinfo/apin11.pdf

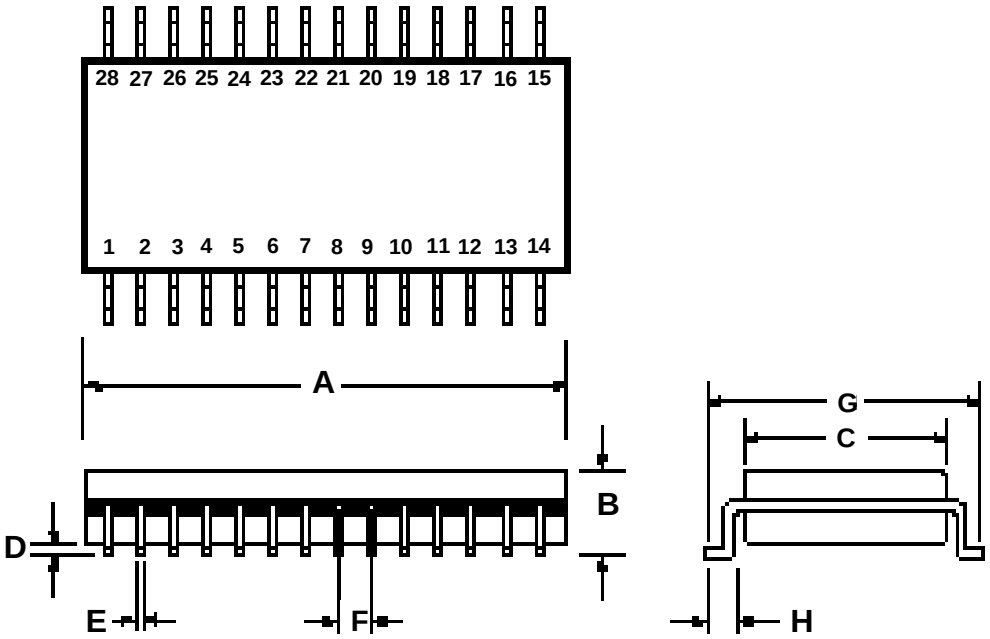
Single-Chip Board Layout Diagrams

http://www.Nuvoton-usa.com/products/isd_products/chipcorder/applicationinfo/apin12.pdf

It is strongly recommended that before any design or layout project starts, the designer should contact Nuvoton Sales Rep for the most update technical information and layout advice.

10. PACKAGING

10.1. 28-LEAD 300-MIL PLASTIC SMALL OUTLINE INTEGRATED CIRCUIT (SOIC)



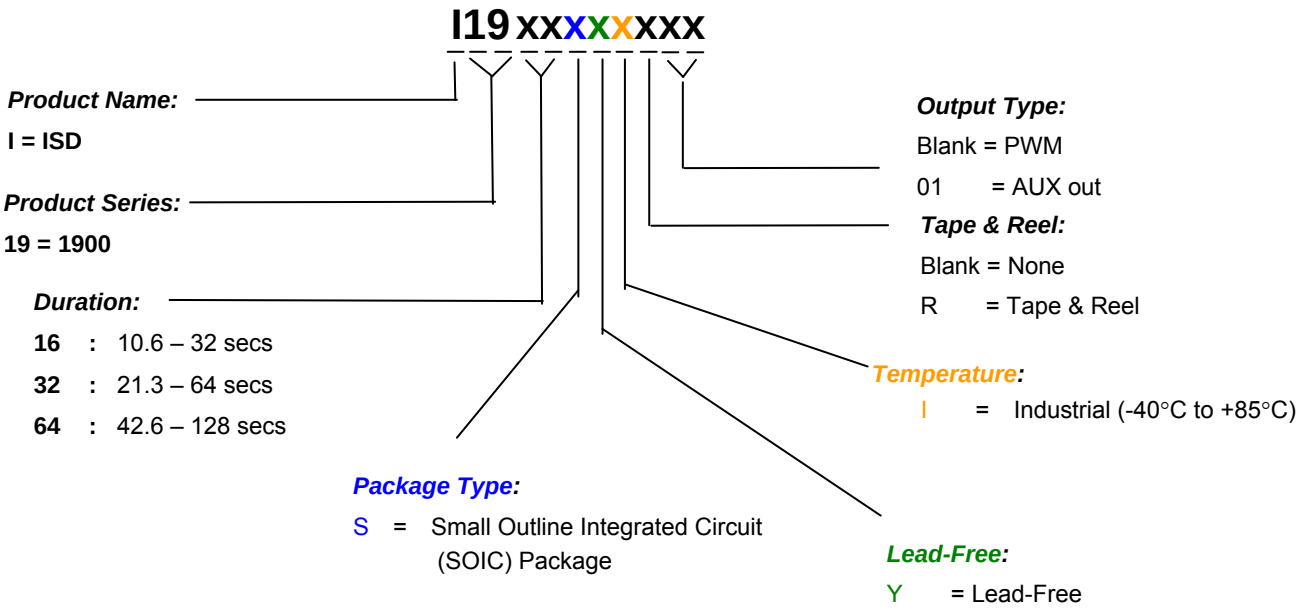
Plastic Small Outline Integrated Circuit (SOIC) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.701	0.706	0.711	17.81	17.93	18.06
B	0.097	0.101	0.104	2.46	2.56	2.64
C	0.292	0.296	0.299	7.42	7.52	7.59
D	0.005	0.009	0.0115	0.127	0.22	0.29
E	0.014	0.016	0.019	0.35	0.41	0.48
F		0.050			1.27	
G	0.400	0.406	0.410	10.16	10.31	10.41
H	0.024	0.032	0.040	0.61	0.81	1.02

Note: *Lead coplanarity to be within 0.004 inches.*

11. ORDERING INFORMATION

Product Number Descriptor Key



When ordering ISD1900 devices, please refer to the above ordering scheme. Contact the local Nuvoton Sales Representatives for any questions and the availability.

For the latest product information, please contact the Nuvoton Sales/Rep or access Nuvoton's worldwide web site at http://www.Nuvoton-usa.com

12. VERSION HISTORY

VERSION	DATE	DESCRIPTION
0	Aug 11, 2007	Initial revision
0.1	Oct 10, 2007	Update block diagram
0.2	Oct 16, 2007	Update description
0.3	July 23, 2008	Generalize for different derivatives.
0.4	Aug 15, 2008	Update timing and application diagrams.
0.41	Aug 21, 2008	Add description of AGC.
0.51	Jan 5, 2009	Rename Norm/$\overline{\text{Mode}}$ to Addr/$\overline{\text{Drct}}$.

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