AM Receiver IC

Data Sheet

Preliminary

General Description

The SDL8086is an AM receiver with built-in very high sensitivity for the time signal transmitted from WWVB, DCF77, JJY, MSF and HBG. The receiver is provided for single-and dual band by using additional capacitor matching pin) reception.

Features

- Low power consumption (<90μA)
- Very high sensitivity (0.4μV)
- Dedicated input for external crystal shunt capacitance matching for dual band application
- High selectivity by using crystal filter
- Power down mode
- Only a few external components necessary
- AGC hold mode
- Wide frequency range (40 ~80 kHz)
- Low power applications (1.8 ~ 3.6 V)
- Integrated AGC adaptation
- Complementary output stage

Application

Time signal receiver WWVB (USA), DCF77(Germany), JJY (Japan), MSF (UK), and HBG (Switzerland).

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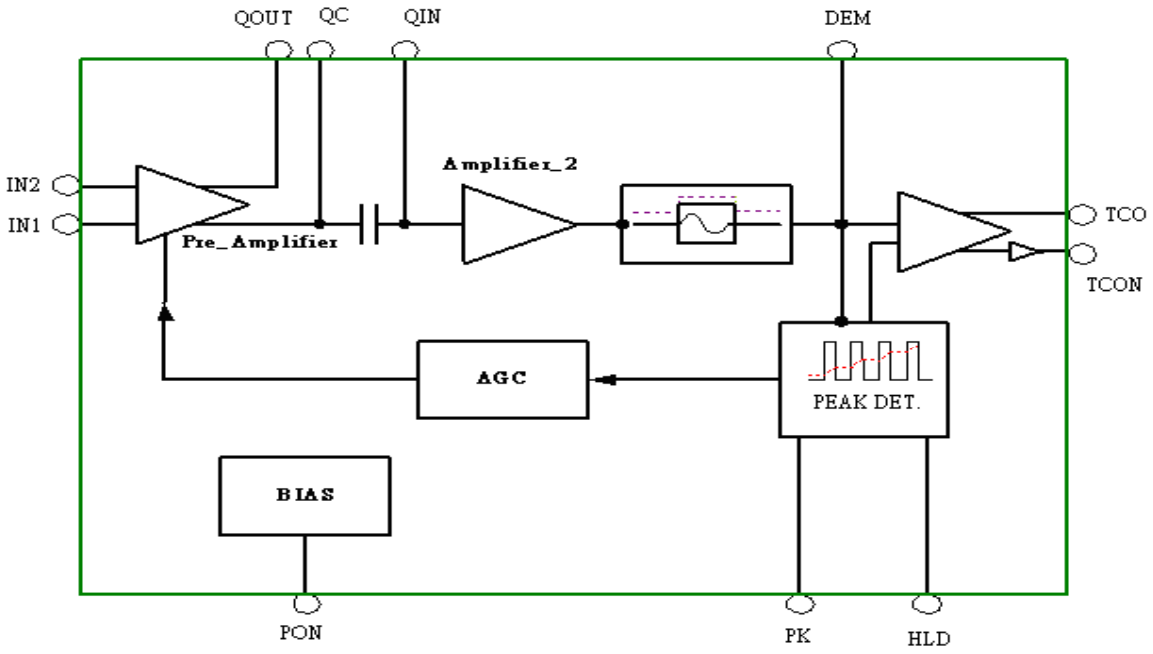
Block Diagram



Pad Coordinates

Pad No.	Pad name	Function	x-axis(μm)	y-axis(μm)
1	QIN	Crystal Input	**155.40**	**725.00**
2	GND	Ground	**155.40**	**610.00**
3	QOUT	Crystal Output	**155.40**	**495.00**
4	VCC	Supply Voltage	**153.40**	**380.00**
5	IN2	Antenna Input2	**155.40**	**265.00**
6	IN1	Antenna Input1	**155.40**	**150.00**
7	TCON	Negative Signal Output	**944.60**	**152.70**
8	TCO	Positive Signal Output	**944.60**	**283.70**
9	PON	Power ON Input	**944.60**	**492.30**
10	PK	Capacity for AGC	**944.60**	**607.30**
11	HLD	AGC Hold	**944.60**	**722.30**
12	DEM	Demodulator Output	**944.60**	**837.30**
13	QC	Crystal matching Cap	**155.40**	**840.00**

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IN1, IN2

A ferrite antenna is connected between IN 1 and IN 2. For high sensitivity, the Q factor of the antenna circuit should be as high as possible.
Please note that a high Q factor requires temperature compensation of the resonant frequency in most cases. We recommend a Q factor between 40 and 150, depending on the application.
An optimal signal-to-noise ratio will be achieved by a resonator resistance from 40 kΩ to 100 kΩ.

QOUT, QIN, QC

In order to achieve a high selectivity, a Crystal is connected between pins QOUT and QIN. It is used with serial resonant frequency according to the time-code transmitter and acts as a serial resonator.
Up to 2 Crystal options can be connected in parallel between QOUT and QIN.

For one Crystal, the parallel capacitor given by the filter crystal (about 1.4 pF) is internally compensated, and the bandwidth of the filter is about 10 Hz.

For two crystals, an additional external capacitor with the value of about 1.4 pF must be connected in parallel between QC and QIN, which means the Parasitic loads should be avoided due to the high impedance of QIN.

DEM

Demodulator output. To assure the function works well, an external capacitor has to be connected to this output.

Note : The value 22nF of capacitor C_{DEM} shown on test circuit represents the minimum value at frequency of 77.5 kHz. For lower frequencies (40kHz, 60kHz) a minimum value of C_{DEM}=47nF should be used.
For a better damping of noise and other interference, it is recommended to double the values of C_{DEM}, which means C_{DEM} = 47nF with 77.5kHz and C_{DEM} = 100nF with 40kHz and 60kHz. This optimization is done according to each application.

HLD

AGC Hold Mode: HLD high (VHLD = VCC) sets normal function, HLD low (VHLD = 0) holds the AGC voltage for a short time. This can be used to prevent the AGC from peak voltages, which created by e.g. a stepper motor

PK

Peak Detector Output. The external capacitor must be connected to assure the function of the AGC regulation works well. The value of the capacitance will influence the AGC regulation time.

Note **:** To realize a good regulation timing of the demodulator with the peak detector, the value of the capacitors at DEM and PK has to be changed according to the different protocols.

VCC, GND

VCC and GND are the supply voltage input. The positive power supplies have to be connected externally, and also the ground pins.
To power down the circuitry, it is recommended to use the PON input and do not switch the power supply.
Switching the power supply will result in a long power-up waiting time.

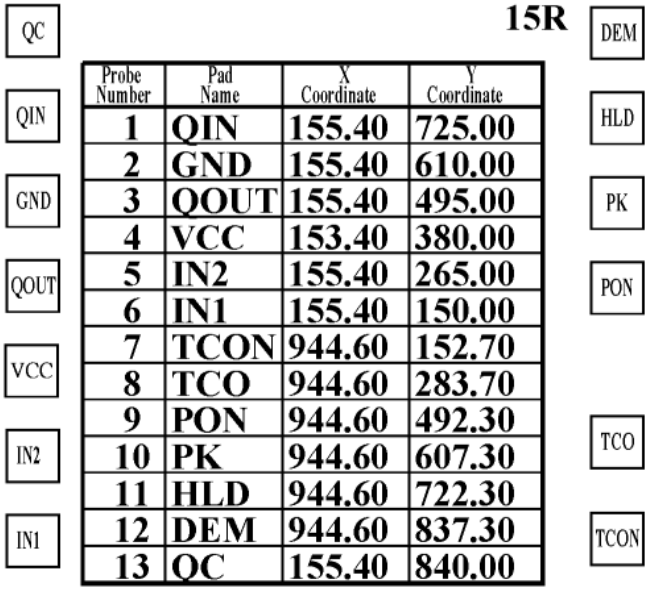
PON

If PON is connected to GND, the receiver will be enabled. The setup time is typically 0.5 sec after applying GND to this pin. If PON is connected to VCC, the receiver will switch to Power Down mode.

TCO, TCON

The serial signal of the time-code transmitter can be directly decoded by a micro controller. The time-code format of several transmitters in detail are described respectively. If TCO is connected, then TCON must be open or counter-wise.

Pad Diagram



Probe Number	Pad Name	X Coordinate	Y Coordinate
1	QIN	155.40	725.00
2	GND	155.40	610.00
3	QOUT	155.40	495.00
4	VCC	153.40	380.00
5	IN2	155.40	265.00
6	IN1	155.40	150.00
7	TCON	944.60	152.70
8	TCO	944.60	283.70
9	PON	944.60	492.30
10	PK	944.60	607.30
11	HLD	944.60	722.30
12	DEM	944.60	837.30
13	QC	155.40	840.00

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply Voltage	V_{CC}	5	V
Ambient Temperature Range	T_{amb}	-20 to +70	°C
Storage Temperature Range	R_{stg}	-55 to +150	°C
Junction Temperature	T_j	125	°C
Electrostatic Handling (HBM)	V_{ESD}	±8000	V
Electrostatic Handling(MM)	V_{ESD}	±650	V

Electrical Characteristics

V_{CC} = 3V, input signal frequency of 60 kHz ±5Hz; Carrier voltage 100% reduction to 30% ;
T_{amb} = 25℃, max./min. limits are at +25℃ ambient temperature, unless otherwise specified.

Parameter	Test condition	Symbol	Min.	Typ.	Max.	Unit
Supply voltage Range	Pad VCC	V_{CC}	1.8		3.6	V
Supply Current	Pad VCC	I_{CC}		< 90	95	μA
Set-up time after VCC ON	V_{CC}=3V	t		1.5		s
Reception Frequency range		F_{in}	40		80	kHz
Minimum Input Voltage	Pad IN1,IN2	V_{in}		0.4	0.6	μV
Maximum Input Voltage	Pad IN1,IN2	V_{in}		30		mV
Input Amplifier max. gain	V_{PK}=0.2V	V_{U1}		47		dB
Input Amplifier min. gain	V_{PK}=0.8V	V_{U2}		-40		dB
Pins TCO,TCON Output low Output high	 I_{OL} =10 μA I_{OH} =-10 μA		 0.9 x V_{CC}		 0.1 x V_{CC}	 V V

Power-ON control (PON pad)

Parameter	Test condition	Symbol	Min.	Typ.	Max.	Unit
Input level Input leakage current	Low level High level 0<V_i< Vcc		 0.85V_{CC} -0.1		0.15V_{CC} 0.1	V V μA
Quiescent current receiver OFF	V_{PON}=V_{CC}, Pad VCC	Icc0		0.03		μA
Set-up time after PON		t		0.5	2	s

AGC hold mode (HLD pad)

Parameter	Test condition	Symbol	Min.	Typ.	Max.	Unit
Input level	Low level High level		 0.85V_{CC}		0.15V_{CC}	V V

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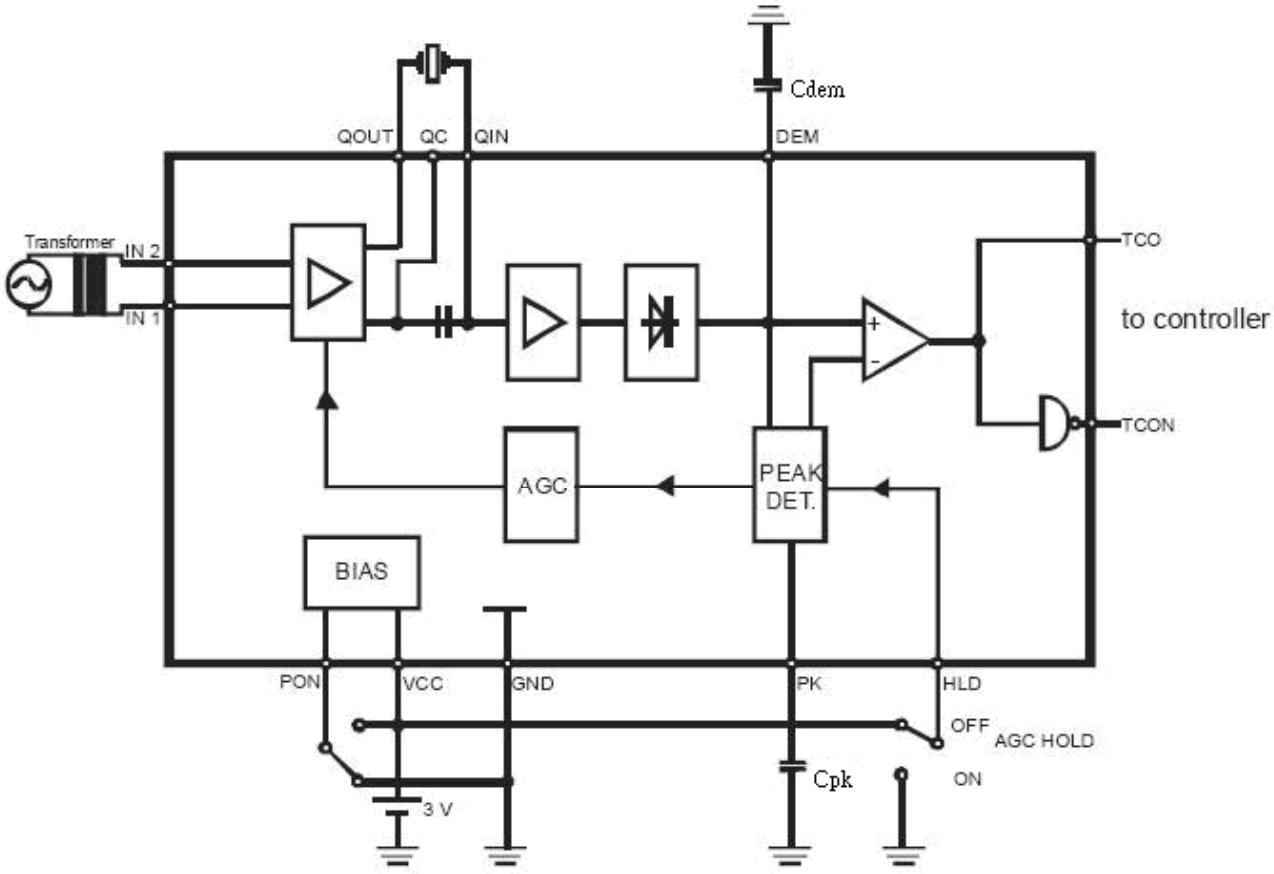
Input leakage current	$0<V_i < V_{CC}$		-0.1		0.1	μA

AC characteristics

Parameter	Test condition	Symbol	Min.	Typ.	Max.	Unit
Output pulse width for TCO and TCON	Modulation according DCF, 200 ms pulse	t_{WO200}	170	195	230	ms
Output pulse width for TCO and TCON	Modulation according DCF, 100 ms pulse	t_{WO100}	70	95	130	ms

Test Circuitry for single frequency reception



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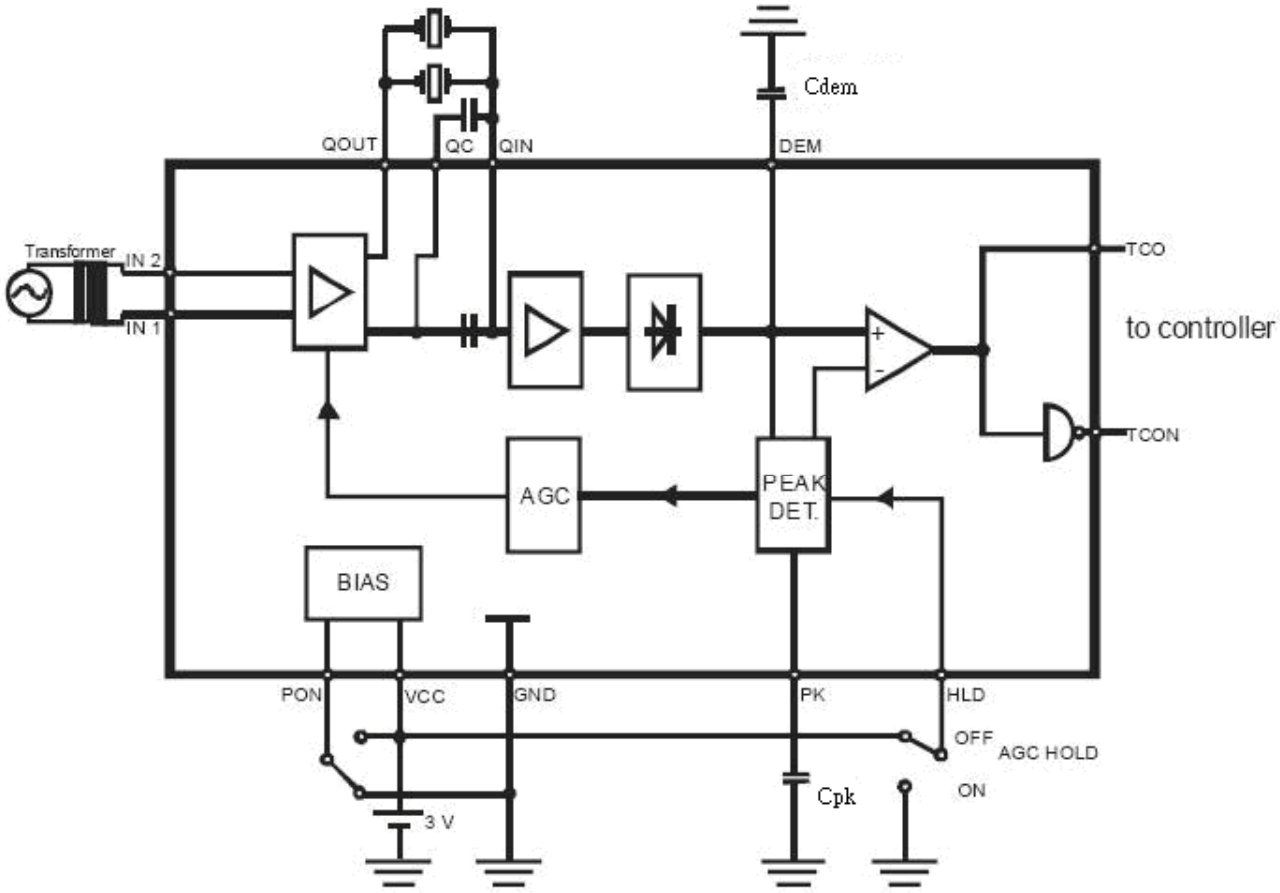
Test Circuitry for dual frequency reception



DEM and PK capacitors

The DEM capacitor influences the stability of the demodulator output. The PK capacitor value influences the AGC regulation time. Note that the suggested values may be different for different PCB layouts and some fine tuning of the DEM capacitor may be necessary to achieve the optimum sensitivity. However, it is not recommended to change the PK value.

	Cdem	Cpk
DCF	47nF	4.7μF
WWVB	100nF	4.7μF
JJY60	100nF	4.7μF
MSF	100nF	4.7μF
JJY40	100nF	4.7μF