OKI

MSM64P164

User's Manual

CMOS 4-bit microcontroller

FIRST EDITION

ISSUE DATE: Oct. 1993

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

5. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.

6. The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans. Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.

7. Certain products in this document may need government approval before they can be exported to particular countries. The purchaser assumes the responsibility of determining the legality of export of these products and will take appropriate and necessary steps at their own expense for these.

8. No part of the contents contained herein may be reprinted or reproduced without our prior permission.

Printed in Japan

Preface

The MSM64P164 is a 4-bit single chip microcontroller, which uses a built-in one time PROM (OTP) in place of built-in mask ROM in the MSM64164.

The MSM64P164 is manufactured with the N-well EPROM process instead of the P-well CMOS process. That is why the porality of the MSM64P164's power supply is defferent than the porality of the chip with the P-well CMOS structure.

The OTP chip alone has no supply.

This manual explains the specific hardware of the MSM64P164 and the differences from the mask ROM version of the MSM64164.

See "MSM64164 User's Manual" for further reference relating to other hardware and instruction sets.

TABLE OF CONTENTS

Chapter 1 Summary

1.1 Summary 1-1
1.2 Features 1-1
1.3 Block Diagram 1-3
1.4 Pin Configuration 1-4
1.5 Explanation of Pins 1-5
1.5.1 Explanation of Each Pin 1-5
1.5.2 PROM Related Pins 1-9
1.5.3 Processing of Unused Pins 1-10

Chapter 2 Power Supply System

2.1 Summary 2-1
2.2 Circuit Configuration of the Power Supply System 2-2
2.2.1 Power Supply Circuit Configuration for IC 2-2
2.2.2 Circuit Configuration for 5V Interface 2-3
2.3 Logic Power Supply 2-4
2.3.1 Configuration of the Logic Power Supply Driving Circuits 2-4
2.3.2 Operations of Optional 1.5V Logic Power Supply Circuits 2-5
2.3.3 Operations of Optional 3.0V Logic Power Supply Circuits 2-5
2.4 LCD Bias Level 2-6

Chapter 3 X'tal Oscillation Circuits

3.1 Summary 3-1
3.2 Configuration of X'tal Oscillation Circuits 3-1

Chapter 4 PROM

4.1 Summary 4-1
4.2 Explanation of Pins 4-1
4.3 PROM Mode 4-3
4.3.1 Setting the PROM Mode 4-3
4.3.2 PROM Mode Functions 4-3
4.3.3 Connection to the EPROM Writer 4-4

Appendixes

Appendix A Diagram of Package Measurements A-1

Appendix B Input and Output Circuit Configurations B-1

Appendix C Examples of Application Circuits C-1

Appendix D Mask Options D-1

Appendix E Electrical Characteristics E-1

Chapter 1

SUMMARY

1. Summary

1.1 Summary

The MSM64P164 is a program memory (ROM) chip built into the MSM64164(mask ROM chip) which is converted to a one time PROM (OTP) chip.

Since the MSM64P164 has a different configuration of the mask ROM chip with P-well CMOS configuration of the chip, the N-well is manufactured with the EPROM process. That is why the polarity of the power source used for LCD bias generation, 5V interface, etc. is reversed, and the arrangement of external circuits is different from the arrangement of the mask ROM chip.

In addition, this chip that differs from the mask ROM chip has no supply.

For these reasons, this OTP version of the MSM64P164 should be used mainly for verification of application program functions.

The MSM64P164 has two operating modes of a microcontroller operating mode and PROM mode. The microcontroller operating mode is a mode to make the same operation as a mask ROM chip and the PROM mode is a mode to write/read PROM.

The descriptions on the microcontroller operating mode are omitted in this manual. Therefore, see "MSM64164 User's Manual". This manual explains different specifications from the mask ROM chip in Chapters 2 and 3 and Chapter 4 explains the PROM mode.

1.2 Features

1) A Rich Set of Instructions Including Byte Calculating Instructions
   - 148 types of instructions
   - Byte addition and subtraction, byte transmission, byte comparing instructions
   - Bit operation instructions
   - Data exchange instructions

2) Rich Addressing Mode
   - Two types of indirect addressing modes for HL registers and XY registers
   - Bit operations for all data memory areas
   - Byte calculation for all data memory areas

3) Operating Frequency: Low-speed clock 32.768 kHz X'tal oscillation (minimum instruction execution time: 91μs)
   High-speed clock 400 kHz CR oscillation

4) Built-In Program Memory: 4064 bytes (PROM)

5) Built-In Data Memory: 256 nibbles

6) I/O Ports: a total of 20 ports
   - 4-bit input-output ports (selectable NMOS open drain output/CMOS output, selectable pull-down and pull-up resistance input/high impedance input) $\times$ 3
   - 4-bit input port (selectable pull-down and pull-up resistance input/high impedance input) $\times$ 1
   - 4-bit output port (selectable NMOS open drain output/CMOS output) $\times$ 1

7) Buzzer Output: 1 output
   - 4-output modes selectable

8) Serial Port: 1 port
   - Synchronous system 8-bit transmission
   - External clock/internal clock selectable
   - MSB first/LSB first selectable

9) LCD Driver: 34 drivers
   - 1/4 duty, during 1/3 bias: 120 segments (30 $\times$ 4)
   - 1/3 duty, during 1/3 bias: 93 segments (31 $\times$ 3)
   - 1/2 duty, during 1/2 bias: 64 segments (32 $\times$ 2)
   - Output ports selectable by mask options on 8 drivers
   - Preparation for several kinds of standard mask option products

10) CR Oscillation System A/D Converter: 2 channels
   - 2-channel system by time division
   - A Counter: 1/ ($10^4 \times 8$) $\times$ 1
   - B Counter: $1/2^{14} \times 1$

11) Capture Circuit: 2 channels
   - 256Hz, 128Hz, 64Hz, 32Hz

12) Watchdog Timer

13) Interrupt Factors: 10 factors
   - Two external factors, five timer base factors, one serial port factor, one A/D converter factor, one watchdog timer factor

14) Power Supply Voltage
   1.5V/3V mask option selectable
   Low current consumption

15) External Appearance
   - Flat package with 80 pins (QFP)

1.3 Block Diagram

Figure 1-1 shows the block diagram of the MSM64P164.

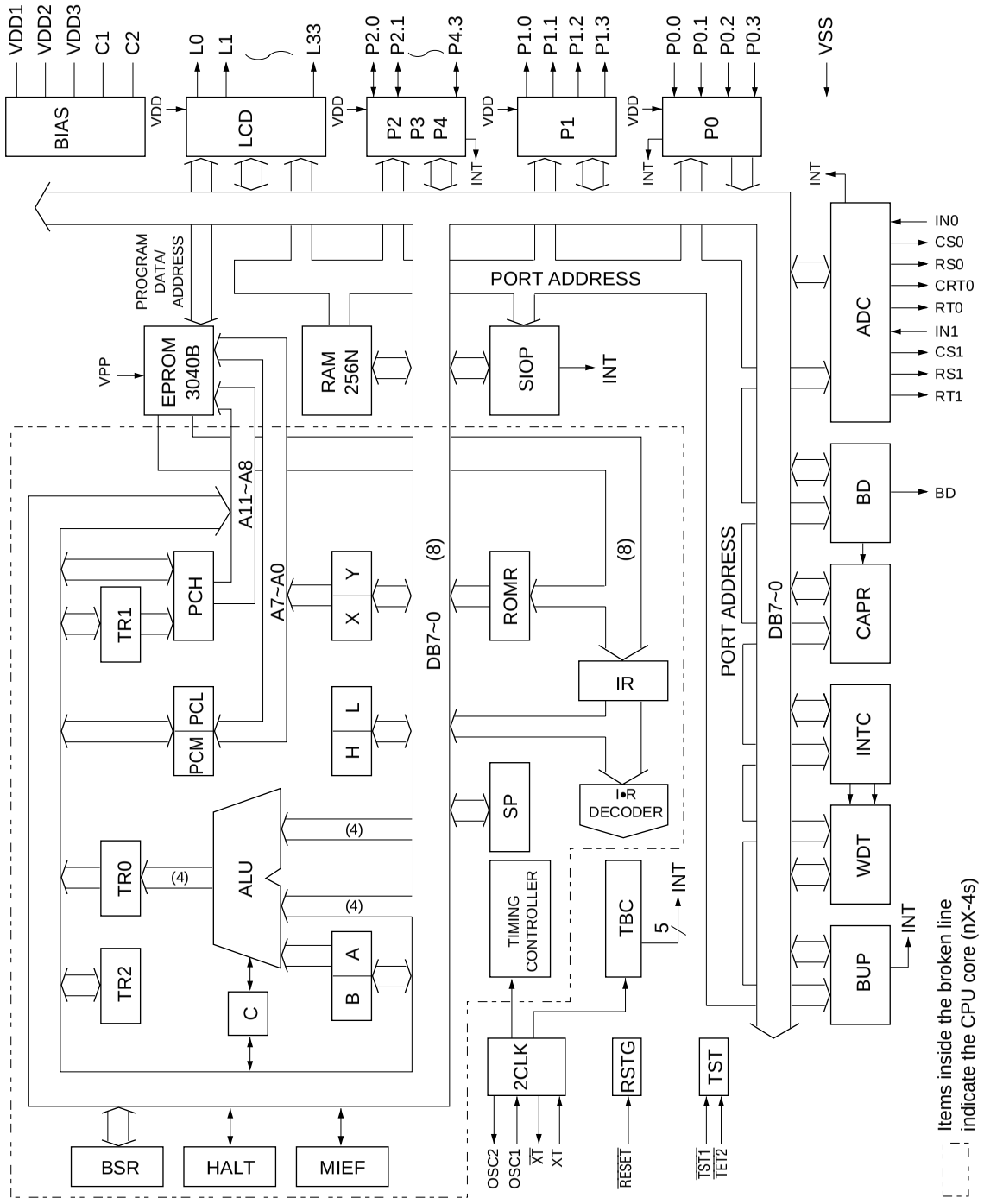
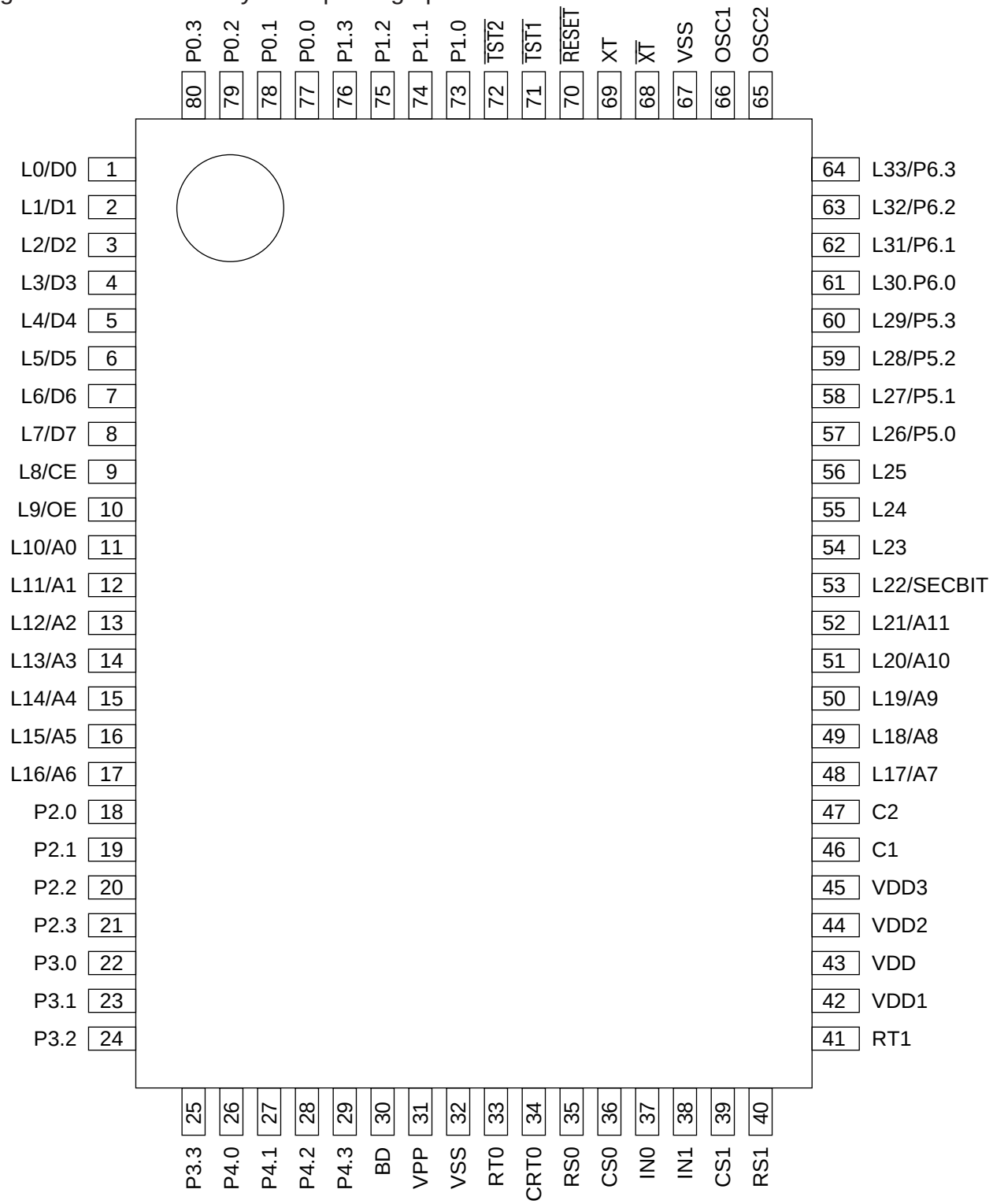


Figure 1-1 Block Diagram of the MSM64P164

1.4 Pin Configuration

Figure 1-2 shows the layout of package pins of the MSM64P164.



Note: The 32 and 67 pins are shortcircuited inside the IC. Therefore, the VSS may be supplied to either pins.

Figure 1-2 Pin Configuration Diagram of the MSM64P164 (QFP)

1.5 Explanation of Pins

1.5.1 Explanation of Each Pin

Table 1-1 shows basic functions of each of the MSM64P164 pins, Table 1-2 shows secondary functions of the same.

Table 1-1 (a) Explanation of Pins (Basic Functions)

Type	Pin Name	Pin No.	Input/ Output	Function
Power Supply	VSS	32,67	—	Digital 0V power supply
	VDD1	42	—	Digital plus side power supply (for 1.5V specs) LCD drive bias output (for 3.0V specs)
	VDD2	44	—	Digital plus side power supply (for 3.0V specs) LCD drive bias output (for 1.5V specs)
	VDD3	45	—	LCD drive bias output (+4.5V)
	VDD	43	—	Input and output port interface plus side power supply
	C1	46	—	LCD drive bias generating capacitor connection pin
	C2	47	—	
	VPP	31	—	Plus side power supply for PROM writing (+12.5V)
Oscillation	XT	69	Input	Low-speed side clock oscillation input pin: Connect to crystal oscillator (32.768 kHz)
	$\overline{XT}$	68	Output	
	OSC1	66	Input	High-speed side clock oscillation output pin: Connect to oscillation external resistor (ROS)
	OSC2	65	Output	
Test	$\overline{TST1}$	71	Input	Input pin for tests These are pulled up to V_{DD} internally.
	$\overline{TST2}$	72	Input	
RESET	$\overline{RESET}$	70	Input	System reset input: When this pin reaches the level "L" ⇒ "H", internal status is initialized and instructions are executed from address 000H. This is pulled up to V_{DD} internally.

Table 1-1 (b) Explanation of Pins (Basic Functions)

Type	Pin Name	Pin No.	Input/ Output	Function
Port	P0.0	77	Input	4-bit input port (P0): These are 4-bit input ports permitting selection of the pull-up resistance input/pull-down resistance input/high impedance input through the control register of port 01 (P01CON). As the secondary functions, an external interrupt function is allocated to P0.0 to P0.3 and a capture trigger function is assigned to P0.0 and P0.1.
	P0.1	78		
	P0.2	79		
	P0.3	80		
	P1.0	73	Output	4-bit output port (P1): These are 4-bit output ports permitting selection of the NMOS open drain output/CMOS output through the control register of port 01 (P01CON). P1.0 is a large electric current driving output port.
	P1.1	74		
	P1.2	75		
	P1.3	76		
	P2.0	18	Input/ Output	4-bit input/output port (P2): These are 4-bit input/output ports permitting selection of input/output per bit through the control registers 0 to 3 of port 2 (P20CON to P23CON), selection of the pull-up and pull-down rsistance input/high impedance input, and selection of the NMOS open drain output/CMOS output. As the secondary functions, an external interrupt function is allocated.
	P2.1	19		
	P2.2	20		
	P2.3	21		
	P3.0	22	Input/ Output	4-bit input/output port (P3): These are 4-bit input/output ports permitting selection of the input/output per bit through the control registers 0 to 3 of port 3 (P30CON to P33CON), selection of the pull-up and pull-down resistance input/high impedance input, and selection of the NMOS open drain output/CMOS output. As the secondary functions, an external interrupt funciton is allocated to P3.0 to P3.3 and a serial port function is asigned to P3.3.
	P3.1	23		
	P3.2	24		
	P3.3	25		
	P4.0	26	Input/ Output	4-bit input/output port (P4): These are 4-bit input/output ports permitting selection of the input/output per bit through the control registers 0 to 3 of port 4 (P40CON to P43CON), selection of the pull-up and pull-down resistance input/high impedance input, and selection of the NMOS open drain output/CMOS output. As the secondary functions, P4.0 to P4.3 have an external interrupt function, P4.0 to P4.2 have a serial port function, and P4.3 has a monitor function of a CR oscillation clock for AD conversion.
	P4.1	27		
	P4.2	28		
	P4.3	29		
Buzzer	BD	30	Output	This is the output pin of buzzer dirver.
A/D Converter	RT0	33	Output	This is the connecting pin for a measuring resistance sensor of a channel 0.
	CRT0	34	Output	This is the connecting pin for a measuring resistance/ capacitance sensor of a channel 0.
	RS0	35	Output	This is the standard resistance connecting pin of a channel 0.
	CS0	36	Output	This is the standard capacitance connecting pin of a channel 0.
	IN0	37	Input	This is the oscillation input pin of a channel 0.
	RT1	41	Output	This is the measuring resistance sensor connecting pin of a channel 1.
	RS1	40	Output	This is the standard resistance connecting pin of a channel 1.
	CS1	39	Output	This is the standard capacitance connecting pin of a channel 1.
	IN1	38	Input	This is the oscillation input pin of a channel 1.

Table 1-1 (c) Explanation of Pins (Basic Functions)

Type	Pin Name	Pin No.	Input/ Output	Function
LCD Driver	L0	1	Output	LCD segment common signal output pins
	L1	2	Output	
	L2	3	Output	
	L3	4	Output	
	L4	5	Output	
	L5	6	Output	
	L6	7	Output	
	L7	8	Output	
	L8	9	Output	
	L9	10	Output	
	L10	11	Output	
	L11	12	Output	
	L12	13	Output	
	L13	14	Output	
	L14	15	Output	
	L15	16	Output	
	L16	17	Output	
	L17	48	Output	
	L18	49	Output	
	L19	50	Output	
	L20	51	Output	
	L21	52	Output	
	L22	53	Output	
	L23	54	Output	
	L24	55	Output	
	L25	56	Output	
	L26/P5.0	57	Output	LCD segment common signal output pins or output ports through mask options
	L27/P5.1	58	Output	
	L28/P5.2	59	Output	
	L29/P5.3	60	Output	
	L30/P6.0	61	Output	
	L31/P6.1	62	Output	
	L32/P6.2	63	Output	
	L33/P6.3	64	Output	

Table 1-2 Explanation of Pins (Secondary Functions)

Type	Pin Name	Pin No.	Input/ Output	Function
External Interrupt	P0.0	77	Input	Secondary functions of P0.0 to P0.3: External interrupt input pins. These can receive an interrupt based on a level variation.
	P0.1	78		
	P0.2	79		
	P0.3	80		
	P2.0	18	Input	Secondary functions of P2.0 to P2.3, P3.0 to P3.3, and P4.0 to 4.3: External interrupt input pins . These can receive an interrupt based on a level variation.
	P2.1	19		
	P2.2	20		
	P2.3	21		
	P3.0	22		
	P3.1	23		
	P3.2	24		
	P3.3	25		
	P4.0	26		
	P4.1	27		
	P4.2	28		
	P4.3	29		
Capture Trigger	P0.0	77	Input	Secondary functions of P0.0 and P0.1: Trigger input pins of the capture circuit.
	P0.1	78		
Serial Port	P3.3	25	Input	Secondary function of P3.3: This is allocated to the data input of a serial port (SIN).
	P4.0	26	Output	Secondary function of P4.0: This is allocated to the data output of a serial port (SOUT).
	P4.1	27	Output	Secondary function of P4.1: This is allocated to the data output of a serial port (SPR).
	P4.2	28	Input/ Output	Secondary function of P4.2: This is allocated to the clock input and output of a serial port (SCLK).
CR Oscillation Monitor	P4.3	28	Output	Secondary function of P4.3: This is a monitor output (MON) of a CR oscillaiton clock (OSCCLK) for an A/D converter and a 400 kHz CR oscillation clock for a system clock.

1.5.2 PROM Related Pins

Table 1-3 shows pins used to write program data to the MSM64P164.

Table 1-3 Explanation of Pins (PROM Functions)

Type	Pin Name	Pin No.	Input/ Output	Function
LCD Driver	VSS	32, 67	Output	0V power supply
	VDD1*	42	—	Plus side power supply pin (+5V supplied)
	VDD2*	44	—	Plus side power supply pin (+5V supplied)
	VPP	31	—	PROM write power supply (+12.5V supplied)
	$\overline{\text{RESET}}$	70	Input	PROM write setting pin PROM mode is set by L level input
	$\overline{\text{TST1}}$	71	Input	
	$\overline{\text{TST2}}$	72	Input	
	L0/D0	1	I/O	Pin for writing and reading of program data
	L1/D1	2	I/O	
	L2/D2	3	I/O	
	L3/D3	4	I/O	
	L4/D4	5	I/O	
	L5/D5	6	I/O	
	L6/D6	7	I/O	
	L7/D7	8	I/O	
	L8/CE	9	I/O	PROM chip enable pin
	L9/OE	10	I/O	PROM output enable signal
	L10/A0	11	Input	Program address input pin
	L11/A1	12	Input	
	L12/A2	13	Input	
	L13/A3	14	Input	
	L14/A4	15	Input	
	L15/A5	16	Input	
	L16/A6	17	Input	
	L17/A7	48	Input	
	L18/A8	49	Input	
	L19/A9	50	Input	
	L20/A10	51	Input	
	L21/A11	52	Input	
	L22	53	Input	Input H level

* PROM mode should be supplied with 5V both to VDD1 and VDD2.

1.5.3 Processing of Unused Pins

Table 1-4 shows processing method of unused pins.

Table 1-4 Processing of Unused Pins

Pin	Recommended Pin Connection
OSC1	Open
OSC2	Open
$\overline{TST1}$~$\overline{2}$	Open
P0.0~P0.3	"L" level, "H" level or open (by selection of input mode)
P1.0~P1.1	Open
P2.0~P2.3	For input setting: "L" level, "H" level or open (by selection of input mode) For output setting: Open
P3.0~P3.3	For input setting: "L" level, "H" level or open (by selection of input mode) For output setting: Open
P4.0~P4.3	For input setting: "L" level, "H" level or open (by selection of input mode) For output setting: Open
BD	Open
RT0	Open
CRT0	Open
RS0	Open
CS0	Open
IN0	Open
RT1	Open
RS1	Open
CS1	Open
IN1	Open
L0~L33	Open

Chapter 2

POWER SUPPLY SYSTEM

2. Power Supply System

2.1 Summary

The MSM64P164 (OTP chip) is manufactured using EPROM process for the N-well that is different from the P-well CMOS structure of the mask ROM of MSM64164 (mask ROM chip). Because of this, the polarity of the power supply system is completely reversed when compared to the mask ROM chip. In addition, note that the names of the power supply pins have also been changed.

Table 2-1 shows a table of the power supply pin functions and Table 2-2 shows the differences between the MSM64164 and the MSM64P164.

Table 2-1 List of Power Supply Pin Functions

Pin Name	Pin No.	Input/ Output	Function
VSS	32, 67	—	0V power supply
VDD1	42	—	Plus side power supply (for 1.5V specifications) Bias output for LCD drive (+1.5V) (for 3.0V specifications)
VDD2	44	—	Plus side power supply (for 3.0V specifications) Bias output for LCD drive (+3.0V) (for 1.5V specifications)
VDD3	45	—	Bias output for LCD drive (+4.5V)
VDD	43	—	Plus side power supply for input/output port interface
VPP	31	—	Plus side power supply for PROM write (+12.5V)

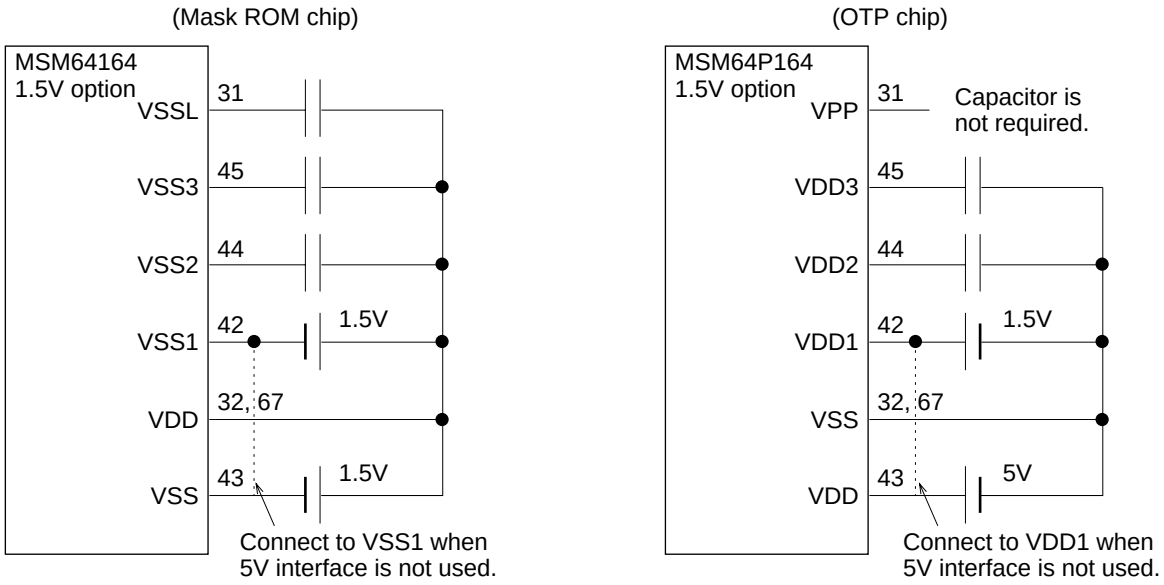
Table 2-2 Differences between the MSM64P164 and the MSM64164

MSM64P164	MSM64164	Different from Mask ROM Chip:
VSS (0V)	VDD (0V)	—
VDD1 (+1.5V)	VSS1 (-1.5V)	Power supply has reversed phase with 1.5V specifications
VDD2 (+3.0V)	VSS2 (-3.0V)	Power supply has reversed phase with 3.0V specifications
VDD3 (+4.5V)	VSS3 (-4.5V)	—
VDD	VSS	Power supply has reversed phase with 5V interface.
VPP (+12.5V)	VSSL	No external capacitor is required

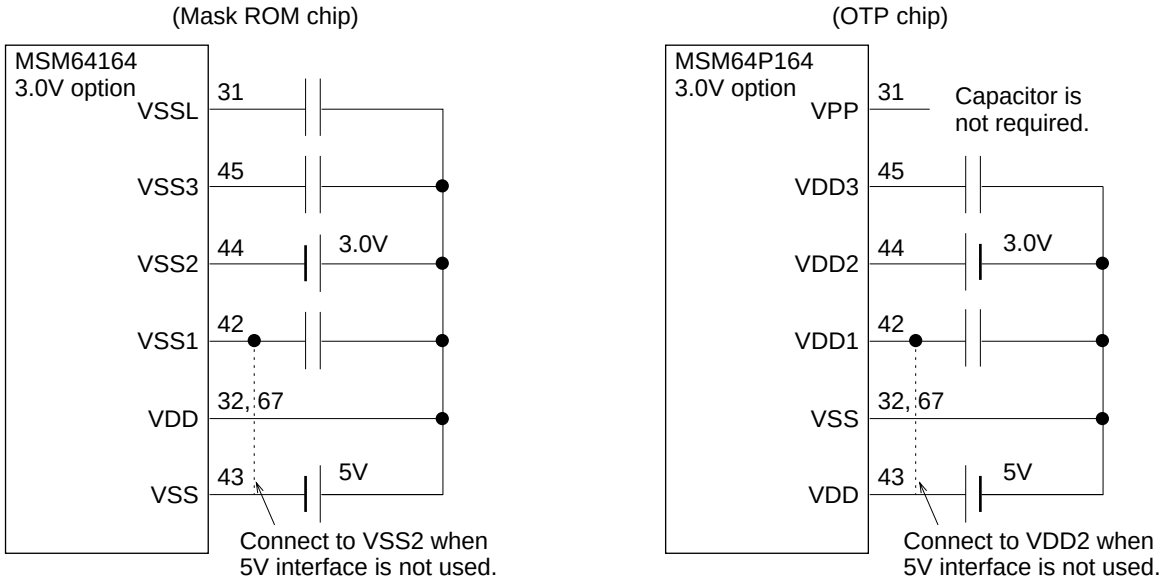
2.2 Circuit Configuration of the Power Supply System

2.2.1 Power Supply Circuit Configuration for IC

Figure 2-1 shows the circuit configuration of the power supply for IC including the differences between the MSM64P164 and the mask ROM chip MSM64164.



(a) Configuration of the power supply system with the 1.5V option

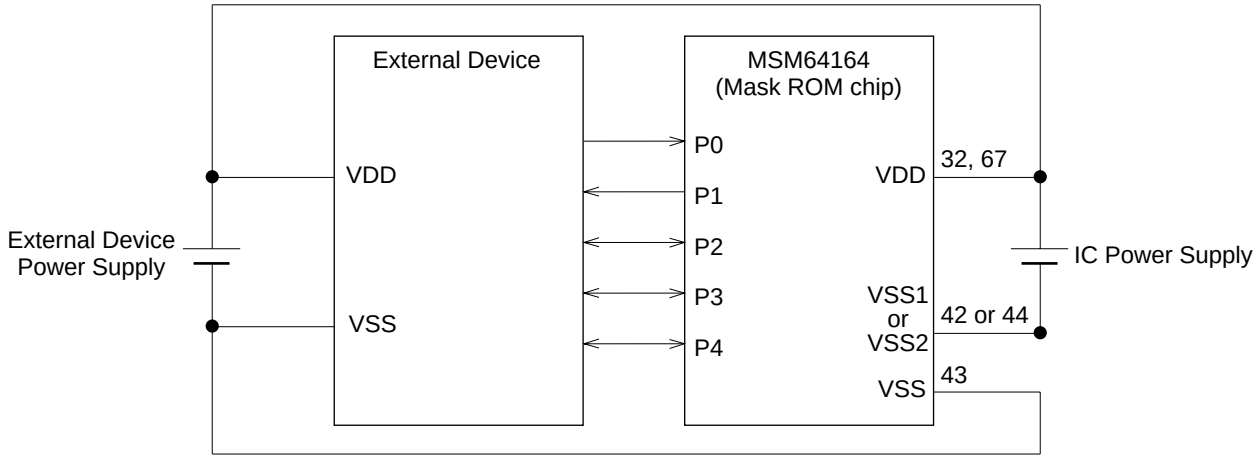


(b) Configuration of the power supply system with the 3.0V option

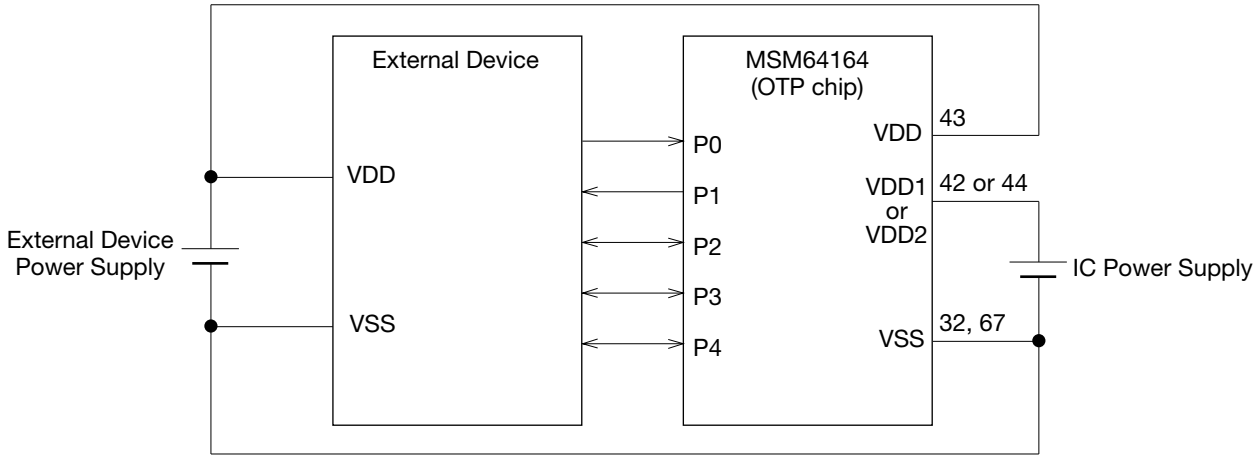
Figure 2-1 Circuit Configuration of the Power Supply System

2.2.2 Circuit Configuration for 5V Interface

The power supplies for the input circuit of port 0, the output circuit of port 1, and the input/output circuit of port 2, 3 or 4 are shown as VDD-VSS levels. However, as shown in Figure 2-1, the polarity of the power suply for a 5V interface is different from the MSM64164 chip. Figure 2-2 shows differences for the circuit configuration between the mask ROM chip and the OTP chip in the case of connecting ports 0 to 4 to a device that operates with another external power supply.
In addition, if all the port-signal levels of the port 0, port 1 and ports 2 to 4 are the same as the IC power supply voltage levels, be sure to connect the VDD pin to VDD1 or VDD2.



(a) Circuit Configuration for the MSM64164



(b) Circuit Configuration for the MSM64P164

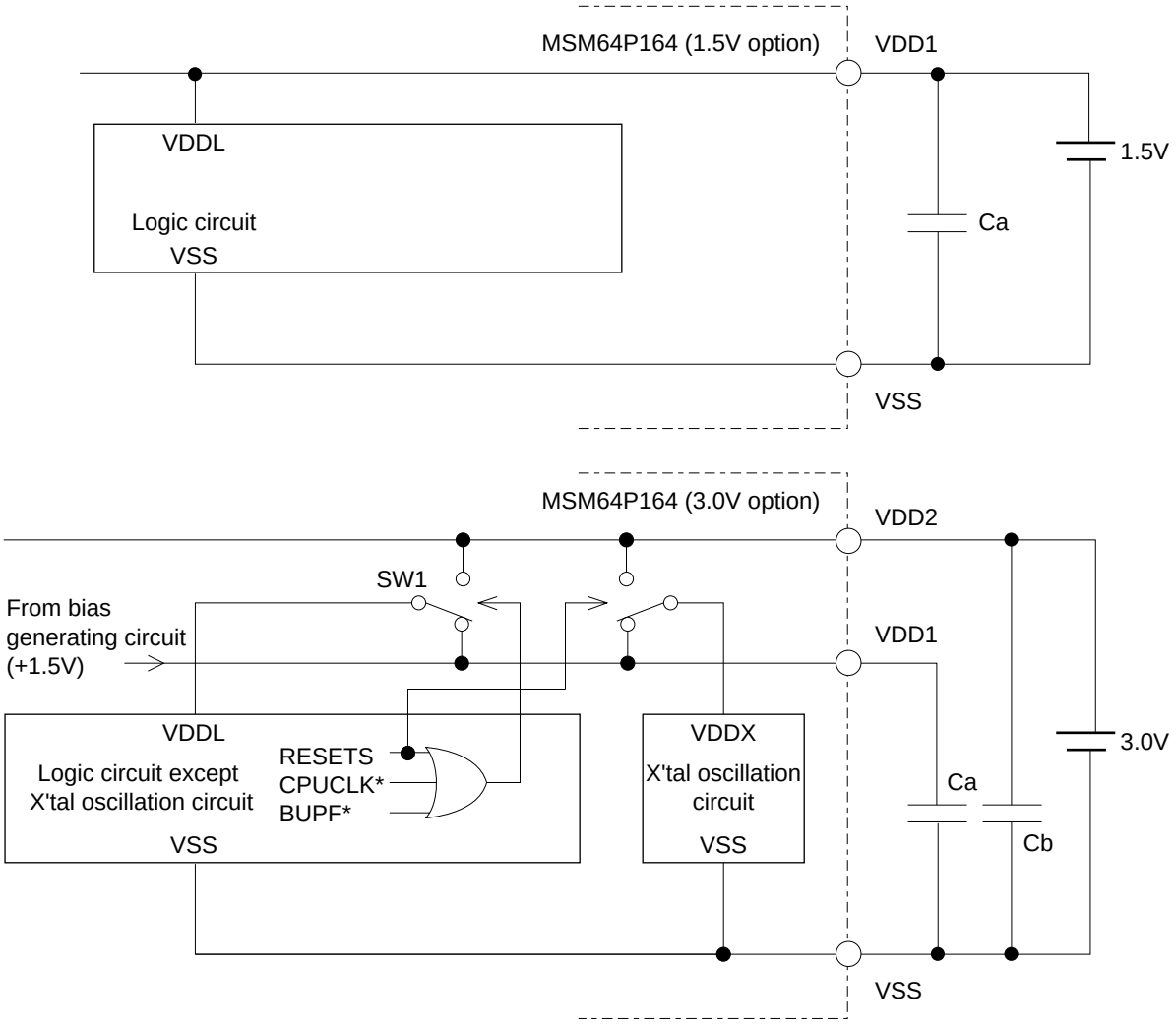
Figure 2-2 Circuit Configuration to Connect Ports 0 to 4 to an External Device with a Different Power Supply

2.3 Logic Power Supply

The MSM64P164 has no built-in logic power supply constant voltage (VR). Internal logic circuit is driven by VDD1 of the lowest voltage level insted. Therefore, the power supply voltage is driven by the 1.5V option and the 1/2 descending output voltage is driven by the 3.0V option. The crystal oscillation circuit power supply uses a different driving method from the logic power supply for the 3.0V option that differs from the mask ROM chip.

2.3.1 Configuration of the Logic Power Supply Driving Circuits

Figure 2-3 shows the configuration of driving circuits of the logic power supply.



* BUPF shows the output of a back-up flag.
CPUCLK shows the output of a system clock selecting bit.

Figure 2-3 Logic Power Supply Driving Circuits

2.3.2 Operations of Optional 1.5V Logic Power Supply Circuits

1.5V optional logic power supply circuits are supplied as a power supply with ordinary logic circuits for IC power supply voltage VDD1.

2.3.3 Operations of Optional 3.0V Logic Power Supply Circuits

In the 3.0V option, IC power supply voltage VDD2 is supplied to the logic circuit except the crystal oscillation circuit in the system reset mode, in the selection of the 400kHz CR oscillation output as the system clock (CPUCLK="1"), and in setting the bit (BUPF) of the back-up control register (BUPCON) to 1, and 1/2 descending output voltage is supplied for other modes than these.
In addition, IC power supply voltage VDD2 in supplied to the crystal oscillation circuit in the system reset mode only, and VDD1 is supplied for other modes than this.

In the system reset mode, BUPF is reset to "0", but the logic voltagae becomes the VDD2 level during 0.5 sec as shown in Figure 2-4. Table 2-3 shows the logic voltage status with the operational mode, CPUCLK bit, and BUPF flag. Figure 2-4 shows the logic voltage status just after the system reset mode.

Table 2-3 Logic Voltage Status

Operational Mode	CPUCLK Flag	BUPF Flag	Logic Voltage (VDDL) except x'tal oscillationcircuit	X'tal oscillation circuit voltage (VDDX)
System reset mode and druing 0.5 sec just after this mode	—	—	VDD2	VDD2
Except the above	0	0	VDD1	VDD1
	0	1	VDD2	
	1	—	VDD2	

(Standard: VSS)

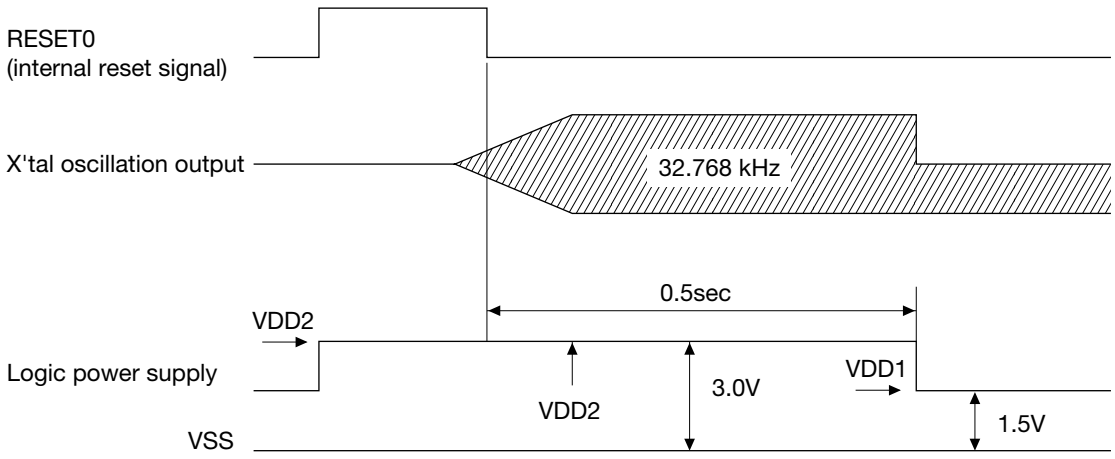


Figure 2-4 Logic Power Supply Status just after System Reset Mode (3.0V Option)

2.4 LCD Bias Level

From the difference of the porality in the power supply system, LCD bias levels are different between the mask ROM chip and the OTP chip.
Table 2-4 shows the both differences.

Table 2-4 Difference of LCD Bias Levels

MSM64164	MSM64P164
VDD	VSS
VSS1	VDD1
VSS2	VDD2
VSS3	VDD3

Chapter 3

X'TAL OSCILLATION CIRCUITS

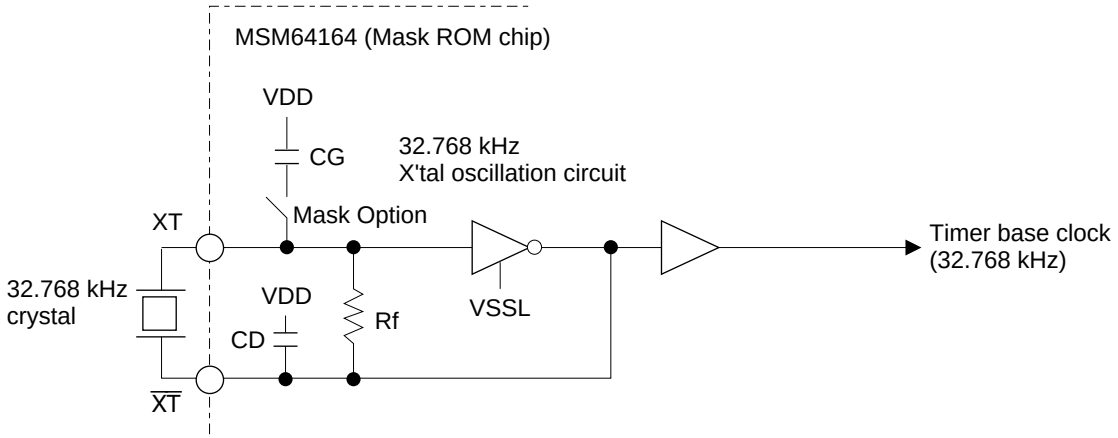
3. X’tal Oscillation Circuits

3.1 Summary

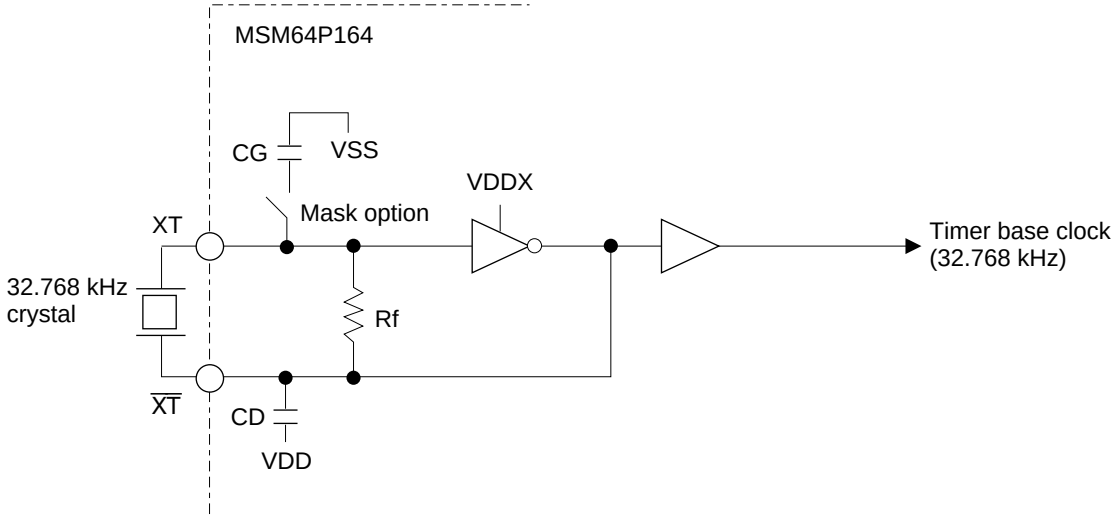
The X’tall oscillation circuit, oscillating at 32.768 kHz and being included in a clock oscillation circuit (2CLK), can be used for fine adjustment by an external capacitor, with cutting a built-in capacity (CG) by a mask option, but since the phase of the power supply of the MSM64P164 is opposite to the MSM64164, mount an external capacitor CGEX between VSS and XT pin.

3.2 Configuration of X’tal Oscillation Circuits

Figure 3-1 shows the configuration of the X’tal oscillation circuit both the MSM64164 (mask ROM chip) and the MSM64P164.



(a) Configuration of X'tal Oscillation Circuit for the MSM64164



(b) Configuration of X'tal Oscillation Circuit for the MSM64P164

Figure 3-1 Configuration of X’tal Oscillation Circuits

Chapter 4

PROM

4. PROM

4.1 Summary

The MSM64P164 uses built-in PROM as program memory. The capacity of this PROM is 4064 bytes, and the capacity that omitted 32 bytes from the 0FE0H address to the 0FFFH address, forming the test data area of the mask ROM chip.

In order to write the program data to this PROM, the MSM64P164 uses a special adapter (OTP 64164F BOARD) which is connected to the general EPROM writer for writing. See also the manual of this special adapter for further reference.

4.2 Explanation of Pins

Table 4-1 shows PROM related pins of the MSM64P164.

Table 4-1 (a) List of PROM Related Pins

Pin Name	Pin No.	Input/ Output	Remarks
VSS	32, 67	—	0V power supply
VDD1	42	—	Plus side power supply pin (+5V supplied)
VDD2	44	—	Plus side power supply pin(+5V supplied)
VPP	31	—	Power supply for PROM writing (+12.5V supplied)
$\overline{\text{RESET}}$	70	Input	PROM mode setting pin PROM mode is activated when the L level is input for 3 common pins
$\overline{\text{TST1}}$	71	Input	
$\overline{\text{TST2}}$	72	Input	

Table 4-1 (b) List of PROM Related Pins

Pin Name	Pin No.	Input/ Output	Function
L0/D0	1	I/O	Program data write and read pins
L1/D1	2	I/O	
L2/D2	3	I/O	
L3/D3	4	I/O	
L4/D4	5	I/O	
L5/D5	6	I/O	
L6/D6	7	I/O	
L7/D7	8	I/O	
L8/$\overline{CE}$	9	Input	PROM chip enable pin
L9/$\overline{OE}$	10	Input	PROM output enable signal
L10/A0	11	Input	Program address input pins
L11/A1	12	Input	
L12/A2	13	Input	
L13/A3	14	Input	
L14/A4	15	Input	
L15/A5	16	Input	
L16/A6	17	Input	
L17/A7	48	Input	
L18/A8	49	Input	
L19/A9	50	Input	
L20/A10	51	Input	
L21/A11	52	Input	
L22	53	Input	Input H level

4.3 PROM Mode

MSM64P164 is capable of two separate modes, an PROM mode, which is used to write to PROM and read from PROM, and a computer operating mode, which is used to execute programs written to PROM. When MSM64P164 is in the PROM mode, it simply operates as PROM. These operations are explained under PROM mode.

4.3.1 Setting the PROM Mode

Setting of the PROM mode is done with $\overline{\text{RESET}}$, $\overline{\text{TST1}}$, and $\overline{\text{TST2}}$, listed in Table 4-2. When the PROM mode is set, LCD pins become PROM related pins.

Table 4-2 PROM Mode Setting

$\overline{\text{RESET}}$	$\overline{\text{TST1}}$	$\overline{\text{TST2}}$	MODE
L	L	L	PROM Mode

4.3.2 PROM Mode Functions

PROM Mode functions are shown in Table 4-3.

Table 4-3 List of PROM Mode Functions

MODE	$\overline{\text{CE}}$	$\overline{\text{OE}}$	VPP	VDD1 VDD2	D7~D0
Read	L	L	5V	5V	Program data output
Program	L	H	12.5V	5V	Program data input
Program Verify	L	L	12.5V	5V	Program data output

4.3.3 Connection to the EPROM Writer

Figure 4-1 shows how to connect the EPROM writer to the MSM64P164.

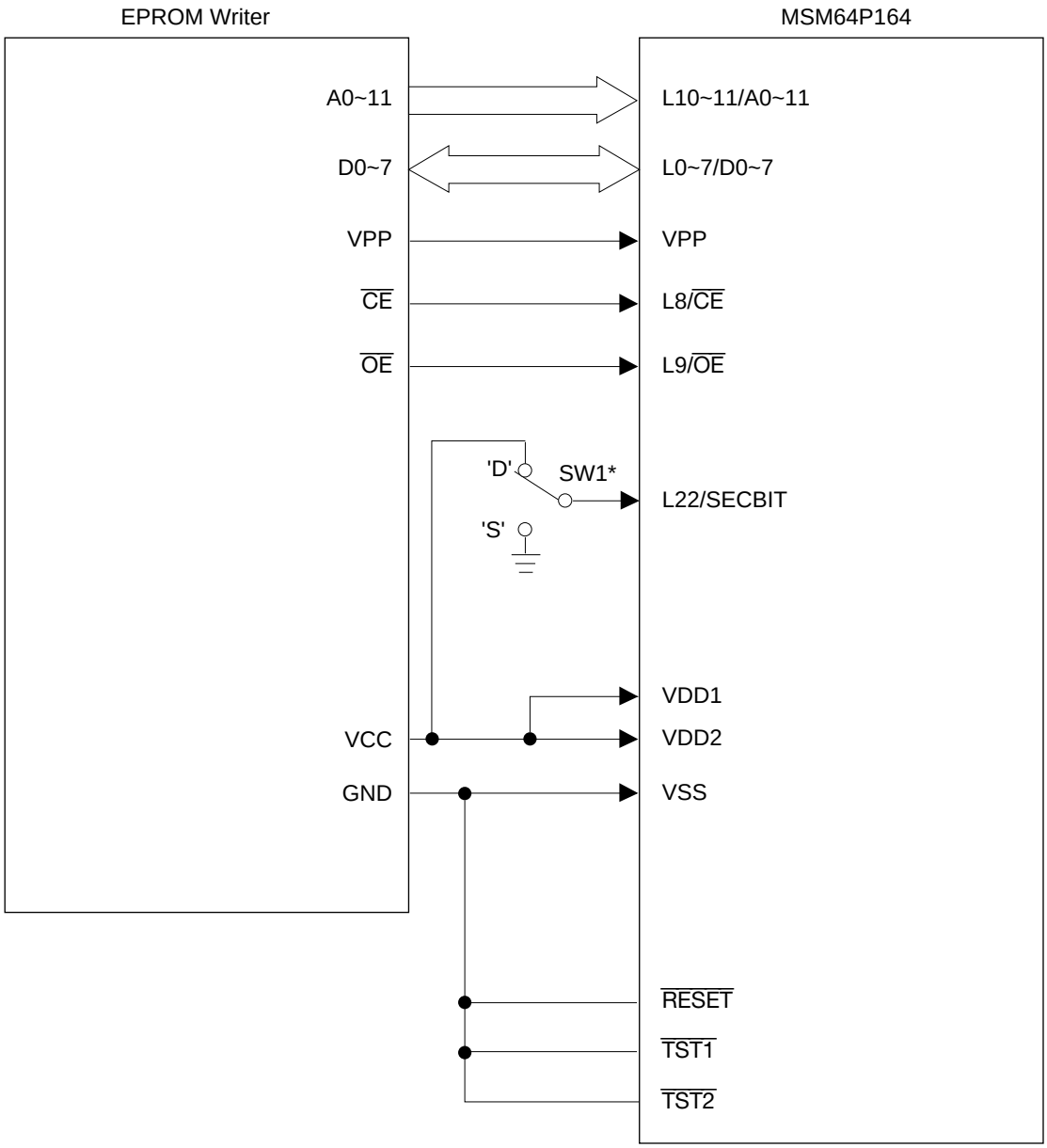


Figure 4-1 Connection to the EPROM Writer

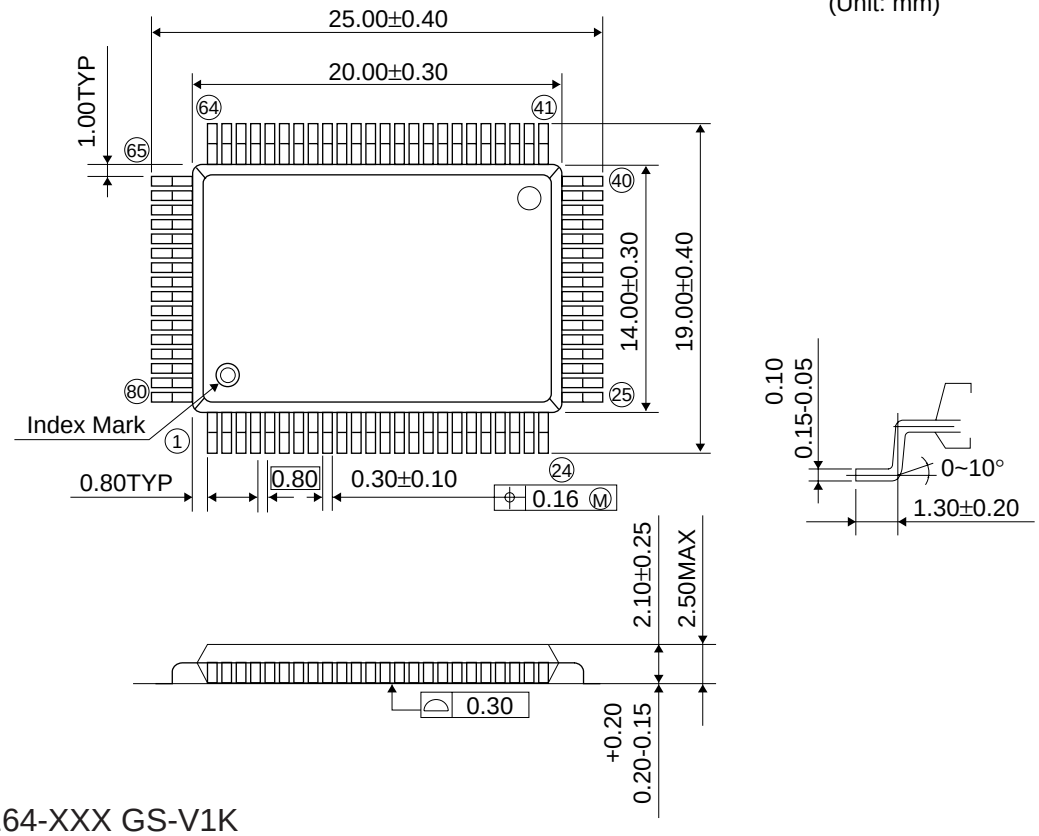
Note: *denotes to set SW1 to 'D'.

APPENDIXES

Appendix A Diagram of Package Measurements

MSM64P164-XXX GS-K

(Unit: mm)



MSM64P164-XXX GS-V1K

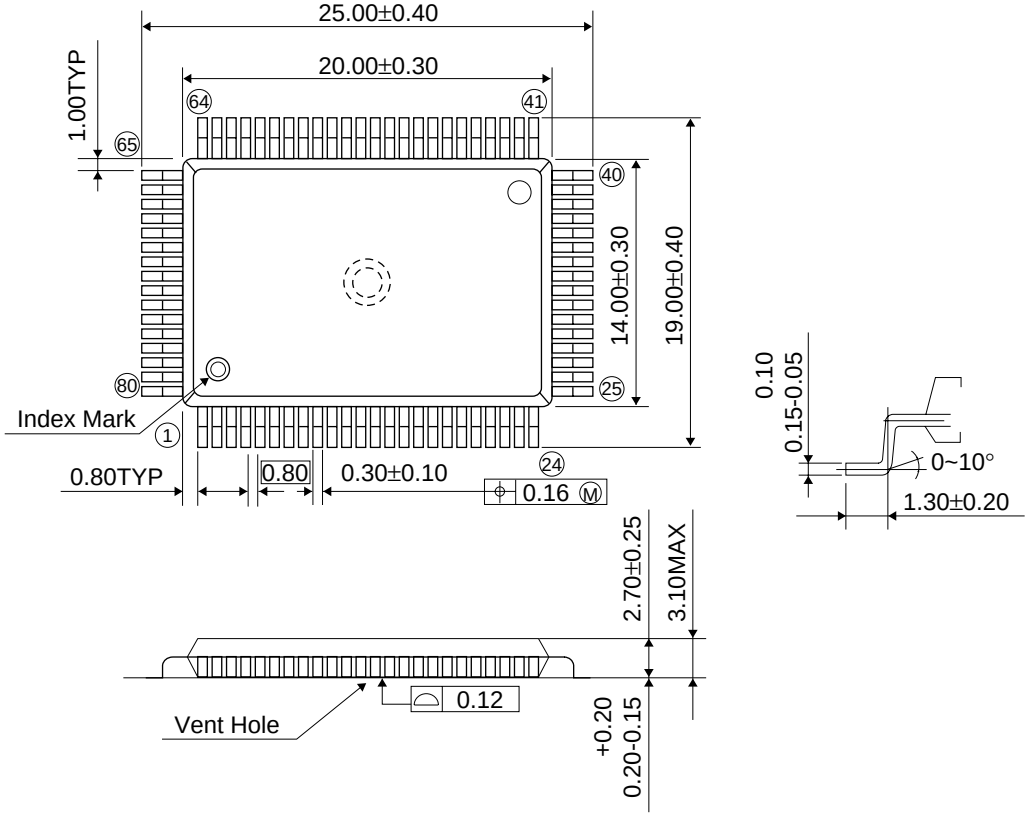
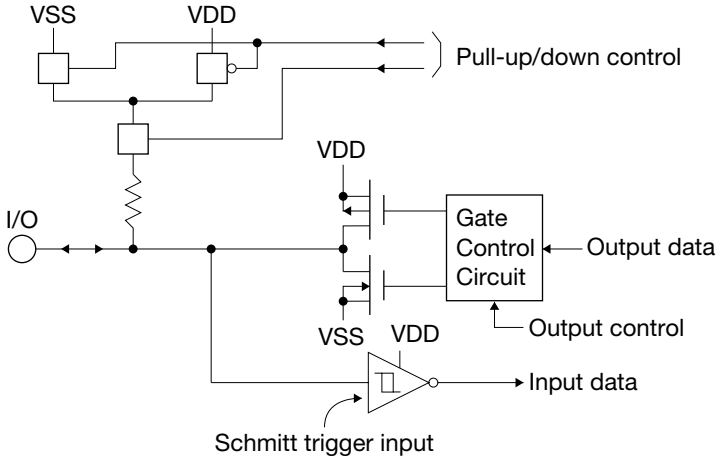


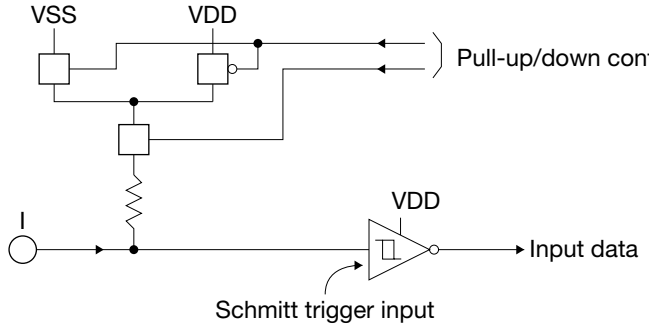
Figure A-1 80 Pin QFP Package Measurements

Appendix B Input and Output Circuit Configurations

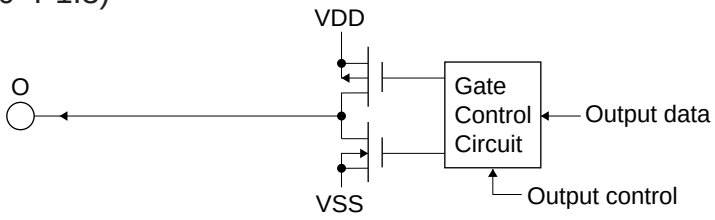
A. Input/ouput port (P2.0~P2.3, P3.0~P3.3, P4.0~P4.3)



B. Input port (P0.0~P0.3)



C. Ouput port (P1.0~P1.3)

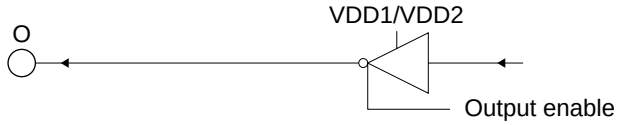


D. Ouput port (L26/P5.0~L29/P5.3, L30/P6.0~L33/P6.3 pins in mask options)

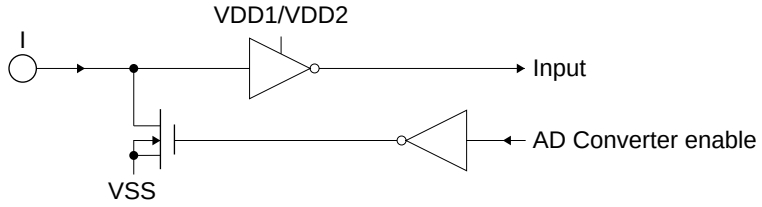
E. BD, CS1 output

(Note) VDD1/VDD2:
VDD1 in 1.5V specifications
VDD2 in 3.0V specifications

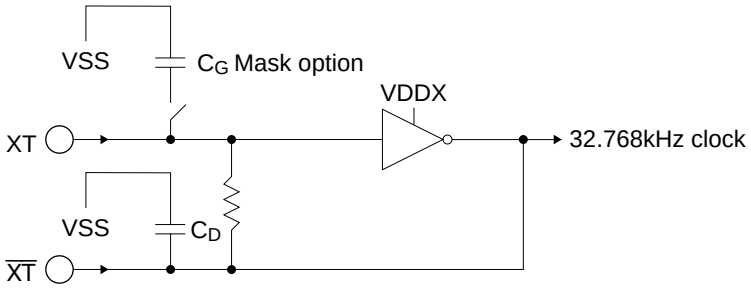
F. RS0, RS1, RT0, RT1, CS0, CRT0 output



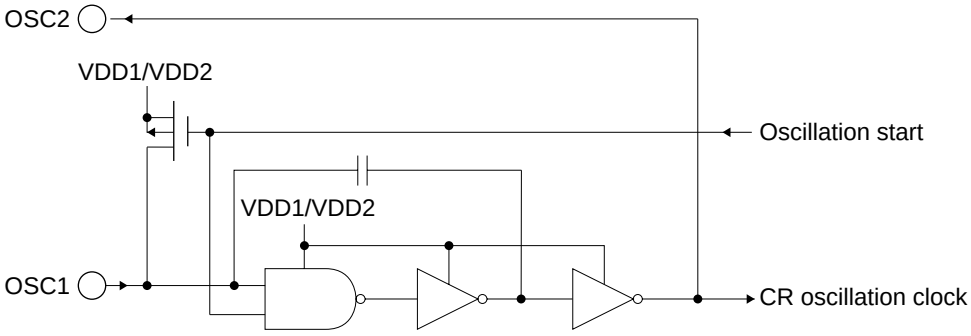
G. IN0, IN1 input



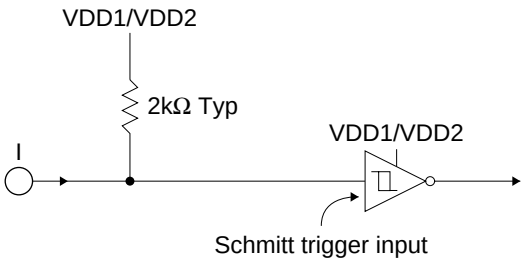
H. X'tal oscillation circuit



I. 400kHz oscillation circuit



J. $\overline{RESET}$, $\overline{TST1}$, $\overline{TST2}$ input



Appendix C Examples of Application Circuits

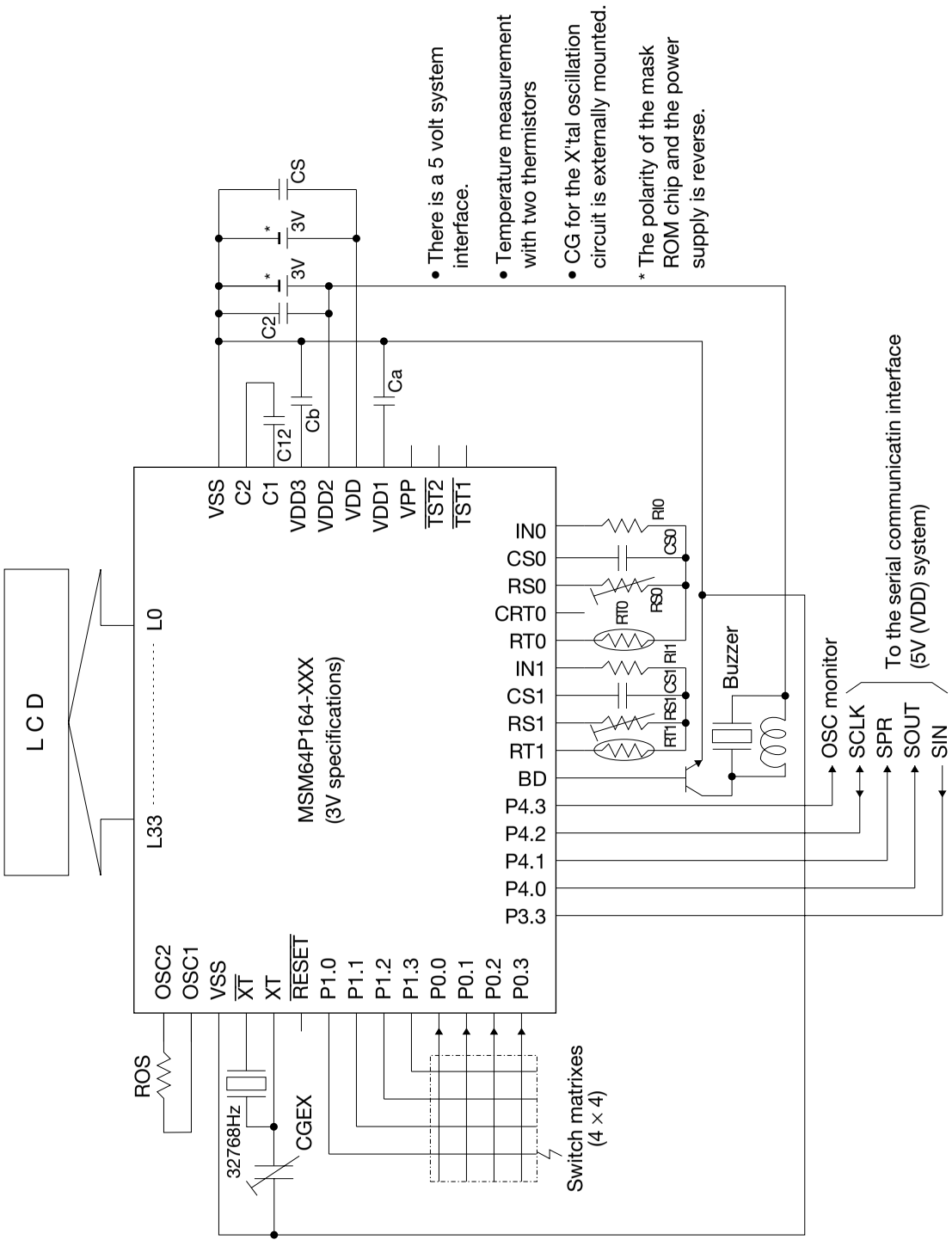


Figure C-1 Example of 3V Specifications Application Circuit

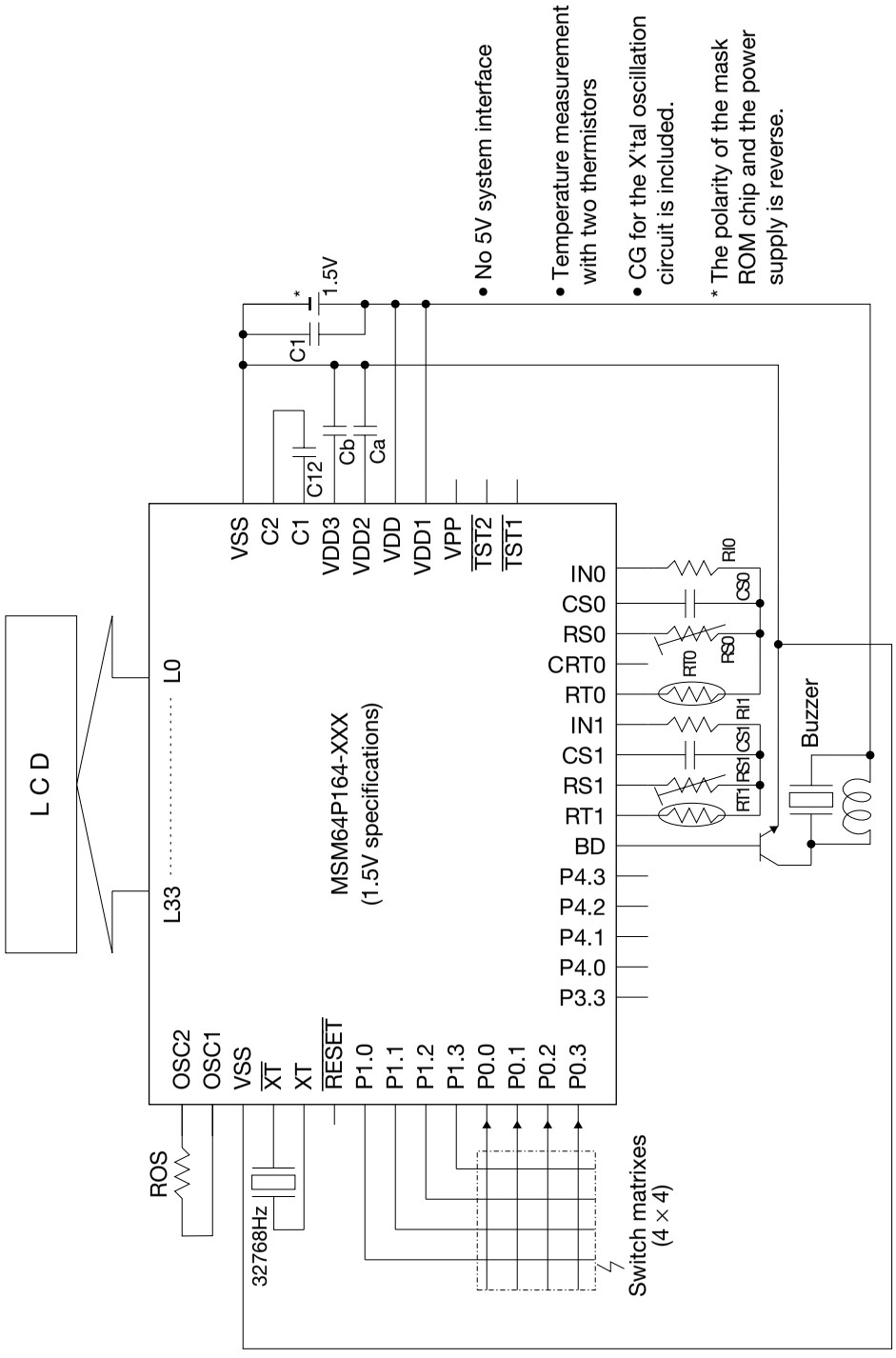


Figure C-2 Example of 1.5V Specifications Application Circuit

Appendix D Mask Options

The method to set mask optins, see "MSM64164 User's Manual" because this is the same as the mask ROM chip.
Standard mask option products prepared to use merit of the software development during a short period for the OTP version are shown.
The standard mask option products are previously separated by code numbers. It is shown in Table D-1.

Table D-1 Line-up of Standard Mask Option Products

Code Name	Power Supply Voltage		Built-in CG	LCD Allocation
	1.5V	3V		
001	❍	—	—	See Table 1 for the mask option allocation.
002	—	❍	❍	See Table 1 for the mask option allocation.
003	❍	—	—	See Table 2 for the mask option allocation.
004	—	❍	❍	See Table 2 for the mask option allocation.

- **LCD driver Mask Option Allocation Table1 (1/4 duty)**

SEG	SIGNAL				C/S/P	COM1		COM2		COM3		COM4	
						DATA	DSPR	DATA	DSPR	DATA	DSPR	DATA	DSPR
L0	COM1	/	/	/	C	—	—	—	—	—	—	—	—
L1		/COM2	/	/	C	—	—	—	—	—	—	—	—
L2		/	COM3	/	C	—	—	—	—	—	—	—	—
L3		/	/	/COM4	C	—	—	—	—	—	—	—	—
L4	SG1	/SG2	/SG3	/SG4	S	a	0	b	0	c	0	d	0
L5	SG5	/SG6	/SG7	/SG8	S	a	1	b	1	c	1	d	1
L6	SG9	/SG10	/SG11	/SG12	S	a	2	b	2	c	2	d	2
L7	SG13	/SG14	/SG15	/SG16	S	a	3	b	3	c	3	d	3
L8	SG17	/SG18	/SG19	/SG20	S	a	4	b	4	c	4	d	4
L9	SG21	/SG22	/SG23	/SG24	S	a	5	b	5	c	5	d	5
L10	SG25	/SG26	/SG27	/SG28	S	a	6	b	6	c	6	d	6
L11	SG29	/SG30	/SG31	/SG32	S	a	7	b	7	c	7	d	7
L12	SG33	/SG34	/SG35	/SG36	S	a	8	b	8	c	8	d	8
L13	SG37	/SG38	/SG39	/SG40	S	a	9	b	9	c	9	d	9
L14	SG41	/SG42	/SG43	/SG44	S	a	10	b	10	c	10	d	10
L15	SG45	/SG46	/SG47	/SG48	S	a	11	b	11	c	11	d	11
L16	SG49	/SG50	/SG51	/SG52	S	a	12	b	12	c	12	d	12
L17	SG53	/SG54	/SG55	/SG56	S	a	13	b	13	c	13	d	13
L18	SG57	/SG58	/SG59	/SG60	S	a	14	b	14	c	14	d	14
L19	SG61	/SG62	/SG63	/SG64	S	a	15	b	15	c	15	d	15
L20	SG65	/SG66	/SG67	/SG68	S	a	16	b	16	c	16	d	16
L21	SG69	/SG70	/SG71	/SG72	S	a	17	b	17	c	17	d	17
L22	SG73	/SG74	/SG75	/SG76	S	a	18	b	18	c	18	d	18
L23	SG77	/SG78	/SG79	/SG80	S	a	19	b	19	c	19	d	19
L24	SG81	/SG82	/SG83	/SG84	S	a	20	b	20	c	20	d	20
L25	SG85	/SG86	/SG87	/SG88	S	a	21	b	21	c	21	d	21
L26	SG89	/SG90	/SG91	/SG92	S	a	22	b	22	c	22	d	22
L27	SG93	/SG94	/SG95	/SG96	S	a	23	b	23	c	23	d	23
L28	SG97	/SG98	/SG99	/SG100	S	a	24	b	24	c	24	d	24
L29	SG101	/SG102	/SG103	/SG104	S	a	25	b	25	c	25	d	25
L30	SG105	/SG106	/SG107	/SG108	S	a	26	b	26	c	26	d	26
L31	SG109	/SG110	/SG111	/SG112	S	a	27	b	27	c	27	d	27
L32	SG113	/SG114	/SG115	/SG116	S	a	28	b	28	c	28	d	28
L33	SG117	/SG118	/SG119	/SG120	S	a	29	b	29	c	29	d	29

- **LCD driver Mask Option Allocation Table2 (1/4 duty)**

SEG	SIGNAL				C/S/P	COM1		COM2		COM3		COM4	
						DATA	DSPR	DATA	DSPR	DATA	DSPR	DATA	DSPR
L0	COM1	/	/	/	C	—	—	—	—	—	—	—	—
L1		/COM2	/	/	C	—	—	—	—	—	—	—	—
L2		/	COM3	/	C	—	—	—	—	—	—	—	—
L3		/	/	/COM4	C	—	—	—	—	—	—	—	—
L4	SG1	/SG2	/SG3	/SG4	S	a	2	b	2	c	2	d	2
L5	SG5	/SG6	/SG7	/SG8	S	a	3	b	3	c	3	d	3
L6	SG9	/SG10	/SG11	/SG12	S	a	4	b	4	c	4	d	4
L7	SG13	/SG14	/SG15	/SG16	S	a	5	b	5	c	5	d	5
L8	SG17	/SG18	/SG19	/SG20	S	a	6	b	6	c	6	d	6
L9	SG21	/SG22	/SG23	/SG24	S	a	7	b	7	c	7	d	7
L10	SG25	/SG26	/SG27	/SG28	S	a	8	b	8	c	8	d	8
L11	SG29	/SG30	/SG31	/SG32	S	a	9	b	9	c	9	d	9
L12	SG33	/SG34	/SG35	/SG36	S	a	10	b	10	c	10	d	10
L13	SG37	/SG38	/SG39	/SG40	S	a	11	b	11	c	11	d	11
L14	SG41	/SG42	/SG43	/SG44	S	a	12	b	12	c	12	d	12
L15	SG45	/SG46	/SG47	/SG48	S	a	13	b	13	c	13	d	13
L16	SG49	/SG50	/SG51	/SG52	S	a	14	b	14	c	14	d	14
L17	SG53	/SG54	/SG55	/SG56	S	a	15	b	15	c	15	d	15
L18	SG57	/SG58	/SG59	/SG60	S	a	16	b	16	c	16	d	16
L19	SG61	/SG62	/SG63	/SG64	S	a	17	b	17	c	17	d	17
L20	SG65	/SG66	/SG67	/SG68	S	a	18	b	18	c	18	d	18
L21	SG69	/SG70	/SG71	/SG72	S	a	19	b	19	c	19	d	19
L22	SG73	/SG74	/SG75	/SG76	S	a	20	b	20	c	20	d	20
L23	SG77	/SG78	/SG79	/SG80	S	a	21	b	21	c	21	d	21
L24	SG81	/SG82	/SG83	/SG84	S	a	22	b	22	c	22	d	22
L25	SG85	/SG86	/SG87	/SG88	S	a	23	b	23	c	23	d	23
L26	P0	/	/	/	P	a	0	—	—	—	—	—	—
L27	P1	/	/	/	P	b	0	—	—	—	—	—	—
L28	P2	/	/	/	P	c	0	—	—	—	—	—	—
L29	P3	/	/	/	P	d	0	—	—	—	—	—	—
L30	P4	/	/	/	P	a	1	—	—	—	—	—	—
L31	P5	/	/	/	P	b	1	—	—	—	—	—	—
L32	P6	/	/	/	P	c	1	—	—	—	—	—	—
L33	P7	/	/	/	P	d	1	—	—	—	—	—	—

Appendix E Electrical Characteristics

(1) For 1.5V specifications in the microcontroller operation mode

- **Absolute Maximum Ratings**

(VSS=0V)

Prameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	VDD1	Ta = 25°C	-0.3 ~ +2.0	V
Power supply voltage 2	VDD2	Ta = 25°C	-0.3 ~ +4.0	V
Power supply voltage 3	VDD3	Ta = 25°C	-0.3 ~ +5.5	V
Power supply voltage 5	VDD	Ta = 25°C	-0.3 ~ +5.5	V
Input voltage 1	VIN1	VDD1 system input, Ta = 25°C	-0.3 ~ VDD1+0.3	V
Input voltage 2	VIN2	VDD system input, Ta = 25°C	-0.3 ~ VDD+0.3	V
Output voltage 1	VOUT1	VDD1 system output, Ta = 25°C	-0.3 ~ VDD1+0.3	V
Output voltage 2	VOUT2	VDD2 system output Ta = 25°C,	-0.3 ~ VDD2+0.3	V
Output voltage 3	VOUT3	VDD3 system output, Ta = 25°C	-0.3 ~ VDD3+0.3	V
Output voltage 4	VOUT4	VDD system output, Ta = 25°C	-0.3 ~ VDD+0.3	V
Storage temperature	TSTG	—	-55 ~ +125	°C

- **Recommended Operating Conditions**

(VSS=0V)

Prameter	Symbol	Condition	Rating	Unit
Operating temperature	TOPE	—	0 ~ +65	°C
Operating voltage	VDD1	—	1.35 ~ 1.7	V
	VDD	—	VDD1 ~ 5.25	V
400kHz OSC external resistance	ROS	—	250 ~ 500	kΩ
X'tal OSC oscillation frequency	fXT	—	30 ~ 35	kHz

- **DC Characteristics**
  (Unless otherwise specified, VSS=0V, VDD1=VDD=1.5V, Ta=0~65˚C)

(1/3)

Parameter (Relevant pin name)	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measure-ment Circuit
VDD2 voltage	VDD2	Ca, Cb, C12=0.1μF +100% - 50%		2.8	3.0	3.2	V	
VDD3 voltage	VDD3	Ca, Cb, C12=0.1μF +100% - 50%		4.3	4.5	4.7	V	
XTOSC oscillation beginning voltage	VSTA	Within 5 seconds from the beginning of an oscillation		1.45	—	—	V	
XTOSC oscillation maintaining voltage	VHOLD	—		1.35	—	—	V	
XTOSC stop detecting time	TSTOP	—		0.1	—	1000	ms	
XTOSC internal capacity	CG	—		10	15	20	pF	
XTOSC external capacity	CGEX	When CG is an external option.		10	—	30	pF	
XTOSC internal capacity	CD	—		10	15	20	pF	
400kOSC internal capacity	COS	—		8	12	16	pF	
400kOSC oscillation frequency	fOSC	External resistance ROS=300kΩ VDD1=1.25 ~ 1.7V		80	220	350	kHz	1
POR generating voltage	VPOR1	POR is generated when VDD1 varies from VPROR 1 to 1.5V.		0	—	0.4	V	
POR non-generating voltage	VPOR2	There is no POR when VDD1 varies from VPROR 2 to 1.5V.		1.2	—	1.5	V	
Current consumption 1	IDD1	CPU is in the HALT mode (400kOSC stop)		—	2	5	μA	
Current consumption 2	IDD2	CPU is in the operating mode (400kOSC stop)		—	20	50	μA	
Current consumption 3	IDD3	CPU is in the operating mode (400kOSC operation)		—	90	180	μA	
Current consumption 4	IDD4	CPU is in the operating mode in the serial transfer. (400kOSC stop)		—	20	50	μA	
Current consumption 5	IDD5	The CR oscillator for an A/D converter opeartes. CPU is in the HALT mode. (400kOSC stop)	RT0=10kΩ	—	150	230	μA	
			RT0=2kΩ	—	600	900	μA	

(Note)
- "XTOSC" indicates a X'tal oscillation circuit at 32.768kHz.
- "400kOSC" indicates a 400kHz CR oscillation circuit.
- "POR" indicates a X'tal oscillation circuit at 32.768kHz.
- "TSTOP" indicates to generate a system reset when XTOSC stops oscillation during more than the time of TSTOP.

- **DC Characteristics**
  (Unless otherwise specified, VSS=0V, VDD1=VDD=1.5V, VDD2=3.0V, VDD3=4.5V, Ta=0~65˚C)

(2/3)

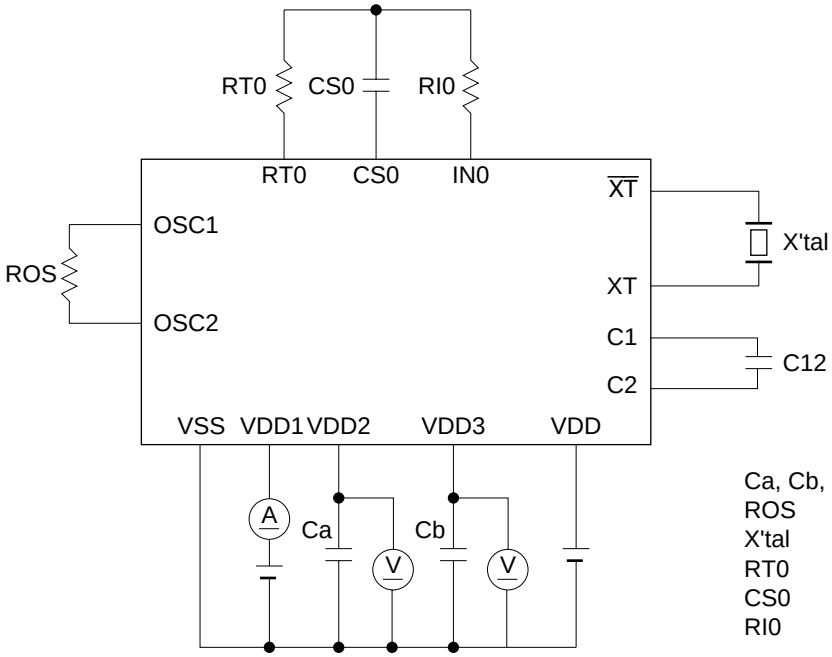
Parameter (Relevant pin name)	Symbol	Condition	Rating			Unit	Measure-ment Circuit
			Min.	Typ.	Max.		
Output current 1 (P1.0)	IOH1	VOH1=VDD-0.5V	-2.1	-0.7	-0.2	mA	2
	IOL1	VOL1=0.5V	1	3	9	mA	
	IOL1S	VDD=5V, VOL1=0.5V	4	12	36	mA	
Output current 2 (P1.1 ~ P1.3) (P2.0 ~ P2.3) (P3.0 ~ P3.3) (P4.0 ~ P4.3)	IOH2	VOL2=VDD-0.5V	-2.1	-0.7	-0.2	mA	
	IOL2	VOL2=0.5V	0.2	0.7	2.1	mA	
	IOL2S	VDD=5V, VOL2=0.5V	1	3	9	mA	
Output current 3 (BD)	IOH3	VOH3=VDD1-0.7V	-1.8	-0.6	-0.2	mA	
	IOL3	VOL3=0.7V	0.2	0.6	1.8	mA	
Output current 4 (RT0, RT1, RS0, RS1, CRT0, CS0, CS1)	IOH4	VOH4=VDD1-0.1V	-1.1	-0.6	-0.3	mA	
	IOL4	VOL4=0.1V	0.3	0.6	1.1	mA	
Output current 5 (When the pins L26 to L33 are set to output ports.)	IOH5	VOL5=VDD-0.5V	-1.5	-0.5	-0.1	mA	
	IOL5	VOL5=0.5V	0.1	0.5	1.5	mA	
	IOL5S	VDD=5V, VOL5S=0.5V	0.2	0.7	2.0	mA	
Output current 6 (OSC2)	IOH6	VOH6=VDD1-0.5V	-2.1	-0.7	-0.2	mA	
	IOL6	VOL6=0.5V	0.2	0.7	2.1	mA	
Output current 7 (L0 ~ L33)	IOH7	VOH7=VDD3-0.2V (VDD3 level)	—	—	-4	µA	—
	IOMH7	VOMH7=VDD2+0.2V (VDD2 level)	4	—	—	µA	
	IOMH7S	VOMH7S=VDD2-0.2V (VDD2 level)	—	—	-4	µA	
	IOML7	VOML7=VDD1+0.2V (VDD1 level)	4	—	—	µA	
	IOML7S	VOML7S=VDD1-0.2V (VDD1 level)	—	—	-4	µA	
	IOL7	VOL7=VSS+0.2V (VSS level)	4	—	—	µA	
Output leak (P1.0 ~ P1.3) (P2.0 ~ P2.3) (P3.0 ~ P3.3) (P4.0 ~ P4.3) (RT0, RT1, RS0, RS1, CRT0, CS0, CS1)	IOOH	VOH=VDD1	—	—	0.3	µA	
	IOOL	VOL=VSS	-0.3	—	—	µA	

- **DC Characteristics**
  (Unless otherwise specified, VSS=0V, VDD1=VDD=1.5V, VDD2=3.0V, VDD3=4.5V, Ta=0~65˚C)

(3/3)

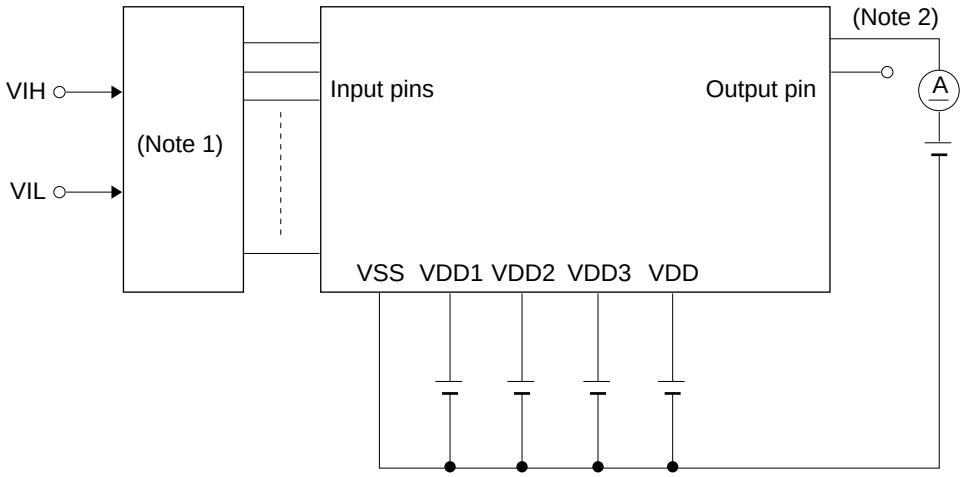
Parameter (Relevant pin name)	Symbol	Condition	Rating			Unit	Measure-ment Circuit
			Min.	Typ.	Max.		
Input current 1 (P0.0 ~ P0.3) (P2.0 ~ P2.3) (P3.0 ~ P3.3) (P4.0 ~ P4.3)	IIH1	VIH1=VDD (for pull-down)	5	18	60	µA	3
	IIL1	VIL1=VSS (for pull-up)	-60	-18	-5	µA	
	IIH1S	VIH1=VDD=5V (for pull-down)	70	250	660	µA	
	IIL1S	VIL1=VSS, VDD=5V (for pull-down)	-660	-250	-70	µA	
	IIH1Z	VIH1=VDD (for high impedance)	0	—	1	µA	
	IIL1Z	VIL1=VSS (for high impedance)	-1	—	0	µA	
Input current 2 (IN0, IN1)	IIH2	VIH2=VDD1 (for pull-down)	5	18	60	µA	
	IIH2Z	VIH2=VDD1 (for high impedance)	0	—	1	µA	
	IIL2Z	VIL2=VSS (for high impedance)	-1	—	0	µA	
Input current 3 (OSC1)	IIL3	VIL3=VSS (for pull-up)	-60	-22	-6	µA	
	IIH3Z	VIH3=VDD1 (for high impedance)	0	—	-1	µA	
	IIL3Z	VIL3=VSS (for high impedance)	-1	—	0	µA	
Input current 4 ($\overline{RESET}$, $\overline{TST1}$, $\overline{TST2}$)	IIH4	VIH=VDD1	0	—	1	µA	
	IIL4	VIL4=VSS	-1.5	-0.75	-0.3	mA	
Input voltage 1 (P0.0 ~ P0.3) (P2.0 ~ P2.3) (P3.0 ~ P3.3) (P4.0 ~ P4.3)	VIH1	—	1.2	—	1.5	V	4
	VIL1	—	0	—	0.3	V	
	VIH1S	VDD=5V	4	—	5	V	
	VIL1S	VDD=5V	0	—	1	V	
Input voltage 2 (IN0, IN1, OSC1)	VIH2	—	1.2	—	1.5	V	
	VIL2	—	0	—	0.3	V	
Input voltage 3 ($\overline{RESET}$, $\overline{TST1}$, $\overline{TST2}$)	VIH3	—	1.2	—	1.5	V	
	VIL3	—	0	—	0.3	V	
Hysteresis width (P0.0 ~ P0.3) (P2.0 ~ P2.3) (P3.0 ~ P3.3) (P4.0 ~ P4.3)	ΔVT1	—	0.05	0.1	0.3	V	
	ΔVT1S	VDD=5V	0.25	1.0	1.5	V	
Hysteresis width ($\overline{RESET}$, $\overline{TST1}$, $\overline{TST2}$)	ΔVT2	—	0.05	0.1	0.3	V	
Input pin capacity (P0.0 ~ P0.3) (P2.0 ~ P2.3) (P3.0 ~ P3.3) (P4.0 ~ P4.3)	CIN	—	—	—	5	pF	1

Measurement Circuit 1

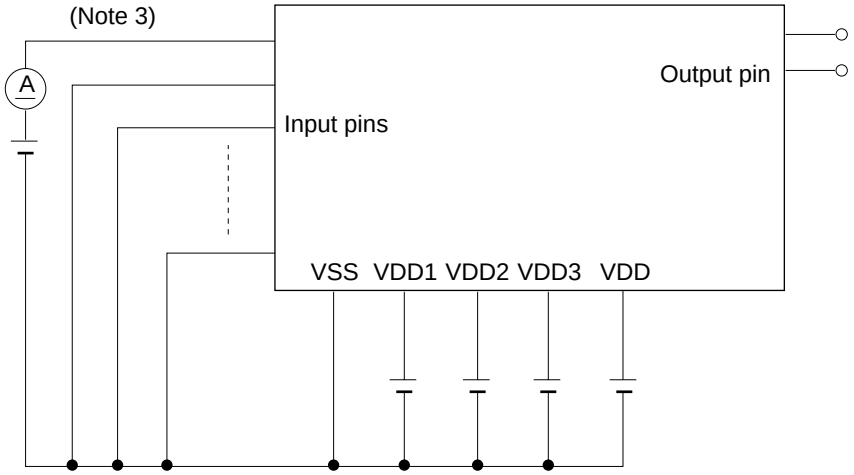


Ca, Cb, C12 : 0.1 μF
ROS : 300 kΩ
X'tal : 32.768 kHz
RT0 : 10 kΩ / 2 kΩ
CS0 : 820 pF
RI0 : 10kΩ

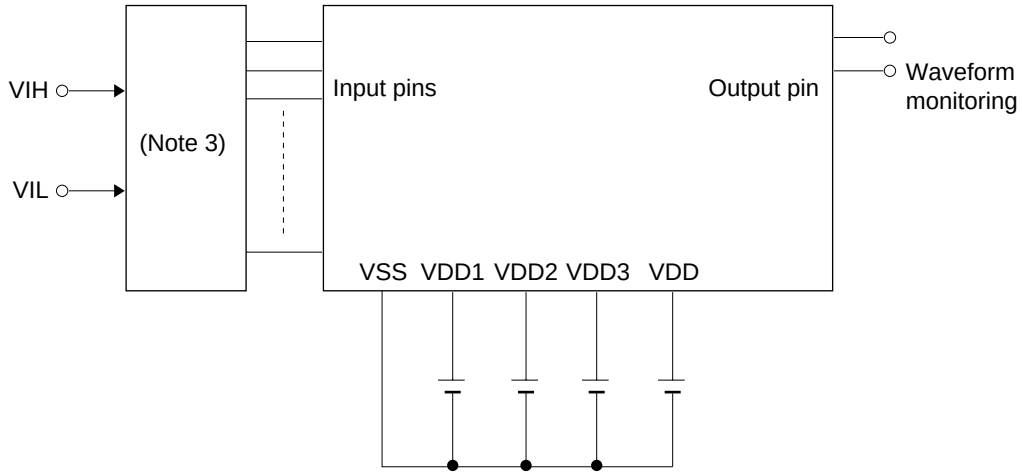
Measurement Circuit 2



Measurement Circuit 3



Measurement Circuit 4



(Note 1) Input logic for specified mode
(Note 2) Repeated on specified output pin
(Note 3) Repeated on specified input pin

- **AD Converter Characteristics**
  (Unless otherwis specified, VSS=0V, VDD1=VDD=1.5V, Ta=0~65˚C)

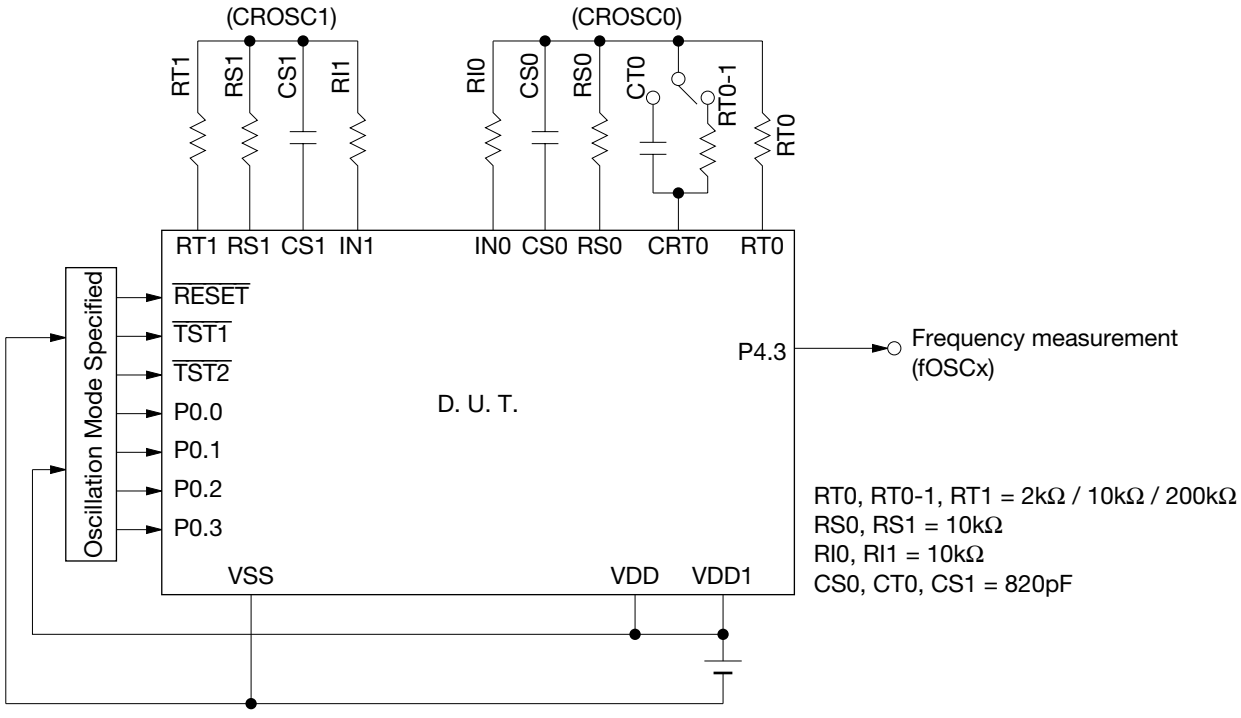
Parameter (Relevant pin name)	Symbol	Condition	Rating			Unit	Measure-ment Circuit
			Min.	Typ.	Max.		
Oscillation resistance	RS0, RS1, RT0, RT0-1, RT1	CS0, CT0, CS1 ≥ 740pF	2	—	—	kΩ	
Input current limiting resistance	RI0, RI1	—	1	10	—	kΩ	
Oscillation frequency	fOSC1	Oscillation resistance = 2kΩ	165	221	256	kHz	5
	fOSC2	Oscillation resistance = 10kΩ	41.8	52.2	60.6	kHz	
	fOSC3	Oscillation resistance = 200kΩ	2.55	3.04	3.53	kHz	
RS•RT oscillation frequency ratio (Note)	Kf1	RT0, RT0-1, RT1 = 2kΩ	3.89	4.18	4.35	—	
	Kf2	RT0, RT0-1, RT1 = 10kΩ	0.990	1	1.010	—	
	Kf3	RT0, RT0-1, RT1 = 200kΩ	0.0561	0.0584	0.0637	—	

(Note) Kfx is the ratio of the oscillation frequency based on the reference resistance and the oscillation frequency based on the sensor resistance in the same condition.

$$Kfx=\frac{fOSCx(RT0 - CS0\ Oscillation)}{fOSCx(RS0 - CS0\ Oscillation)},\ \frac{fOSCx(RT0\text{-}1 - CS0\ Oscillation)}{fOSCx(RS0 - CS0\ Oscillation)},\ \frac{fOSCx(RT1 - CS1\ Oscillation)}{fOSCx(RS1 - CS1\ Oscillation)}$$

(x=1, 2, 3)

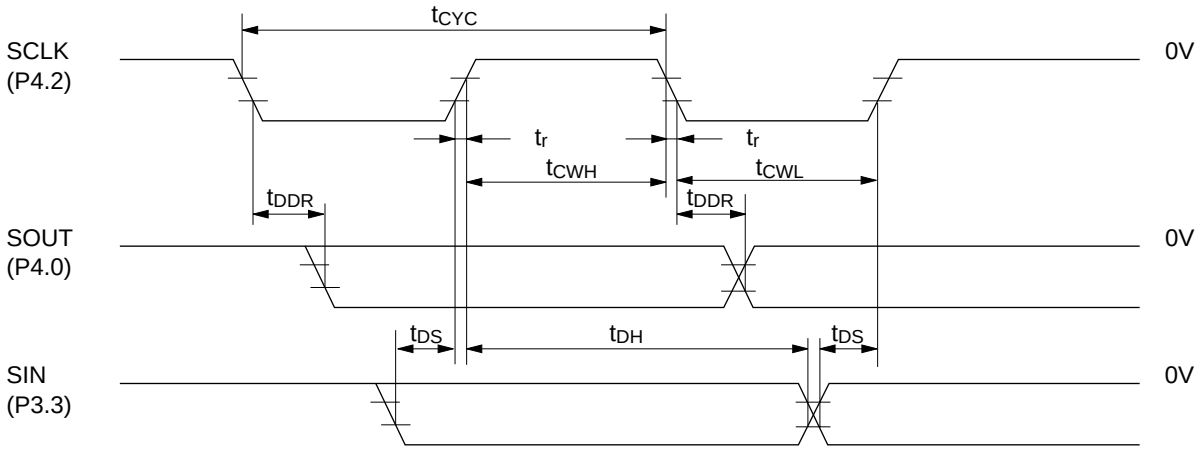
Measurement Circuit 5



- **AC Characteristics**
  (Serial interface, VSS=0V, VDD1=1.5V, VDD=5V, Ta=0~65˚C)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input fall time	tf	—	—	15	50	ns
SCLK input rise time	tr	—	—	15	50	ns
SCLK input "L" level pulse width	tCWL	—	0.8	—	—	µs
SCLK input "H" level pulse width	tCWH	—	0.8	—	—	µs
SCLK input cycle time	tCYC	—	2.0	—	—	µs
SCLK output cycle time	tCYC1(O)	CPU is in the operating mode at 32kHz	—	30.5	—	µs
SCLK output cycle time	tCYC2(O)	CPU is in the operating mode at 400kHz	—	2.5	—	µs
SOUT output delay time	tDDR	CL = 10pF	—	—	0.4	µs
SIN input set-up time	tDS	—	0.5	—	—	µs
SIN input hold time	tDH	—	0.8	—	—	µs

- **AC Characteristics timing**
  ("H" level=4V, "L" level=1V)



(2) For 3.0V specifications in the microcontroller operation mode

- **Absolute Maximum Ratings**

(VSS=0V)

Prameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	VDD1	Ta = 25°C	-0.3 ~ +2.0	V
Power supply voltage 2	VDD2	Ta = 25°C	-0.3 ~ +4.0	V
Power supply voltage 3	VDD3	Ta = 25°C	-0.3 ~ +5.5	V
Power supply voltage 5	VDD	Ta = 25°C	-0.3 ~ +5.5	V
Input voltage 1	VIN1	VDD2 system input, Ta = 25°C	-0.3 ~ VDD2+0.3	V
Input voltage 2	VIN2	VDD system input, Ta = 25°C	-0.3 ~ VDD+0.3	V
Output voltage 1	VOUT1	VDD2 system output, Ta = 25°C	-0.3 ~ VDD2+0.3	V
Output voltage 2	VOUT2	VDD3 system output Ta = 25°C,	-0.3 ~ VDD3+0.3	V
Output voltage 3	VOUT3	VDD system output, Ta = 25°C	-0.3 ~ VDD+0.3	V
Storage temperature	TSTG	—	-55 ~ +125	°C

- **Recommended Operating Conditions**

(VSS=0V)

Prameter	Symbol	Condition	Rating	Unit
Operating temperature	TOPE	—	0 ~ 65	°C
Operating voltage	VDD2	—	2.7 ~ 3.5	V
	VDD	— (Note)	(0.8•VDD2, MIN +2.7) ~ 5.25	V
400kHz OSC external resistance	ROS	—	90 ~ 500	kΩ
X'tal OSC oscillation frequency	fXT	—	30 ~ 66	kHz

(Note) The lower limit of VDD indicates to be 80% of VDD2 and minimum 2.7V.

- **DC Characteristics**
  (Unless otherwis specified, VSS=0V, VDD2=VDD=3.0V, Ta=0~65˚C)

(1/3)

Parameter (Relevant pin name)	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measure-ment Circuit
VDD1 voltage	VDD1	Ca, Cb, C12=0.1µF +100% -50%		1.3	1.5	1.7	V	
VDD3 voltage	VDD3	Ca, Cb, C12=0.1µF +100% -50%		4.3	4.5	4.7	V	
XTOSC oscillation beginning voltage	VSTA	Within 5 seconds from the beginning of an oscillation		2.7	—	—	V	
XTOSC oscillation maintaining voltage	VHOLD	—		2.7	—	—	V	
XTOSC stop detecting time	VSTOP	—		0.1	—	1000	ms	
XTOSC internal capacity	CG	—		10	15	20	pF	
XTOSC external capacity	CGEX	When CG is an external option.		10	—	30	pF	
XTOSC internal capacity	CD	—		10	15	20	pF	
400kOSC internal capacity	COS	—		8	12	16	pF	
400kOSC oscillation frequency	fOSC	External resistance ROS=100kΩ VDD2=2.0 ~ 3.5V		300	400	620	kHz	1
POR generating voltage	VPOR1	POR is generated when VDD2 varies from VPROR1 to 3.0V.		0	—	0.7	V	
POR non-generating voltage	VPOR2	POR is not generated when VDD2 varies from VPROR2 to 3.0V.		2	—	3	V	
Current consumption 1	IDD1	CPU is in the HALT mode (400kOSC stop)		—	2.0	5.0	µA	
Current consumption 2	IDD2	CPU is in the operating mode (400kOSC stop)		—	20	50	µA	
Current consumption 3	IDD3	CPU is in the operating mode (400kOSC operation)		—	220	450	µA	
Current consumption 4	IDD4	fSCK=300kHz in the serial transfer CPU is in the operating mode. (400kOSC stop)		—	20	50	µA	
Current consumption 5	IDD5	CR oscillator for an A/D converter opeartes. CPU is in the HALT mode. (400kOSC stop)	RT0=10kΩ	—	300	450	µF	
			RT0=2kΩ	—	1300	2000	µA	

(Note)
- "XTOSC" indicates an oscillation circuit at 32.768kHz.
- "400kOSC" indicates a 400kHz CR oscillation circuit.
- "POR" indicates a power-on reset.
- "TSTOP" indicates to generate a system reset when XTOSC stops oscillation during more than the time of TSTOP.

- **DC Characteristics**
  (Unless otherwis specified, VSS=0V, VDD1=1.5V, VDD2=VDD=3.0V, VDD3=4.5V, Ta=0~65˚C)

(2/3)

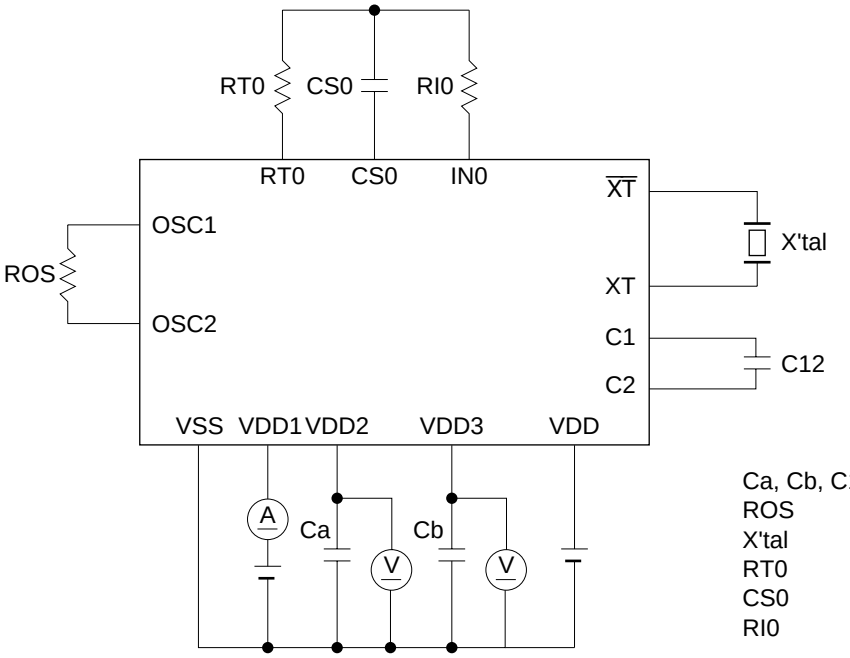
Parameter (Relevant pin name)	Symbol	Condition	Rating			Unit	Measure-ment Circuit
			Min.	Typ.	Max.		
Output current 1 (P1.0)	IOH1	VOH1=VDD-0.5V	-6	-2	-0.7	mA	2
	IOL1	VOL1=0.5V	3	8	25	mA	
	IOL1S	VDD=5V, VOL1=0.5V	4	12	36	mA	
Output current 2 (P1.1 ~ P1.3) (P2.0 ~ P2.3) (P3.0 ~ P3.3) (P4.0 ~ P4.3)	IOH2	VOL2=VDD-0.5V	-6	-2	-0.7	mA	
	IOL2	VOL2=0.5V	0.7	2	6	mA	
	IOL2S	VDD=5V, VOL2=0.5V	1	3	9	mA	
Output current 3 (BD)	IOH3	VOH3=VDD2-0.7V	-6	-2	-0.7	mA	
	IOL3	VOL3=0.7V	0.7	2	6	mA	
Output current 4 (RT0, RT1, RS0, RS1, CRT0, CS0, CS1)	IOH4	VOH4=VDD2-0.1V	-2.5	-1.3	-0.7	mA	
	IOL4	VOL4=0.1V	0.7	1.3	2.5	mA	
Output current 5 (When the pins L26 to L33 are set to output ports.)	IOH5	VOL5=VDD-0.5V	-1.5	-0.6	-0.15	mA	
	IOL5	VOL5=0.5V	0.15	0.6	1.5	mA	
	IOL5S	VDD=5V, VOL5S=0.5V	0.2	0.7	2.0	mA	
Output current 6 (OSC2)	IOH6	VOH6=VDD2-0.5V	-6	-2	-0.7	mA	
	IOL6	VOL6=0.5V	0.7	2	6	mA	
Output current 7 (L0 ~ L33)	IOH7	VOH7=VDD3-0.2V (VDD3 level)	—	—	-4	µA	—
	IOMH7	VOMH7=VDD2+0.2V (VDD2 level)	4	—	—	µA	
	IOMH7S	VOMH7S=VDD2-0.2V (VDD2 level)	—	—	-4	µA	
	IOML7	VOML7=VDD1+0.2V (VDD1 level)	4	—	—	µA	
	IOML7S	VOML7S=VDD1-0.2V (VDD1 level)	—	—	-4	µA	
	IOL7	VOL7=0.2V (VSS level)	4	—	—	µA	
Output leak (P1.0 ~ P1.3) (P2.0 ~ P2.3) (P3.0 ~ P3.3) (P4.0 ~ P4.3) (RT0, RT1, RS0, RS1, CRT0, CS0, CS1)	IOOH	VOH=VDD2	—	—	0.3	µA	
	IOOL	VOL=VSS	-0.3	—	—	µA	

- **DC Characteristics**
  (Unless otherwis specified, VSS=0V, VDD1=1.5V, VDD2=VDD=3.0V, VDD3=4.5V, Ta=0~65˚C)

(3/3)

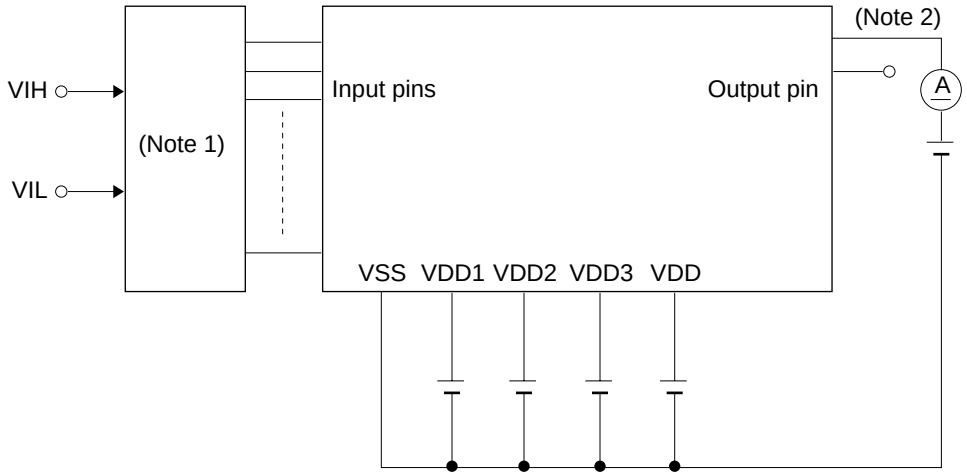
Parameter (Relevant pin name)	Symbol	Condition	Rating			Unit	Measure-ment Circuit
			Min.	Typ.	Max.		
Input current 1 (P0.0 ~ P0.3) (P2.0 ~ P2.3) (P3.0 ~ P3.3) (P4.0 ~ P4.3)	IIH1	VIH1=VDD (for pull-down)	30	90	300	µA	
	IIL1	VIL1=VSS (for pull-up)	-300	-90	-30	µA	
	IIH1S	VIH1=VDD=5V (for pull-down)	80	250	800	µA	
	IIL1S	VIL1=VSS, VDD=5V (for pull-down)	-800	-250	-80	µA	
	IIH1Z	VIH1=VDD (for high impedance)	0	—	1	µA	
	IIL1Z	VIL1=VSS (for high impedance)	-1	—	0	µA	
Input current 2 (IN0, IN1)	IIH2	VIH2=VDD2 (for pull-down)	30	90	300	µA	
	IIH2Z	VIH2=VDD2 (for high impedance)	0	—	1	µA	3
	IIL2Z	VIL2=VSS (for high impedance)	-1	—	0	µA	
Input current 3 (OSC1)	IIL3	VIL3=VSS (for pull-up)	-300	-110	-10	µA	
	IIH3Z	VIH3=VDD2 (for high impedance)	0	—	1	µA	
	IIL3Z	VIL3=VSS (for high impedance)	-1	—	0	µA	
Input current 4 ($\overline{\text{RESET}}$, $\overline{\text{TST1}}$, $\overline{\text{TST2}}$)	IIH4	VIH4=VDD2	0	—	1	µA	
	IIL4	VIL4=VSS	-3	-1.5	-0.75	mA	
Input voltage 1 (P0.0 ~ P0.3) (P2.0 ~ P2.3) (P3.0 ~ P3.3) (P4.0 ~ P4.3)	VIH1	—	2.4	—	3	V	
	VIL1	—	0	—	0.6	V	
	VIH1S	VDD=5V	4	—	5	V	
	VIL1S	VDD=5V	0	—	1	V	
Input voltage 2 (IN0, IN1, OSC1)	VIH2	—	2.4	—	3	V	4
	VIL2	—	0	—	0.6	V	
Input voltage 3 ($\overline{\text{RESET}}$, $\overline{\text{TST1}}$, $\overline{\text{TST2}}$)	VIH3	—	2.4	—	3	V	
	VIL3	—	0	—	0.6	V	
Hysteresis width (P0.0 ~ P0.3) (P2.0 ~ P2.3) (P3.0 ~ P3.3) (P4.0 ~ P4.3)	△VT1	—	0.2	0.5	1	V	
	△VT1S	VDD=5V	0.25	1.0	1.5	V	
Hysteresis width ($\overline{\text{RESET}}$, $\overline{\text{TST1}}$, $\overline{\text{TST2}}$)	△VT2	—	0.2	0.5	1	V	
Input pin capacity (P0.0 ~ P0.3) (P2.0 ~ P2.3) (P3.0 ~ P3.3) (P4.0 ~ P4.3)	CIN	—	—	—	5	pF	1

Measurement Circuit 1

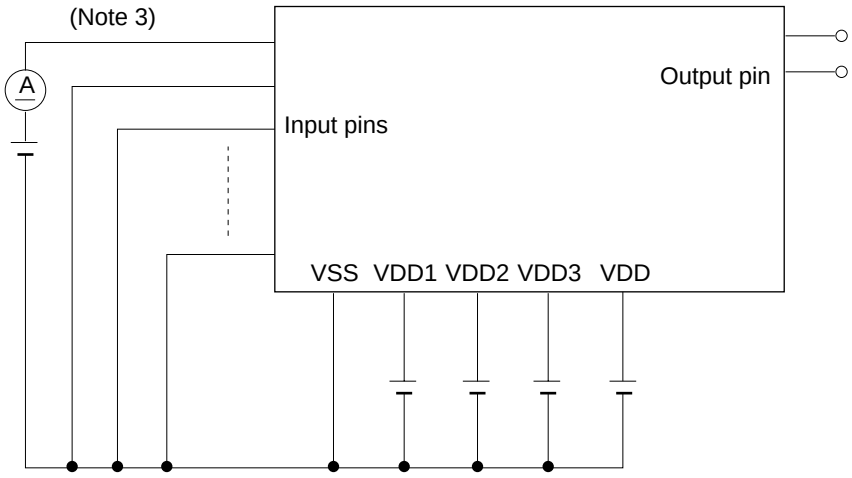


Ca, Cb, C12 : 0.1 µF
ROS : 100 kΩ
X'tal : 32.768 kHz
RT0 : 10 kΩ / 2 kΩ
CS0 : 820 pF
RI0 : 10kΩ

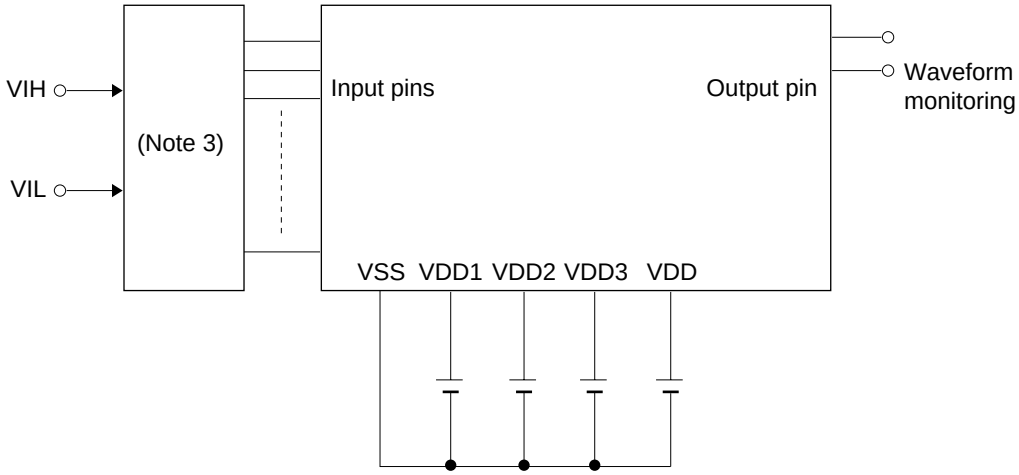
Measurement Circuit 2



Measurement Circuit 3



Measurement Circuit 4



(Note 1) Input logic for specified mode
(Note 2) Repeated on specified output pin
(Note 3) Repeated on specified input pin

- **AD Converter Characteristics**
  (Unless otherwis specified, VSS=0V, VDD2=VDD=3V, Ta=0~65˚C)

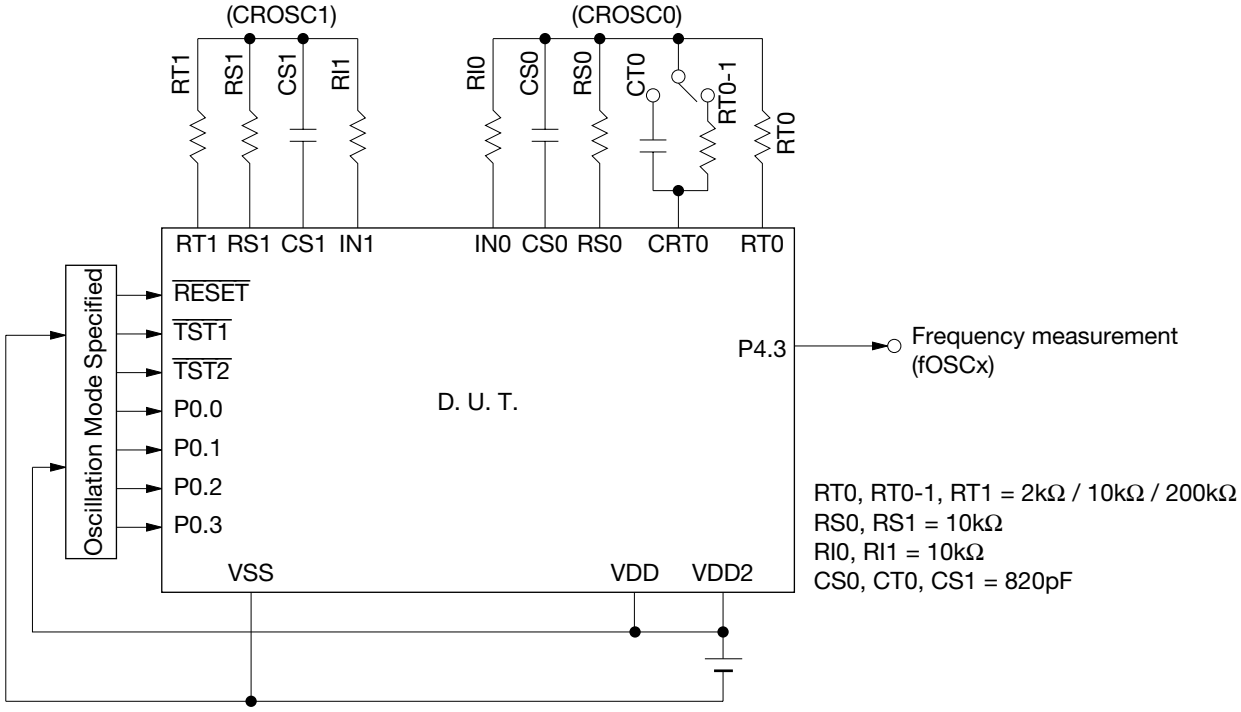
Parameter (Relevant pin name)	Symbol	Condition	Rating			Unit	Measure-ment Circuit
			Min.	Typ.	Max.		
Oscillation resistance	RS0, RS1, RT0, RT0-1, RT1	CS0, CT0, CS1 ≥ 740pF	1	—	—	kΩ	
Input current limiting resistance	RI0, RI1	—	1	10	—	kΩ	
Oscilation frequency	fOSC1	Oscillation resistance = 2kΩ	200	239	277	kHz	5
	fOSC2	Oscillation resistance = 10kΩ	46.5	55.4	64.3	kHz	
	fOSC3	Oscillation resistance = 200kΩ	2.79	3.32	3.85	kHz	
RS•RT oscillation frequency ratio (Note)	Kf1	RT0, RT0-1, RT1 = 2kΩ	4.115	4.22	4.326	—	
	Kf2	RT0, RT0-1, RT1 = 10kΩ	0.990	1	1.010	—	
	Kf3	RT0, RT0-1, RT1 = 200kΩ	0.0573	0.0616	0.0659	—	

(Note) Kfx is the ratio of the oscillation frequency based on the reference resistance and the oscillation frequency based on the sensor resistance in the same condition.

$$Kfx=\frac{fOSCx(RT0 - CS0\ Oscillation)}{fOSCx(RS0 - CS0\ Oscillation)},\ \frac{fOSCx(RT0\text{-}1 - CS0\ Oscillation)}{fOSCx(RS0 - CS0\ Oscillation)},\ \frac{fOSCx(RT1 - CS1\ Oscillation)}{fOSCx(RS1 - CS1\ Oscillation)}$$

(x=1, 2, 3)

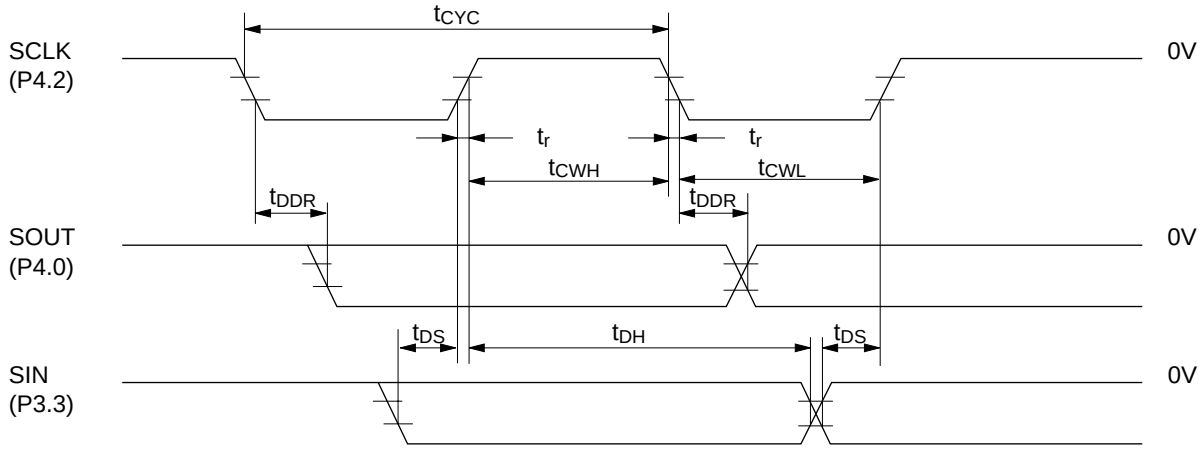
Measurement Circuit 5



- **AC Characteristics**
  (Serial interface, VSS=0V, VDD2=3V, VDD=5V, Ta=0~65˚C)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input fall time	tf	—	—	15	50	ns
SCLK input rise time	tr	—	—	15	50	ns
SCLK input "L" level pulse width	tCWL	—	0.8	—	—	µs
SCLK input "H" level pulse width	tCWH	—	0.8	—	—	µs
SCLK input cycle time	tCYC	—	2.0	—	—	µs
SCLK output cycle time	tCYC1(O)	CPU is in the operating mode at 32kHz	—	30.5	—	µs
SCLK output cycle time	tCYC2(O)	CPU is in the operating mode at 400kHz	—	2.5	—	µs
SOUT output delay time	tDDR	CL = 10pF	—	—	0.4	µs
SIN input set-up time	tDS	—	0.5	—	—	µs
SIN input hold time	tDH	—	0.8	—	—	µs

- **AC Characteristics timing**
  ("H" level=4V, "L" level=1V)



(3) PROM Mode (Common specifications for 1.5V and 3.0V)

- **Absolute Maximum Ratings**

(VSS=0V)

Prameter	Symbol	Condition	Rating	Unit
PROM power supply voltage	VCC	VCC=VDD1=VDD2, Ta = 25°C	-0.3 ~ +6.7	V
Program voltage	VPP	Ta = 25°C	-0.3 ~ +14.0	V
PROM input voltage	VI	VCC system input, Ta = 25°C	-0.3 ~ VCC+0.3	V
PROM output voltage	VO	VCC system output, Ta = 25°C	-0.3 ~ VCC+0.3	V
Storage temperature	TSTG	—	-55 ~ +125	°C

- **Recommended Operating Conditions**

(VSS=0V)

Prameter	Symbol	Condition	Rating	Unit
Operating temperature	TOPEP	—	0 ~ 65	°C
VCC power supply voltage	VCC	VCC=VDD1=VDD2	4.75 ~ 5.25	V
VPP power supply voltage	VPP	In read	4.75 ~ 5.25	V
		In write	12.0 ~ 13.0	V
Input voltage	VIH	VCC=VDD1=VDD2	4 ~ VCC	V
	VIL	—	0 ~ 1	V

< Read Operation >

- **DC Characteristics**
  (Unless otherwise specified, VDD1=VDD2=VPP=5V±5%, Ta=25˚C±5°C)

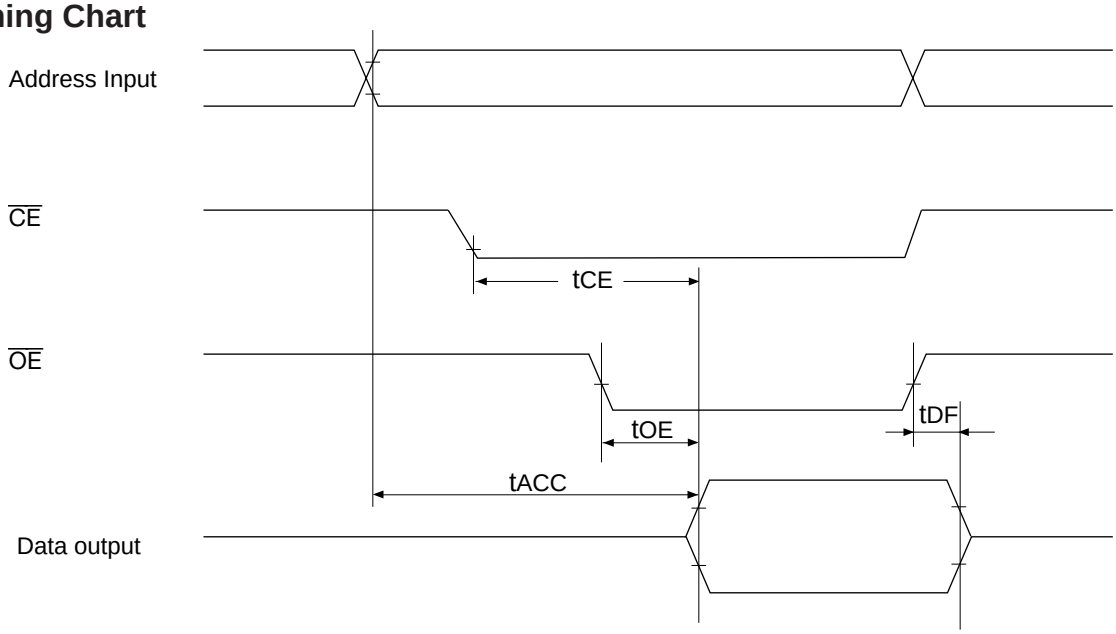
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
VCC power supply current (standby)	ICC1	VCC=VDD1=VDD2 $\overline{CE}$=VIH	—	—	35	mA
VCC power supply current (operation)	ICC2	VCC=VDD1=VDD2 $\overline{CE}$=VIL	—	—	100	mA
Input voltage	VIH	VCC=VDD1=VDD2	4	—	VCC	V
	VIL	—	0	—	1	V
Output current	IOH	VCC=VDD1=VDD2 VOH=VCC-0.5V	-2	-0.7	-0.2	mA
	IOL	VOL=0.5V	0.2	0.7	2	mA

- **AC Characteristics**
  (Unless otherwise specified, VCC=5V±5%, VPP=VCC, Ta=0˚C~70°C)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Address aaccess time	tACC	$\overline{OE}$=$\overline{CE}$=VIL	—	—	120	ns
$\overline{CE}$ access time	tCE	$\overline{OE}$=VIL	—	—	120	ns
$\overline{OE}$ access time	tOE	$\overline{CE}$=VIL	—	—	50	ns
Output disable time	tDF	$\overline{CE}$=VIL	0	—	40	ns

Measurement conditions: Input pulse level ..... 0.45V~4.55V
Input rise / fall time 5ns
Threshold level ..... Input 0.8V, 2V / output 0.8V, 2V

- **Timing Chart**



< Write Operation >

- **DC Characteristics**
  (Unless otherwise specified, VSS=0V, VDD1=VDD2=5V±5%, VPP=12.5V±0.5V, Ta=25˚C±5°C)

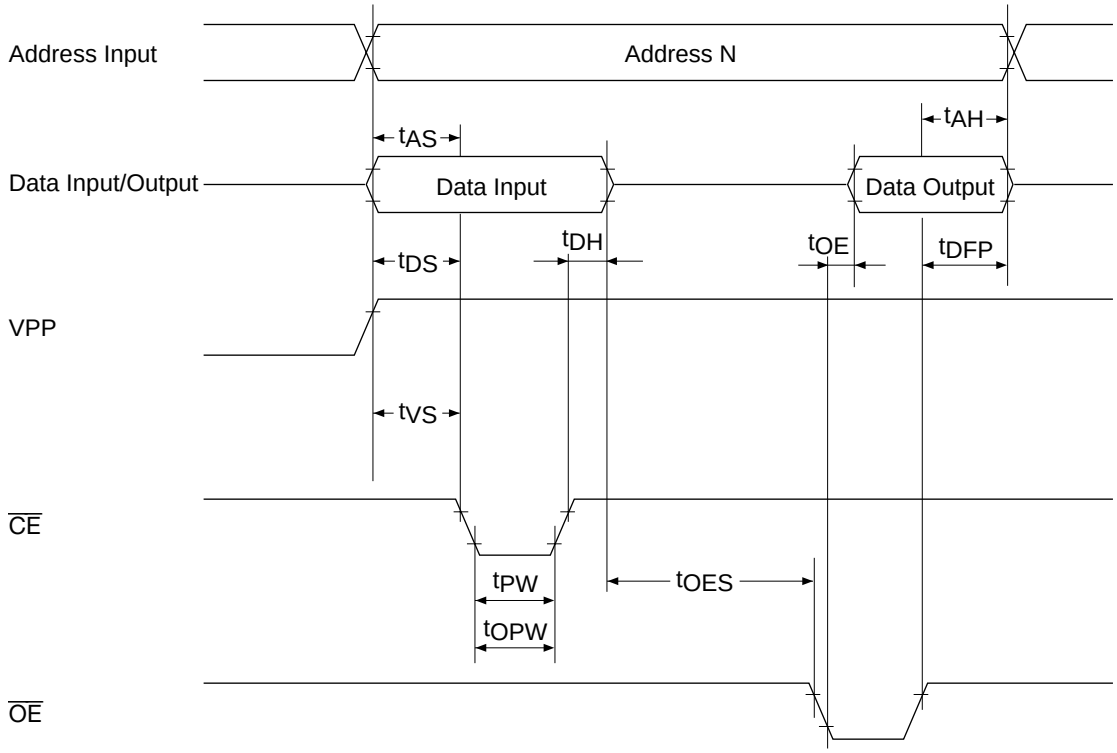
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
VPP power supply current	IPP	$\overline{CE}$=VIL	—	—	50	mA
VCC power supply current	ICC	VCC=VDD1=VDD2	—	—	100	mA
Input voltage	VIH	VCC=VDD1=VDD2	4	—	VCC	V
	VIL	—	0	—	1	V
Output current	IOH	VCC=VDD1=VDD2 VOH=VCC-0.5V	-2	-0.7	-0.2	mA
	IOL	VOL=0.5V	0.2	0.7	2	mA

- **AC Characteristics**
  (Unless otherwise specified, VSS=0V, VDD1=VDD2=5V±5%, VPP=12.5V±0.5V, Ta=25˚C±5°C)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Address set-up time	tAS	—	2	—	—	µs
$\overline{OE}$ set-up time	tOES	—	2	—	—	µs
Data set-up time	tDS	—	2	—	—	µs
Address hold time	tAH	—	0	—	—	µs
Data hold time	tDH	—	2	—	—	µs
$\overline{OE}$ output floating delay time	tDEP	—	0	—	130	ns
VPP power supply set-up time	tVS	—	2	—	—	µs
Initial program pulse width	tPW	VDD1=VDD2 6V±0.25V	0.95	1.0	1.05	ms
Additional program pulse width	tOPW	VDD1=VDD2 6V±0.25V	2.85	—	78.75	ms
$\overline{OE}$ output effective delay time	tOE	—	—	—	150	ns

Measurement conditions: Input pulse level ..... 0.45V~4.55V
Input rise / fall time ..... Less than 20ns
Threshold level ..... Input 0.8V, 2V / output 0.8V, 2V

- **Program Timing Chart**



MSM64P164

User's Manual

First Edition: October 1993