DATA SHEET

OKI

MSM6307

D2B TRANSCEIVER LSI

FIRST EDITION

ISSUE DATE: JUN., 1993

Contents

Introduction to D2B

The D2B (Domestic Digital Bus) concept was designed by ***Philips*** *to provide the world-wide industry with a communication performance for various environments, such as audio/video, automotive, data processing and industrial. For every field, D2B provides the suitable modes, which determine the transfer speed and amount of data for each frame transmitted or received. Any system coring a MCU and a D2B user interface is enabled to communicate with another equally designed system originating or being addressed (master to slave transceptions and vice-versa) using standard D2B protocols.*

D2B should be of special interest to the manufacturers of home entertainment electronics who are given an unique platform to realize individual home bus integrations with interactive communication capabilities on control level.

System compatibility is given thanks to the rigorous standardization of command structures. In other words, every AV set which is equipped with a D2B interface can be linked with others equally equipped from different manufacturers and still communicate accurately. Yet the manufacturer maintains his individual brand identity as only the mandatory commands are involved with the standardization, not the user interface.

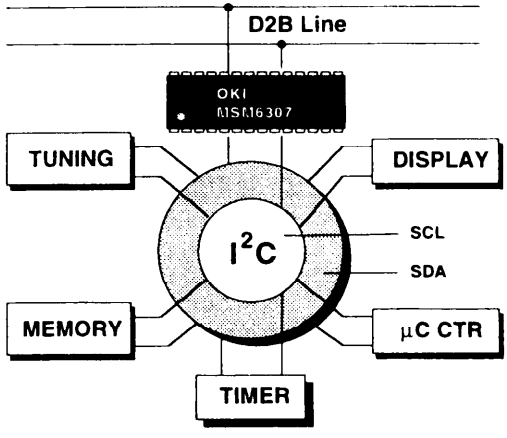
D2B features allow the user to extend a bus network up to 150 meters length realized with a balanced cable pair to which up to 50 apparatus' can be connected without requiring driver circuits or other peripheral aid. The exchange of commands and data sequences among different AV sets allow to execute complex functions required for a desired performance upon pressing a single button, for instance, on a remote control unit. Consequently, a TV program can be recorded on a VTR without pressing individual buttons on each set involved with this process. Other convenient functions may be included in this operation, such as monitoring with PIP (picture in picture) while watching a different program. During the same process not needed sets can be disengaged for maximum energy economy.

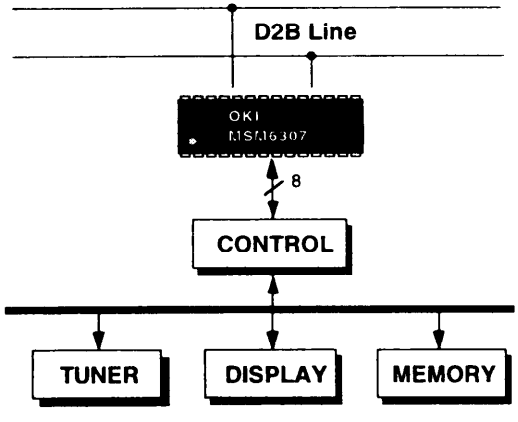
Other opportunities include the shifting of preset stations from one system to another, the automatic alignment of antennas, home bus control through the telephone line, and many more useful and convenient functions. What is more, the user manuals for a given AV configuration can be simplified and yet the consumer enjoys all functions he paid money for.

Introduction to D2B

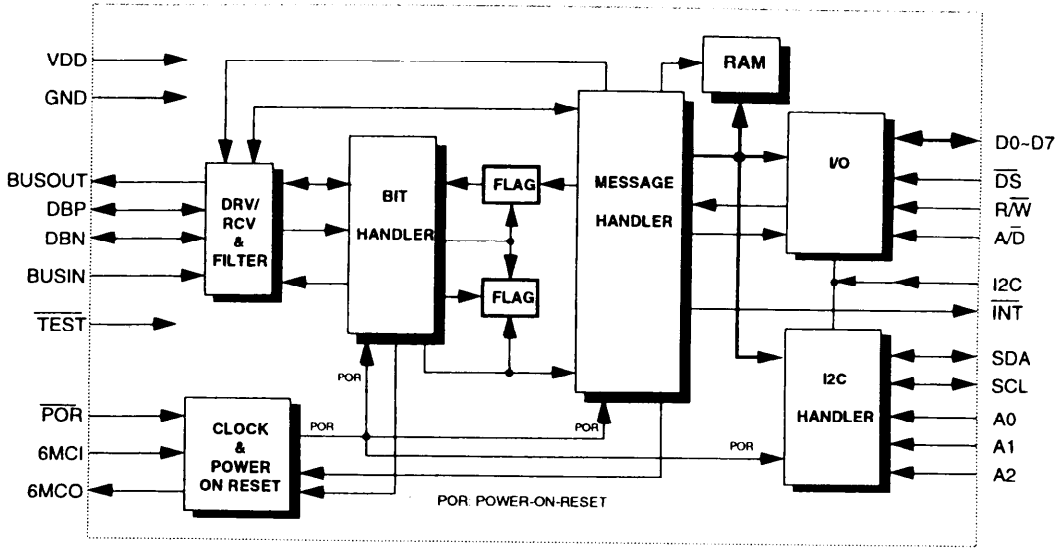
OKI Electric's MSM6307 interfaces between conventional bus systems and D2B including buffering of data and interrupt after each transmission and reception. Transceived are D2B frames which contain in fixed sequences addresses, control bits and data, as well as parity bits, acknowledge bits and an end bit.

MSM6307 operates under MCU control while the program ROM, on-chip or off-chip, contains the D2B software driver in addition to the system control program. The MCU serves the hardware interfaces of the MSM6307, 8-bit parallel or I2C, and sends control bytes and data into the D2B chip registers and buffers to be send out over the D2B bus to other D2B units. A receiving D2B equipped unit writes the bytes into the buffer of its D2B chip and can be read out by its controlling MCU after the interrupt signalled by that D2B chip. The MCU then interpretates the data in order to execute the desired sequence of functions. Numerous on-chip control and information registers allow complex function controls, which can be realized by convenient controller programming.

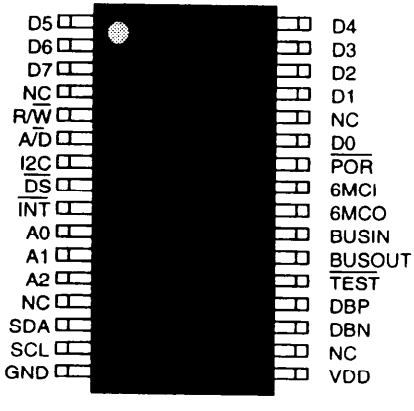




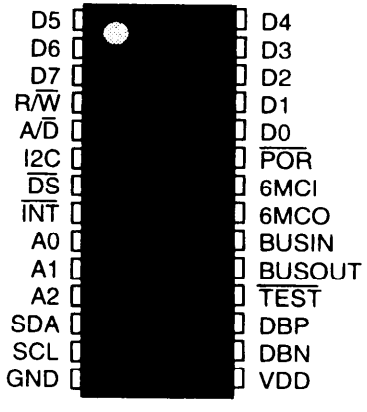
Block Diagram
Pin Assignment



32-PIN SMALL OUTLINE
(top view)



28-PIN DUAL IN-LINE
(top view)

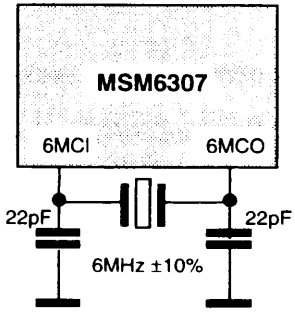


Pin Description

SYMBOL	DIP	SOP	I/O	DESCRIPTION
VDD	15	17	I	Power supply input, nominally +5 Volts.
GND	14	16	I	Ground terminal, nominally 0 Volts.
$\overline{POR}$	23	26	I	Reset input which requires a capacitor to ground to perform power-on reset function. A "L" level resets the chip, a "H" level releases the reset.
6MCI	22	25	I	Oscillation clock input, rating 6 MHz, typically.
6MCO	21	24	O	Oscillation clock output.
$\overline{DS}$	7	8	I	Data strobe for the parallel interface. Upon a "L" level addresses or data are valid for read and write.
R/$\overline{W}$	4	5	I	During active $\overline{DS}$, the level on this pin selects data read or write operation from and to the parallel interface of the LSI. "H" = read, "L" = write.
A/$\overline{D}$	5	6	I	Selects whether adresses or data are to be transported on the parallel bus. "H" = address, "L" = data.
SDA	12	14	IO	Data I/O line of the I^2C interface, open drain output.
SCL	13	15	IO	Clock line of the I^2C interface, open drain output.
A0~A2	9~11	10~12	I	These inputs set the3 LSBs of the I^2C slave address, programming the I^2C address out of 8 allowed I^2C slave addresses
$\overline{I2C}$	6	7	I	Selects the hardware interfaces. "H" = I^2C, "L" = 8-bit parallel Make sure that SDA, SCL, A0, A1, A2 are grounded in the parallel mode. In the I^2C mode, A/D is grounded while R/$\overline{W}$ and $\overline{DS}$ are connected to VDD.
INT	8	9	O	After each time slot this output sends an interrupt signal in both I^2C and parallel interface selections.
BUSIN	20	23	I	This is the TTL level D2B input. If the internal D2B driver is used, this input must be connected to VDD.
BUSOUT	19	22	O	This is the TTL level D2B output. If the internal D2B driver is used, this input must be left open.

Pin Description, cont'd

SYMBOL	DIP	SOP	I/O	DESCRIPTION
DBN/DBP	16/17	19/20	IO	These are the differential D2B lines and lead to the internal driver/receiver section to the one direction and to further D2B bus units to the other. In case of using the TTL inputs BUSIN & BUSOUT, DBN and DBP must be bridged.
D0~D7			IO	Bi-directional 8-bit data bus.
TEST	18	21	I	This is an input for factory testing and may be wired to VDD or left open in applications.



NOTE: Capacitor values may change in accordance with X-TAL characteristics.

Operating Ranges

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{DD}	Power supply voltage	T_a = 25°C	-0.3 ~ 7.0	V
V_I	Input voltage range	T_a = 25°C	-0.3~V_{DD}+0.3V	V
V_O	Output voltage range	T_a = 25°C	-0.3~V_{DD}+0.3V	V
T_{stg}	Storage temperature	-	-55 ~ 150	°C
I_O	Maximum output current	T_a = 25°C	10	mA
P_D	Maximum power loss	T_a = 25°C	700	mW

NOTE: Ratings stressed over above values may cause device malfunction or permanent damage!

Recommended Operating Range

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{DD}	Power supply voltage	-	+4.75 ~ +5.25	V
T_a	Ambient temperature	-	-40 to +85°C	°C
f_{OSC}	Oscillation frequency	-	6 ±10%	MHz
f_{DUTY}	Duty cycle	-	50 ±8%	%

DC Parameters

DC Characteristics

(Ta = -40 to +85°C, V_{DD} = +5V ±10%)

SYMBOL	PARAMETER	PIN REF	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage	A,B	-	2.2	-	-	V
V_{IL}	Input low voltage	A,B	-	-	-	0.8	V
V_{IH}	Input high voltage	C,D,E	-	3.5	-	-	V
V_{IL}	Input low voltage	C,D,E	-	-	-	1.5	V
V_{IHL}	Input leak current	A,B,C,E	$0<V_{IN}<V_{DD}$	-1	-	1	µA
V_{OH}	Output high voltage	F	I_O= -40µA	2.4	-	-	V
V_{OL}	Output low voltage	F	I_O= 1.6mA	-	-	0.4	V
V_{OH}	Output high voltage	A	I_O= -400µA	2.4	-	-	V
V_{OL}	Output low voltage	A	I_O= 2mA	-	-	0.4	V
V_{OL}	Output low voltage	C	I_O= 3mA	-	-	0.4	V
I_{IHL}	Input leak current	D	$V_{IN} < V_{DD}$	-	-	1	µA
I_{IL}	Input low current	D	V_{IN}= 0V	-	-	-0.2	mA
I_{DD}	Active supply current	-	f_{OSC}= 6MHz	-	9	20	mA

PIN REFERENCES:

A: D0 ~ D7
B: $\overline{DS}$, A/$\overline{D}$, R/$\overline{W}$, BUSIN
C: SCL, SDA
D: $\overline{POR}$, $\overline{TEST}$
E: I2C, A0, A1, A2
F: BUSOUT, $\overline{INT}$

DC Characteristics of the D2B Interface

(Ta = -40 to +85°C, V_{DD} = +5V ±10%)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{Ion}	ON-Voltage input [V_{DBP}-V_{DBN}]	120	-	-	mV
V_{Ioff}	OFF-Voltage input [V_{DBP}-V_{DBN}]	-	-	20	mV
V_{Ihy}	Differential hysteresis input [V_{DBP}-V_{DBN}]	20	-	-	mV
V_{cdm}	Common mode input voltage	1	-	3.75	V
R_{in}	Differential input resistance	100	-	-	kΩ
V_{out}	Differential bus output voltage [V_{DBP}-V_{DBN}] *1	150	-	300	mV
V_{coff}	Driver OFF voltage V_{DBP}, V_{DBN}	0.45xVDD	-	0.55xVDD	V
V_{con}	Driver ON-voltage V_{DBP}, V_{DBN} *2	0.45xVDD	-	0.55xVDD	V

*1 Load resistance 60Ω, driver ON
*2 DBP, DBN short circuited

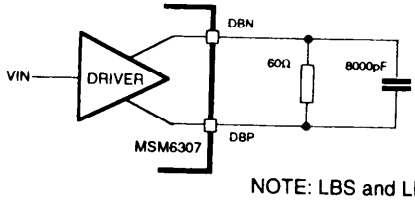
D2B Bus Timing

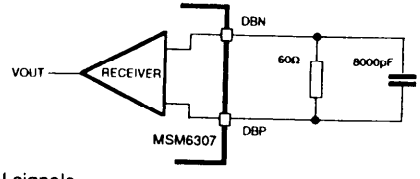
D2B Bus Timing

(Ta = -40 to +85°C, V_{DD} = +5V ±10%)

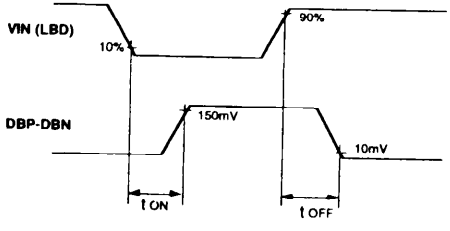
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{DN}	Driver ON delay with test load.	-	-	1.6	µs
t_{OFF}	Driver OFF delay with test load	-	-	1.6	µs
t_{DET}	Detector delay	-	-	750	ns

Can be measured on BUSIN & BUSOUT in the test mode.

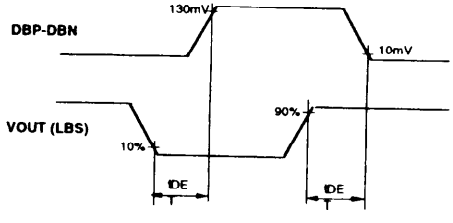




NOTE: LBS and LBD are internal signals.



LINE DRIVER PROPAGATION DELAY



DETECTOR PROPAGATION DELAY

I²C Interface

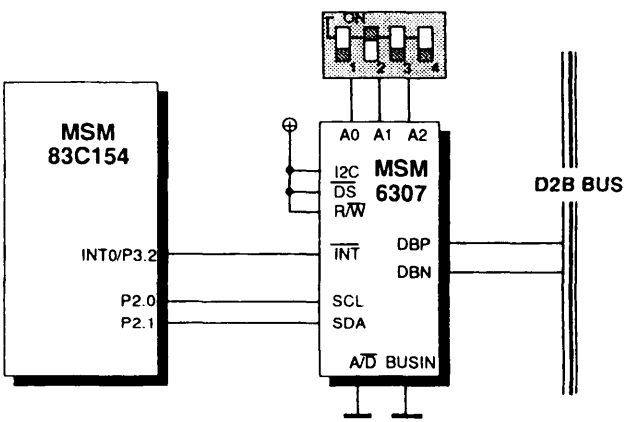
In an I²C environment the MSM6307 works as an I²C slave peripheral only. Both SDA and SDL are bi-directional lines connected to a positive supply voltage via a pull-up resistor. When the bus is free both lines exhibit "H" level. Outputs of devices connected to this bus must provide open drain or open collector to perform the wired-AND function.

Data on the SDA must be stable during the high period of the clock, SCL. The "H" or "L" state on the data line can only change when the clock on SCL is "L".

While the signal on SCL is "H", a start condition is given at the instant of a "H" to "L" transition on the SDA line. The reverse transition from "L" to "H" defines the stop condition. Start and stop conditions are generated by the master (MCU), exclusively, so is the obligatory acknowledge bit after 8 data bits. The transmitting device releases the SDA line with a "H" level for the duration of the acknowledge pulse from the receiver. The 9th. bit on SCL is the clock pulse for the acknowledgement.

After valid start condition the bus is considered busy and released again a certain time after the stop condition applies.

Simplified Circuit with 8-bit Controller

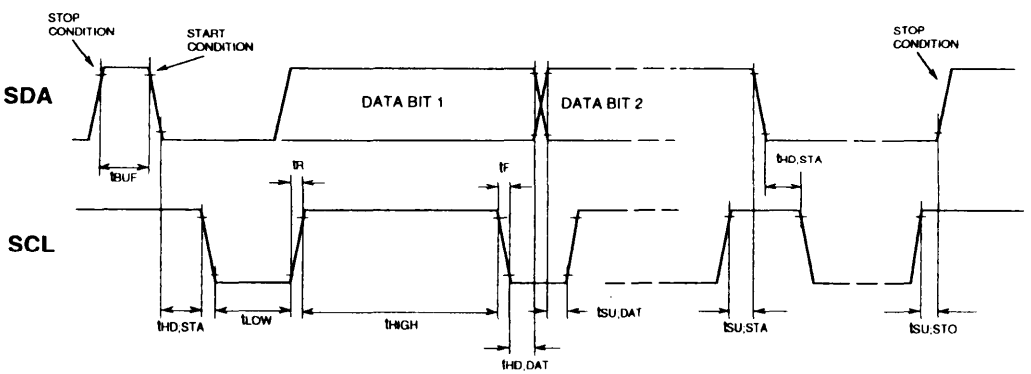


I²C Interface, cont'd

I²C Interface Timing (fast mode)

(Ta = -40 to +85°C, V_{DD} = +5V ±10%)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	0	-	100	kHz
t_{BUF}	Bus free time before transmission start.	4.7	-	-	µs
$t_{HD;STA}$	Hold time at start condition after which 1st clock.	4.0	-	-	µs
t_{LOW}	Clock low period	4.7	-	-	µs
t_{HIGH}	Clock high period	4.0	-	-	µs
$t_{HD;DAT}$	Data hold time	5.0	-	-	µs
$t_{SU;DAT}$	Data set-up time	250	-	-	ns
$t_{SU;STA}$	Set-up time for start condition	4.7	-	-	µs
$t_{SU;STO}$	Set-up time for stop condition	4.7	-	-	µs
t_R	SDA and SCL rise time	-	-	1	µs
t_F	SDA and SCL fall time	-	-	300	ns



I²C Message Format

Slave Address Format

The I²C slave address is a 7 bit address, the 4 MSBs are fixed, the three LSBs are programmable. The desired I²C slave address of the IC is set with the inputs pins A2, A1 and A0. The MSM6307 does not support general calls on I²C.

B6	B5	B4	B3	B2	B1	B0
0	1	0	0	A2	A1	A0

Slave Receiver Format

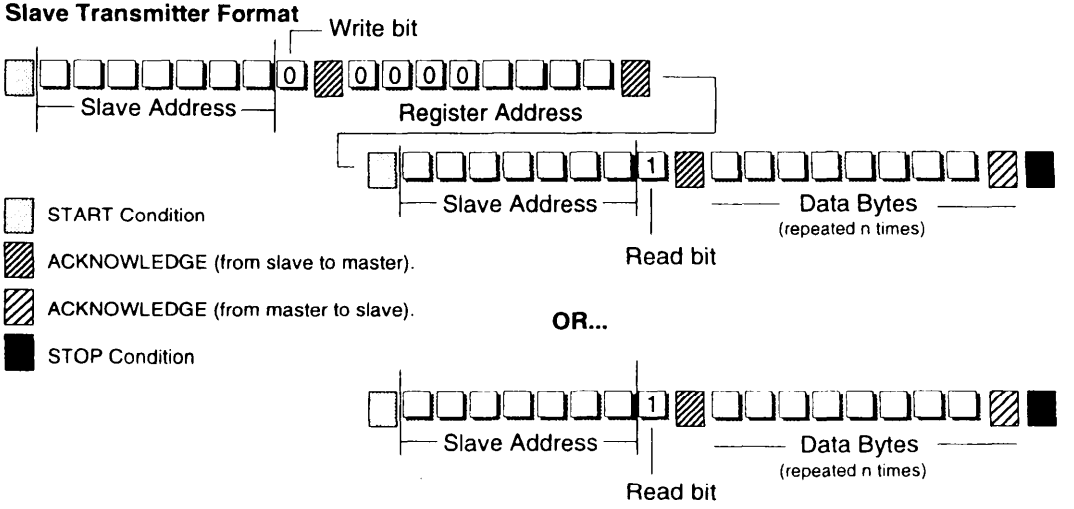
START Condition

ACKNOWLEDGE (from slave to master).

STOP Condition

NOTE: All addresses and data are sent and received with their MSB first.
A register or buffer address is always preceded by 4 Zeros (MSBs). When specifying a register or buffer address the internal pointer of that register or buffer is reset to its first position.
In the I2C mode the master is the controlling MCU.

Slave Transmitter Format



START Condition

ACKNOWLEDGE (from slave to master).

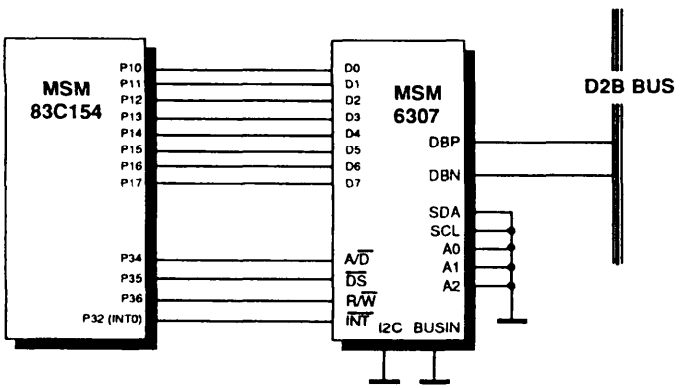
ACKNOWLEDGE (from master to slave).

STOP Condition

Parallel Interface Write & Read Timing (Ta = -40 to +85°C, V_{DD} = +5V ±10%)

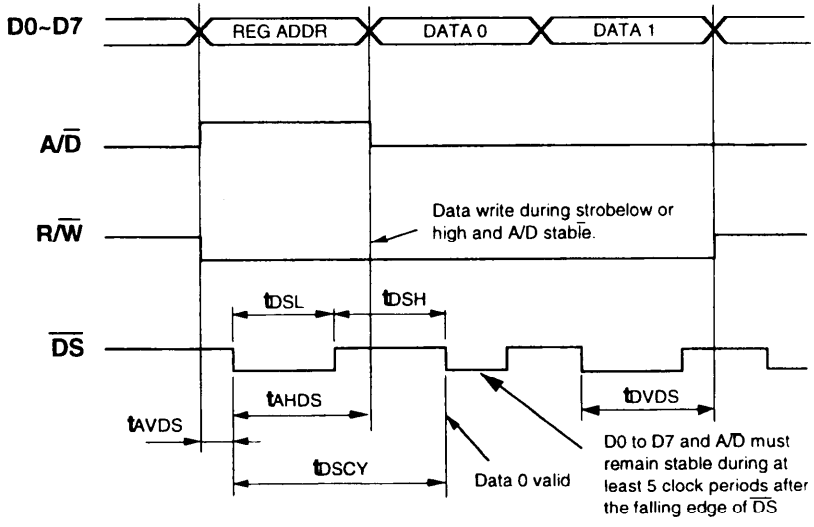
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
tCYC	Clock cycle time	-	166.67	-	ns
tAVDS	Address valid to data strobe low	-1 tcyc	-	-	ns
tDSL	Data strobe low time	3 tcyc	-	-	ns
tDSH	Data strobe high time	3 tcyc	-	-	ns
tAHDS	Address hold time after data strobe low	5 tcyc	-	-	ns
tDSCY	Data strobe cycle time	66 tcyc	-	-	ns
tDVDS	Data strobe low to data valid time	10 tcyc	-	-	ns
tDOV	First data valid after data strobe low (READ)	-	-	66 tcyc	ns

Simplified Circuit with 8-bit Controller

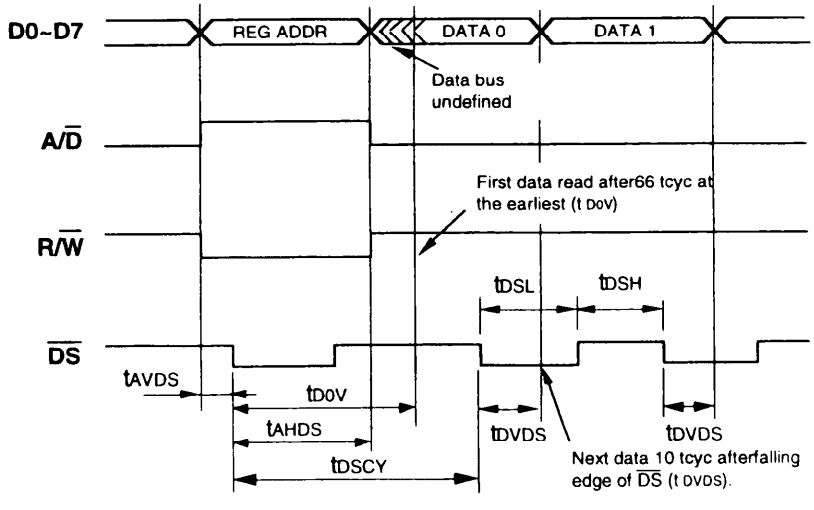


NOTE: Treatment of Unused pins when Parallel Interface mode.
SDA, SCL, A0, A1, A2 = GND

WRITE Timing



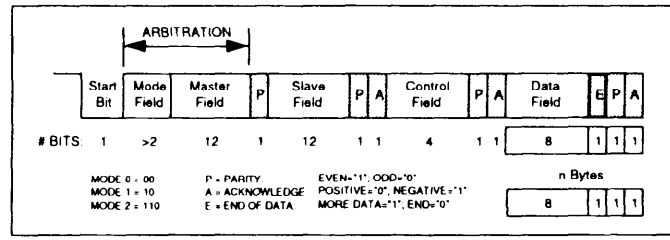
READ Timing



D2B Frame

Definition
A frame refers to the maximum amount of data that can be transceived after having won the bus arbitration. Every apparatus can transmit or receive for the duration of one frame or less but never for more. Within this frame several data bytes may be contained in the data field.

D2B FRAME



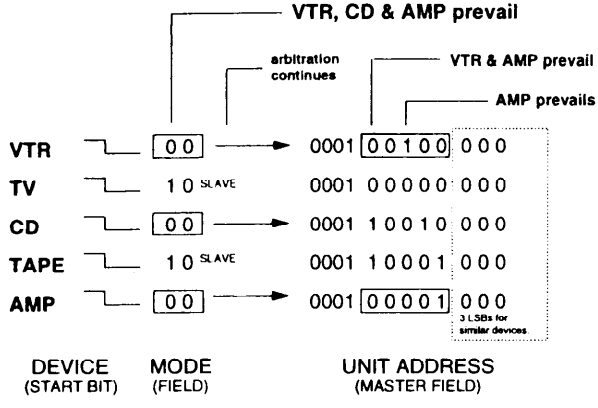
Start Bit
An apparatus that wants to master the bus tests whether it is in use and attempt to capture it. If it does not want to become a master it monitors the bus. To initiate a message transfer, the apparatus puts a "L" on the bus for a unique length of time. The other apparatus' will recognize it as the start bit.

Mode Field
Three different speed modes can be selected in the mode field. At the end of the start bit competing masters (which may be in different speed modes) enter the mode field by putting a series of bits on the bus, which select either of the available modes. The speed of the transfer is selected by the mode bits in the mode field. In case of competing masters, arbitration takes place during the mode bits, while the lowest mode prevails. The selection in the mode field entails a data rate and data amount limitation which is associated with each mode as displayed by the table below. MSM6307 supports mode 0 and mode 1.

Mode	Master-to-Slave	Slave-to-Master
0	2 Data Bytes 209 Bytes/sec.	2 Data Bytes 198 Bytes/sec
1	32 Data Bytes 2457 Bytes/sec	16 Data Bytes 1497 Bytes/sec

Master Field
Here, the address of the device attempting to obtain the bus is defined and followed by the parity bit for the address data. If two or more apparatus' are transmitting in the same mode, the arbitration continues into the master field. Due to the wired-AND property, the applying master with the lowest address prevails. Please refer to the diagram on the next page.
Competing masters put their address on the bus with the most significant bit (MSB) first. After each bit they read and compare. If the bus condition differs from their address bit they refrain from further attempts and continue as potential slaves.
At the end of the address field, the 12th. bit, only one master is still transmitting. This master, then, closes the address field by issuing a parity bit enabling the other apparatus' to check the validity of the address.

Arbitration Diagram



Control Field

With the MSB first, the master sends a 4-bit word onto the bus which contains the information about the nature of the transmission as listed in the table below. The control field is closed with a parity bit from the master and an acknowledgement bit from the slave, after which the master continues to the next field.

The slave reads the control bits and checks their parity. If the slave does not acknowledge the master may repeat the transfer. Acknowledgement is refused when the slave cannot perform the requested task or when the parity is even. In this event, it returns to the monitoring state.

Slave Field

Provided the arbitration has been won, the master sends the address of the apparatus it requires as a slave expressed in 12 bits headed by the MSB. All slaves continue reading the bus until the slave address bits do not agree with the own address and return to monitoring state. If the address matches the contacted slave reacts with an acknowledge bit provided the parities of master and slave addresses are odd and therefore correct.

B3	B2	B1	B0	FUNCTION	
0	0	0	0	Read slave status	READ
0	0	0	1	Reserved	
0	0	1	0	Read slave status and lock	
0	0	1	1	Read data and lock	
0	1	0	0	Read medium & least significant lock address nibble	
0	1	0	1	Read most significant lock address nibble	
0	1	1	0	Read slave status and unlock	
0	1	1	1	Read data and unlock	
1	0	0	0	Write memory address and lock	WRITE
1	0	0	1	Reserved	
1	0	1	0	Write commands and lock	
1	0	1	1	Write data and lock	
1	1	0	0	Reserved	
1	1	0	1	Reserved	
1	1	1	0	Write commands and unlock	
1	1	1	1	Write data and unlock	

D2B Frame, cont'd

Data Field
This last field is reserved for the actual data the master intends to send to or receive from the slave with the MSB first. It is composed of 8 data bits followed by an "End-of-Data" bit, indicating that the current Data Field is the last one (E = 0) or that more Data Fields are to be expected in the frame (E = 1), a Parity bit (odd parity) and an Acknowledge bit. The End-of-Data bit is required as the assigned frame is not necessarily carrying the maximum number of Data Fields. The transmission of the Data Field is succesfully concluded, when a positive acknowledge is received.

Parity Bits
They are included in order to protect the master address bits, slave address bits, control bits and the end-of-data bit. The parity is defined correct for an odd number of ones which equals to a logical "0". In case of even parity indicating a fault the parity bit is logic "1".

End-Of-Data Bit
Every data byte is followed by this EOD bit to inform whether the prior byte was the last byte to receive. The last data byte is signalled by a logic "0". If more data follows, by a logic "1".

Acknowledge Bit
In due course of every frame transfer there are 3 acknowledge bits demanded, after the slave address, after the control bits and after each data byte. The acknowledge bit is logic "0" for a positive acknowledge and is logic "1" in the opposite case.
The slave will not acknowledge the first acknowledge bit positive when one of the following conditions is met:

1. Slave not present,
2. Timing error,
3. Mode too high for the slave,
4. Parity fault on master and/or slave address.

If one of these cases occur, the transmission will be stopped entirely and cannot be resumed within the same frame.

The slave will not acknowledge the second acknowledge bit positive when one of the following conditions is met:

1. Parity fault on the control bits,
2. Receiver buffer not empty,
3. No data in data buffer,
4. If locked to another master,
5. Slave has no memory,
6. Receiver not locked when lock address requested,
7. Timing error,
8. Reserved control codes.

Also in these cases transmission will be stopped rigorously and the source can be investigated in the slave status register or in the interrupt register for timing errors.

The receiver will not acknowledge the third acknowledge bit positive when one of the following conditions is met:

1. Parity fault on the data,
2. Timing error during the last transfer,
3. Receiver buffer full.

The transmitter retries the last byte, unless the last Data Field was the last one fitting in the frame.

Cable Characteristics

The D2B system uses a balanced pair of cables to realize the bus structure with the following parameters:

Conductor resistance:	<0.1Ω/m
Impedance (Z_0):	120Ω ±20%
Bus length:	150m max.
Resistive termination:	120Ω ±5% (each end)
Number of apparatus:	50 sets max.

Stubs, if any, should not be longer than 2.5 meters.

Logic Levels

The D2B differential bus concept employs negative logic. When the bus level V_{DBP}-V_{DBN} is >+120mV the status is considered "H" and logic "0". Reversely, when the level is <+20mV the status is "L" and logic "1". These voltages are detection threshold values.

NOTES

Buffers & Registers

HEX	BINARY	ABBR	R/W	#B
00	00000000	GL	W	2
	Global register			
01	00000001	LA	R	2
	Lock address register			
02	00000010	MBW	W	34
	Master buffer (write)			
03	00000011	MBR	R	34
	Master buffer (read)			
04	00000100			
	Not defined			
05	00000101	SRB	R	34
	Slave receiver buffer			
06	00000110	STB	W	16
	Slave transmitter buffer			
07	00000111	INT	R	1
	Interrupt register			
08	00001000	CLINT	W	1
	Clear interrupt register			
09	00001001	SSR	R	1
	Slave status register			
0A	00001010	MCR	W	1
	Master command register			
0B	00001011	MSR	R	1
	Master status register			
0C	00001100	SRCR	W	1
	Slave receiver command register			
0D	00001101	SRSR	R	1
	Slave receiver status register			
0E	00001110	STCR	W	1
	Slave transmitter command register			
0F	00001111	STSR	R	1
	Slave transmitter status register			

Considering that the buffers and registers are split in 4 major functional groups the following display informs the individual allocations.

MASTER SECTION

Master Buffer Read/Write
Master Command Register
Master Status Register

SLAVE RECEIVER SECTION

Slave Receiver Buffer
Slave Receiver Command Register
Slave Receiver Status Register

SLAVE TRANSMITTER SECTION

Slave Transmitter Buffer
Slave Transmitter Command Register
Slave Transmitter Status Register

GENERAL SECTION

Global Register
Lock Address Register
Interrupt Register
Clear Interrupt Register
Slave Status Register

NOTE, that on the left table the Master Buffer is mentionend twice, once for read and once for write operations with different addresses. The actual buffer exists once with the specified 34 bytes capacity.

MASTER SECTION

A Transmission

Supply the master buffer with the receiving slave address, control code and data to be transmitted.

Initiate a master request using the Master Command Register to start the transmission.

Now transmitting; wait for an interrupt from the Master Section.

Read the Master Status Register to see how many bytes have been transmitted.

REMARK: If not all data bytes have been transmitted as intended, the not yet transmitted bytes can be transmitted within a next frame, another master transmission cycle.

Clear the master interrupt in the Clear Interrupt Register.

A Reception

Supply the Master Buffer with the slave address and the control code.

Initiate a master request using the Master Command Register to enable reception.

Now receiving; wait for an interrupt from the Master Section.

Read the Master Status Register to ascertain how many bytes have been received.

Read the received bytes from the Master Buffer.

Clear the Master interrupt in the Clear Interrupt Register.

Use of Registers, cont'd

SLAVE SECTIONS

SLAVE RECEIVER

Now receiving; wait for the interrupt from the slave receiver.

A Reception

Read the Slave Receiver Status Register to ascertain how many bytes have been received.

Read the bytes from the Slave Receiver Buffer.

Clear the slave receiver interrupt in the Clear Interrupt Register.

REMARK: The slave receiver buffer is automatically cleared at initialization, writing the Global Register.

Clear the slave receiver buffer by writing into the Slave Receiver Command Register (pointer returns to head).

SLAVE TRANSMITTER

A Transmission

Write the bytes to be transmitted into the buffer of the Slave Transmitter Buffer.

Declare data validity in the buffer by writing into the Slave Transmitter Command Register.

Now transmitting; wait for an interrupt from the Slave Transmitter.

Read the Slave Transmitter Status Register to ascertain how many bytes have been transmitted.

REMARK: If not all data bytes have been transmitted as intended, a new slave transmitter cycle may start by writing the residual bytes to the slave transmitter buffer.

Clear the slave transmitter interrupt in the Clear Interrupt Register.

Use of Registers, cont'd

GLOBAL SECTION

The **Global Register** is used to specify chip master addresses and other static parameters related to the intended communication cycle (every cycle sends or receives one D2B frame at a time). This register must be loaded before the chip can take any action.

The **Lock Address Register** contains the address of the master to which the device (as slave) is currently locked, in order to avoid interruption through unauthorized access during the communication (frame).

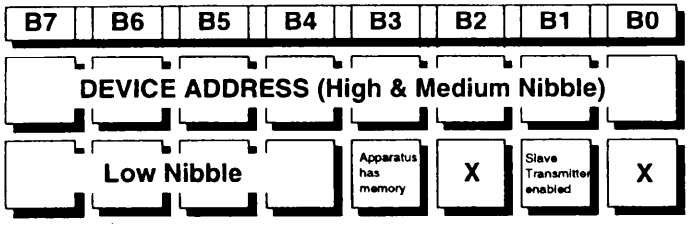
The **Slave Status Register** contains the Status Byte that is returned to a master in a case of which a "Read Slave Status" control code has been issued by that master.

The **Interrupt Register** MUST be examined after every hardware interrupt from the MSM6307. The byte in the Interrupt Register informs the source of the interrupt (master, slave receiver, slave transmitter interrupts / timing error or reset).

Consequently, the **Clear Interrupt Register** is employed to clear either of the possible interrupts. In case of a timing error during a frame the interrupt is issued by the originating unit and must be reset accordingly prior to taking any further action.

As for the individual use and interpretation of buffer/register contents, please refer to the Register Guide hereafter.

Register Guide GL 00H



The Global Register is used to specify the chip's apparatus address and some static properties of the chip. The address can be changed without violating the D2B protocol. The new address will come in effect at the instant of sending the next first mode bit either by another master or by the chip acting as the master itself. The chip will be unlocked after reloading the Global Register. It is essential that to initialize the chip first, loading this register, if not the chip will not perform any D2B communication task.

NOTES:

GLOBAL REGISTER

ADDRESS: 00H
TYPE: WRITE ONLY
SIZE: 2 BYTES
BOOLEAN:
TRUE = 1
FALSE = 0

1. Byte
B7~B0: B11~B4 of D2B device address.

2. Byte
B7~B4: B3~B0 of the D2B device address.
B3: Apparatus has property memory and accepts memory request.
B2: Don't care.
B1: D2B slave transmitter section enabled and chip accepts data request.
B0: Don't care.

NOTES:

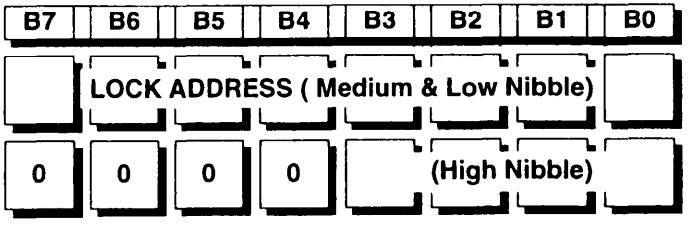
LOCK ADDRESS REGISTER

ADDRESS: 01H
TYPE: READ ONLY
SIZE: 2 BYTES
BOOLEAN:
TRUE = 1
FALSE = 0

1. Byte
B7~B0: Locking master address medium and low nibble (B7 to B0).

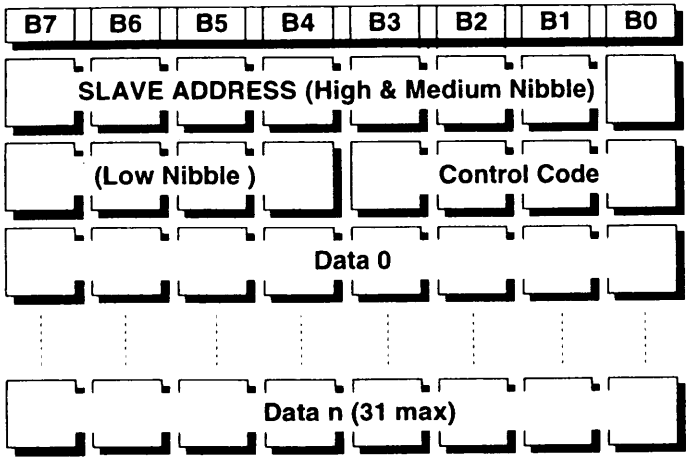
2. Byte
B7~B4: all "0"
B3~B0: Locking master address high nibble (B11 to B8).

NOTES:



This register is used to determine the address of the master to which the chip (slave) is locked at the moment. If locked the address in this register is valid. Also refer to the Slave Status Register 09H.

NOTES:



The Master Buffer must be loaded with all the information needed to initiate a message on the D2B bus. In case of a master receive action, only the first two bytes need to be filled. For a master transmit action at least three bytes must be filled. Writing this buffer does not yet initiate the message. Please refer to the Master Command Register, 0AH.

NOTES:

MASTER BUFFER (WRITE)

ADDRESS: 02H
TYPE: WRITE ONLY
SIZE: 34 BYTES
BOOLEAN:
TRUE = 1
FALSE = 0

1. Byte
B7~B0: High and medium nibble of the slave address to sent the frame to (B11 to B4).

2. Byte
B7~B4: Low nibble of the slave address to sent the frame to (B3 to B0).
B3~B0: Contain the control bits as per separate table (chapter D2B protocol).

3. Byte to nth Byte
These are the data bytes to be transmitted from the master to the slave. Maximum 32 bytes can be sent within one frame (Master transmitter and Mode 1, only).

NOTES:

MASTER BUFFER (READ)

ADDRESS: 03H
TYPE: READ ONLY
SIZE: 34 BYTES
BOOLEAN:

TRUE = 1
FALSE = 0

1. Byte

B7-B0: High and medium nibble of the slave address of the apparatus from where the bytes are read (B11 to B4).

2. Byte

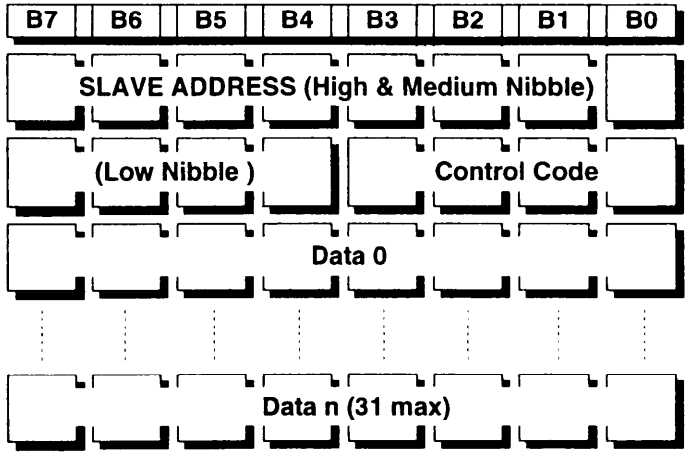
B7-B4: Low nibble of the slave address of the apparatus from where the bytes are read (B3 to B0).

B3-B0: Contain the control bits as per separate table (chapter D2B protocol).

3. Byte to nth Byte

These are the data bytes read from the slave. Maximum 32 bytes could be read within one frame, however, a slave may send 16 bytes maximum in Mode 1 and a mere 2 byte in Mode 0.

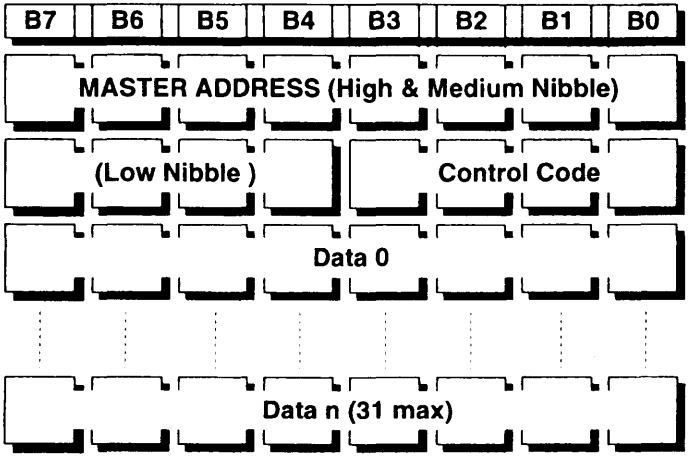
NOTES:



With a master receive action it is possible to read the data that was received from the slave apparatus. The 3rd. to nth. byte contain the actually received data, while the number of bytes received can be retrieved from the Master Status register, 0BH. In fact, the same memory location is used as for the Master Buffer Write, 02H.

NOTES:

Register Guide SRB 05H



The data received after a slave receive action can be read in the Slave Receiver Buffer. The 3rd. to nth. bytes represent the actual data received from the master, while the number of bytes received can be found in the Slave Receiver Status Register.

NOTES:

SLAVE RECEIVER BUFFER

ADDRESS: 05H
TYPE: READ ONLY
SIZE: 34 BYTES
BOOLEAN:
TRUE = 1
FALSE = 0

1. Byte

B7~B0: High and medium nibble of the master address of the apparatus from where the bytes are received (B11 to B4).

2. Byte

B7~B4: Low nibble of the master address of the apparatus from where the bytes are received (B3 to B0).

B3~B0: Contain the control bits as per separate table (chapter D2B protocol).

3. Byte to n Byte

These are the actual data bytes received from the master.

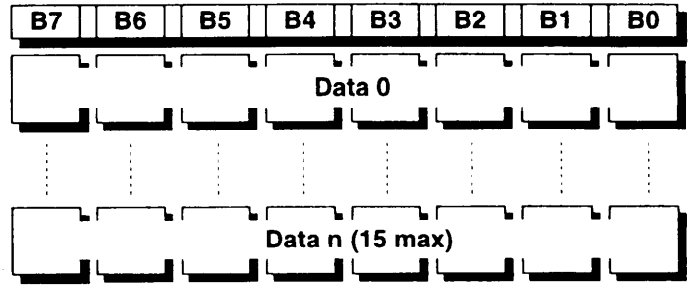
NOTES:

SLAVE TRANSMITTER BUFFER

ADDRESS: 06H
TYPE: WRITE ONLY
SIZE: 16 BYTES
BOOLEAN:
TRUE = 1
FALSE = 0

1. Byte ~ nth Byte
All bytes are reserved for data to be transmitted to the master.

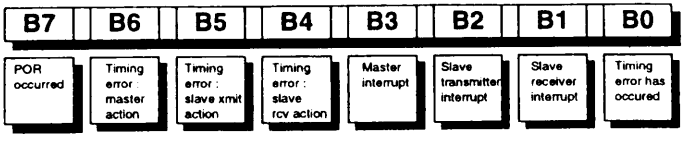
NOTES:



The Slave Transmitter Buffer must be filled with the data bytes to be transmitted when the chip is addressed as slave and the control code in the Master Buffer Read is "read data". This buffer is erased when the chip is addressed as slave and a "write memory address" is specified in the control field.

NOTES:

Register Guide IR 07H



This register has the information about the cause of an interrupt. It must be polled when the hardware interrupt is not used. Generally, the chip requires attention when the register contents is not "all zero". Note that bit B0 is OR-wired bit B6~B4.

NOTES:

INTERRUPT REGISTER

ADDRESS: 07H
TYPE: READ ONLY
SIZE: 1 BYTE
BOOLEAN:
TRUE = 1
FALSE = 0

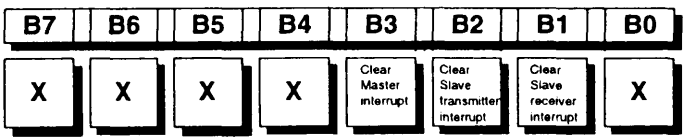
B7: Power-on reset occured.
B6: Timing error during master action.
B5: Timing error during slave transmit action.
B4: Timing error during slave receive action.
B3: Interrupt from the master section.
B2: Interrupt from the slave transmitter.
B1: Interrupt from the slave receiver.
B0: Timing error has occured. Source in B4~B6.

NOTES:

CLEAR INTERRUPT REGISTER

ADDRESS: 08H
TYPE: WRITE ONLY
SIZE: 1 BYTE
BOOLEAN:
TRUE = 1
FALSE = 0

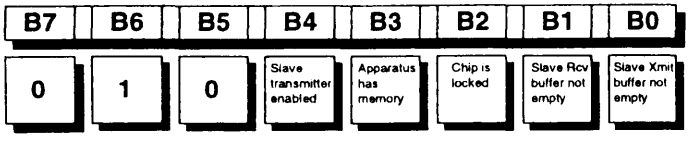
NOTES:



Likewise, this register is used to clear either of the interrupts and timing errors that may have occured. Writing to CLINT also clears an interrupt caused by POR.

NOTES:

Register Guide SSR 09H



This register allows to read the byte the chip transmits when it is addressed as slave and a "read slave status" control code is specified. Bits B7, B6 and B5 are always as shown above.

NOTES:

SLAVE STATUS REGISTER

ADDRESS: 09H
TYPE: READ ONLY
SIZE: 1 BYTE
BOOLEAN:
TRUE = 1
FALSE = 0

B7/B6: Always 0 and 1 indicating the highest mode available to the slave.

B5: Always "0"

B4: Slave transmitter enabled.

B3: Apparatus has memory.

B2: Chip is locked.

B1: Slave receiver buffer not empty.

B0: Slave transmitter buffer not empty.

NOTES:

Register Guide MCR 0AH

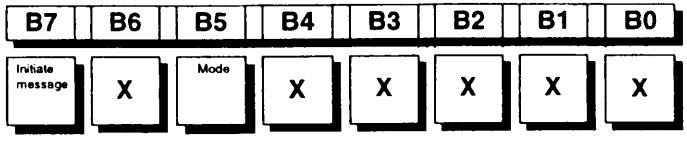
MASTER COMMAND REGISTER

ADDRESS: 0AH
TYPE: WRITE ONLY
SIZE: 1 BYTE
BOOLEAN:
TRUE = 1
FALSE = 0

B7 = 1: Request to initiate a message.
B7 = 0:
Cancel message request.
After a maximum duration of a frame (>17ms) it can be determined whether the action was successful. When after that time still no master interrupt is received, one can be certain that the message was not initiated.

B5 = 1: Sets mode 1
B5 = 0: Sets mode 0

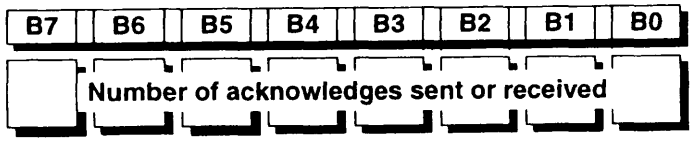
NOTES:



This register is used to start a message on the D2B bus as a master and defines the mode.

NOTES:

Register Guide MSR 0BH



The result of a master action can be ascertained using this register which is normally read after a master interrupt.

NOTES:

MASTER STATUS REGISTER

ADDRESS: 0BH
TYPE: READ ONLY
SIZE: 1 BYTE
BOOLEAN:
TRUE = 1
FALSE = 0

B7~B0=0:
No acknowledge received or transmitted, thus no data transceived.
B7~B0=1:
A positive slave address acknowledge received during the last transfer and no data transceived.
B7~B0=2:
A positive slave address and control acknowledge received during the last transfer and no data transceived.
B7~B0=>2:
A positive slave address and control acknowledge received during the last transfer and (B7~B0)-2 positive data acknowledges received or transmitted. Value minus 2 data bytes transceived.

NOTES:

B7 = 0:
Cancel message request.
After a maximum duration of a time slot (>17ms) it can be determined whether the action was successful. When after that time still no master interrupt is received, one can be certain that the message was not initiated.

B5 = 1: Sets mode 1
B5 = 0: Sets mode 0

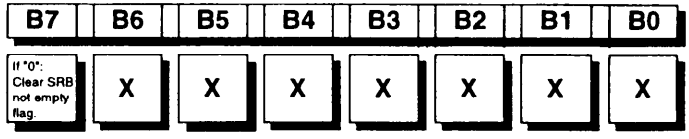
SLAVE RECEIVER COMMAND REGISTER

ADDRESS: 0CH
TYPE: WRITE ONLY
SIZE: 1 BYTE
BOOLEAN:
TRUE = 1
FALSE = 0

B7 = 1: No effect

B7 = 0: Clears the "Not empty" flag and the Slave Status Register's (09H) bit B1 is set to "0". Then, the chip is ready to receive new bytes.

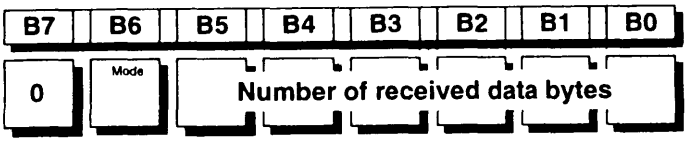
NOTES:



This register allows to declare the Slave Receiver Buffer empty after which the chip is anewly ready to receive data.

NOTES:

Register Guide SRSR 0DH



Here, the number of received data bytes and the mode in which this data was received are specified. Normally this register is read after a slave receiver interrupt.

NOTES:

SLAVE RECEIVER STATUS REGISTER

ADDRESS: 0DH
TYPE: READ ONLY
SIZE: 1 BYTE
BOOLEAN:
TRUE = 1
FALSE = 0

B7: Always "0"

B6: "0" = Mode 0
"1" = Mode 1

B5-B0: Have the number of received data bytes.

NOTES:

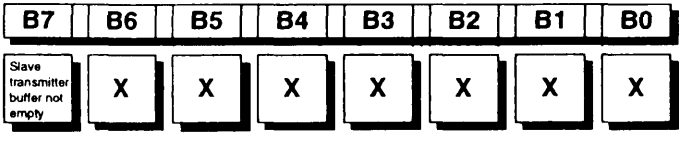
SLAVE TRANSMITTER COMMAND REGISTER

ADDRESS: 0EH
TYPE: WRITE ONLY
SIZE: 1 BYTE
BOOLEAN:
TRUE = 1
FALSE = 0

B7 = 1: Set "Slave Transmitter Buffer not empty" flag (B0 of 0AH) and declare data ready to be transmitted.

B7 = 0: Reset "Slave Transmitter Buffer not empty" flag (B0 of 0AH) to receive new bytes. This command has no effect when the chip is already busy with a frame in which the bytes are being send. If after a maximum duration of a frame (>17ms) still no interrupt is received from the slave transmitter section it is certain that no bytes have been or will be send.

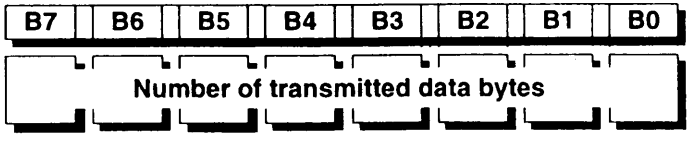
NOTES:



With this register the data in the Slave Transmitter Buffer is declared valid. When the chip is addressed as slave and the control code is "read data" the data in the Slave Transmitter Buffer will be transmitted.

NOTES:

Register Guide STSR 0FH



This register specifies the number of data bytes which are transmitted in a slave transmit action. Normally, it is examined after a slave transmitter interrupt.

NOTES:

SLAVE TRANSMITTER STATUS REGISTER

ADDRESS: 0FH
TYPE: READ ONLY
SIZE: 1 BYTE
BOOLEAN:
TRUE = 1
FALSE = 0

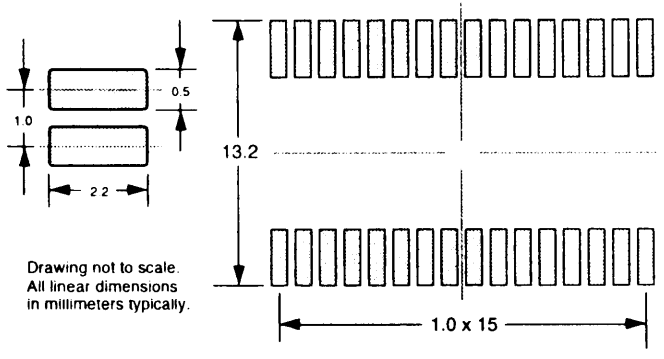
B7: Always "0"

B6: "0" = Mode 0
"1" = Mode 1

B5~B0: Have the number of received data bytes.

NOTES:

SMD Print Pad Layout



Soldering Recommendation

PACKAGE	PART NUMBER	CONDITIONS	METHOD	PEAK TEMP
28-pin DIP	MSM6307RS	-	Wave soldering	260°C x 10 sec
32-pin SOP	MSM6307GS-VK	with or without dry pack	IR-Reflow	240°C x 10 sec
			Vapor Reflow	215°C x 10 sec

For more details on IC packaging, handling and soldering, please refer to **PACKAGE INFORMATION** Handbook , 4. edition, December 1989.

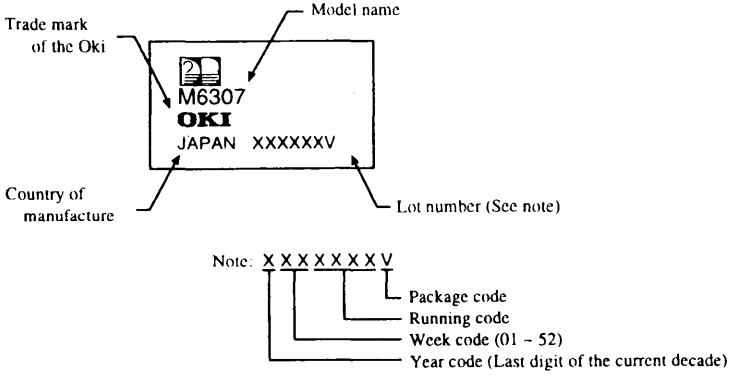
Package Outline

28-Pin Dual In-Line Package

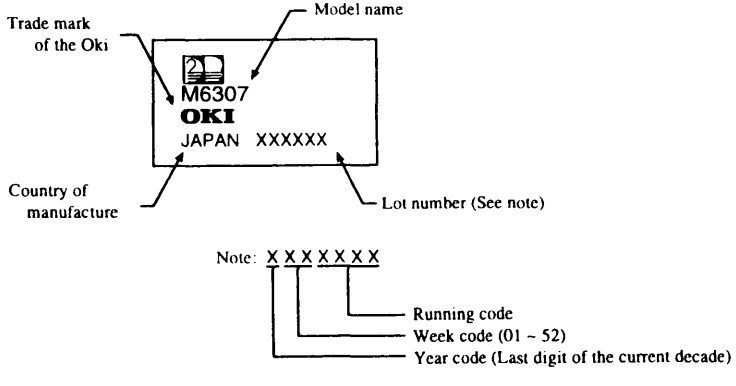
32-Pin Small Outline Package

NOTE: All linear dimensions in millimeters typically, unless otherwise specified.

● MSM6307GS-VK



● MSM6307GS-VK



NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Please make sure before using the product that the information you are referring to is up-to-dated.

2. The outline of action and examples of application circuits described herein have been chosen as an explanation of the standard action and performance of the product. When you actually plan to use the product, please ensure that the outside conditions are reflected in the actual circuit and assembling designs.

3. NO RESPONSIBILITY IS ASSUMED BY US FOR ANY CONSEQUENCE RESULTING FROM ANY WRONG OR IMPROPER USE OR OPERATION, ETC. OF THE PRODUCT.

4. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.

5. The products described herein falls within the category of strategical goods, etc. under the Foreign Exchange and Foreign Trade Control Law. Accordingly, before exporting the product you are required under the Law to file the application for the export license by your local Government.

6. No part of the contents contained herein may be reprinted or reproduced without our prior permission.

7. MS-DOS is a registered trademark of Microsoft Corporation.

OKI

Oki Electric Industry Co., Ltd.

Head Office Annex 7-5-25 Nishishinjuku, Shinjuku-ku, Tokyo 160 Japan
Tel: 3-5386-8100 Fax: 3-5386-8110 Telex: J27662 OKIDENED

For further information please contact:

Oki Electric Industry Co., Ltd.
Head Office Annex
7-5-25 Nishishinjuku,
Shinjuku-ku, Tokyo 160, Japan
Tel 3-5386-8100
Fax 3-5386-8110
Telex J27662 OKIDENED
Electronic Devices Group
Overseas Marketing Dept

Oki Semiconductor
785 North Mary Avenue,
Sunnyvale, CA 94086 U.S.A.
Tel: 408-720-1900
Fax: 408-720-1918
Telex: 296687 OKI SNTA

Oki Electric Europe GmbH
Hellersbergstraße 2,
D-4040 Neuss
Germany
Tel: 2131-15960
Fax: 2131-103539
Telex: 8517427 OKI D

Oki Electronics (Hong Kong) Ltd.
Suite 1801-4, Tower 1,
China Hong kong City,
33 Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel 7362336
Fax 7362395
Telex 45999 OKIHK HX

Printed in Japan

E3S005361