OKI Semiconductor

MSM538022E

524,288-Word x 16-Bit or 1,048,576-Word x 8-Bit MASKROM

DESCRIPTION

The OKI MSM538002E is a high-speed CMOS Mask ROM that can electrically switch between 524,288-word x 16-bit or 1,048,576-word x 8-bit configurations. The MSM538002E Operates on a single 5.0V power supply and is TTL compatible. The chip's asynchronous I/O requires no external clock assuring easy operation. A power-down mode provides low power dissipation when the chip is not selected. The CE and OE pins are provided as control signals that permit three-stated output allowing easy memory expansion on a system bus. The MSM531602C is suited for use as large capacity fixed memory for microcomputers and data terminals.

FEATURES

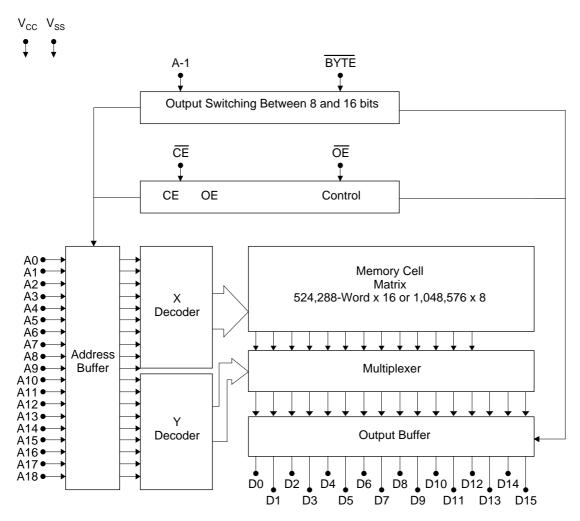
Single 5.0V power supply 524,288-words x 16-bit / 1,048,576-words x 8-bit Access time 80ns MAX Input/Output TTL compatible Tri-State output configurations Internal powerdown function Packages: 42-PIN PLASTIC DIP (DIP42-P-600-2.54) (MSM538002E-xxRS) 44-PIN PLASTIC SOP (SOP44-P-600-1.27-K) (MSM538002E-xxGS-K) 44-PIN PLASTIC TSOP (TSOPII44-P-400-0.8-K) (MSM538002E-xxTS-AK) 8MEPROM (42-PIN) pin compatible

PIN CONFIGURATION

				NC	1		44	NC
A18	1	42	NC	A18	2		43	NC
A17	2	41	A8	A17	3		42	A8
A7	3	40	A9	A7	4		41	A9
A6	4	39	A10	A6	5		40	A10
A5	5	38	A11	A5	6		39	A11
A4	6	37	A12	A4	7		38	A12
АЗ	7	36	A13	А3	8		37	A13
A2	8	35	A14	A2	9		36	A14
A1	9	34	A15	A1	10		35	A15
A0	10	33	A16	A0	11		34	A16
CE	11	32	BYTE	CE	12		33	BYTE
V_{SS}	12	31	V_{SS}	V_{SS}	13		32	V_{SS}
ŌĒ	13	30	D15/A-1	ŌĒ	14		31	D15/A-1
D0	14	29	D7	D0	15		30	D7
D8	15	28	D14	D8	16		29	D14
D1	16	27	D6	D1	17		28	D6
D9	17	26	D13	D9	18		27	D13
D2	18	25	D5	D2	19		26	D5
D10	19	24	D12	D10	20		25	D12
D3	20	23	D4	D3	21		24	D4
D11	21	22	V_{CC}	D11	22		23	V_{CC}
	42PIN DIP	1			L	44PIN SOP/ TSOP	ı	

Pin Name	Function
D15/A-1	Data output / address input
A0 to A18	Address input
D0 to D15	Data output
CE	Chip enable
ŌĒ	Output enable
BYTE	Mode switch
V _{CC} , V _{SS}	Power supply

BLOCK DIAGRAM



FUNCTION TABLE

CE	ŌĒ	BYTE	A-1/D15	D0 to D7	D8 to D15	D _{OUT} Mode	LSB	MSB
Н	Х	Х	X	Hi-Z	Hi-Z	Hi-Z		
L	Н	Х	X	Hi-Z	Hi-Z	111-2		
L	L	Н	Input Inhibited (D15)	D0 to D7	D8 to D15	16 bit	A0	A18
L	L	L	L	D0 to D7	Hi-Z	8 bit	A-1	A18
L	L	L	Н	D8 to D15	Hi-Z	O DIL	A-1	Alo

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rated Value	Unit
Power Supply Voltage	V _{CC}		-0.3 to 7	V
Input Voltage	V _I	to V _{SS}	-0.3 to V_{CC} + 0.5	V
Output Voltage	Vo		-0.3 to $V_{CC} + 0.5$	V
Power Dissipation	P _D	Per Package T _{opr} = 25°C	1.0	W
Operating Temperature	T _{opr}	_	0 to 70	°C
Storage Temperature	T _{stg}	_	-55 to 150	°C

Recommended Operating Conditions

Davamatan	Symbol Conditions	Conditions	F	I Imit		
Parameter		Min.	Тур.	Max.	Unit	
Dower Supply Voltage	V _{CC}	_	4.75	5.0	5.25	V
Power Supply Voltage	V _{SS}	-	0.0	0.0	0.0	V
"H" Input Voltage	V _{IH}	_	2.2	5.0	V _{CC} +0.5	V
"L" Input Voltage	V _{IL}	_	-0.3	0.0	0.8	V
Operating Temperature	T _{opr}	_	0	_	70	°C

DC Characteristics

 $(V_{CC} = 5V \pm 5\%, Ta = 0 \text{ to } 70^{\circ}C)$

Darameter	Cymbal	Conditions	R	I Imit		
Parameter	Symbol Conditions		Min.	Тур.	Max.	Unit
"H" Output Voltage	V _{OH}	$I_{OH} = -400 \mu A$	2.4	_	_	V
"L" Output Voltage	V _{OL}	I _{OH} = 2.1mA	_	_	0.4	V
Input Leakage Current	I _{LI}	$V_I = 0$ to V_{CC}	-10		10	μA
Output Leakage Current	I _{LO}	$V_O = 0$ to V_{CC} $CE = V_{IH MIN}$	-10	_	10	μA
Power Supply Current (Operating)	I _{CC}	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}, t_C = 80$ ns	_	_	60	mA
Power Supply Current	I _{CCS} 1	$\overline{CE} = V_{CC} - 0.2V$	_	-	50	μA
(Standby)	I _{ccs}	CE = V _{IH MIN}	_	_	500	μA

AC CHARACTERISTICS

Timing conditions

Parameter	Conditions
Input Signal Level	V _{IH} =3.0V, V _{IL} =0.0V
Transtion Time	t _r =t _f =5ns
Timing Reference Level	Input Voltage=1.5V Output Voltage=0.8V&2.0V
Load Condition	CL=50pF+1TTL

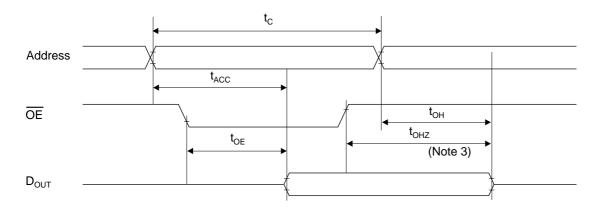
Read Cycle

(Ta = 0 to 70°C)

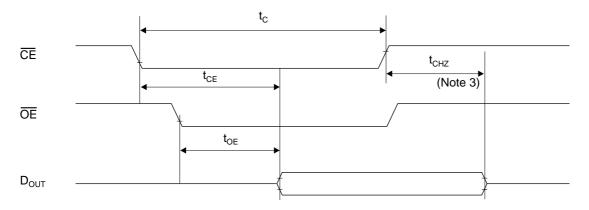
Dominion to a	Symbol	Conditions	R			
Parameter			Min.	Тур.	Max.	Unit
Cycle time	t _C	_	80	_	_	ns
Address Access time	t _{ACC}		_	_	80	ns
CE Access time	t _{CE}	_	_	_	80	ns
OE Access time	t _{OE}	_	_	_	40	ns
CE Output Disable time	t _{CHZ}	_	0	_	35	ns
OE Output Disable time	t _{OHZ}	_	0	_	30	ns
Output Hold time	t _{OH}	_	0	_	_	ns

MSM538022E

Read Cycle (Note 1)



Read Cycle (Note 2)



Note)

- \overline{CE} is low level.
 Address is fixed before or at the same time when \overline{CE} level falls.
 t_{CHZ} & t_{OHZ} indicate the time until floating. They are not determined by the output level.

I/O CAPACITANCE

Davastar	Cumala al	Canditions	R	I Imit		
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
Input Capacitance	Cı	V _I =0V	_	_	8	pF
Output Capacitance	Co	V _O =0V	_	_	10	pF



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ADDRESSES & SEMICONDUCTOR WEB SITES

OKI Electric Industry Co., Ltd.,

Device Business Group, 10-3, Shibaura, 4-chome, Minato-ku, Tokyo 108, Japan, Tel.: +81-(0)3-5445-6327,

Fax.: +81-(0)3-5445-6328,

http://www.oki.co.jp/OKI/DBG/english/index.htm

(NOTE: URL is case sensitive)

OKI Semiconductor Group.

785 North Mary Avenue, Sunnyvale, CA 94086, U.S.A., Tel.: +1-408-720-1900, Fax.: +1-408-720-1918, http://www.okisemi.com/

OKI Electric Europe GmbH,

Head Office Europe, Hellersbergstrasse 2, D-41460 Neuss, Germany, Tel: +49-2131-15960, Fax: +49-2131-103539, http://www.oki-europe.de/

OKI Electronics (Hong Kong) Ltd.,

Suite 1901-1&19, Tower 3, China Hong Kong City, 33 Canton Road, Tsimshatsui, Kowloon, Hong Kong, Tel.: +852-2-736-2336,

Fax.: +852-2-736-2395

OKI Semiconductor (Asia) Pte. Ltd.,

78 Shenton Way 09-01, Singapore 0207, Tel.: +65-221-3722, Fax.: +65-323-5376

OKI Semiconductor (Asia) Pte. Ltd.,

Taipei Branch,

7th Fl. No.260, Tun Hwa North Road,

Taipei, Taiwan, R.O.C., Sumitomo-Flysun Building, Tel.: +886-2-2719-2561,

Fax.: +886-2-2715-2892 http://www.oki.net.tw/

For further information, please contact:

