FEDS51V4223C-03

OKI Semiconductor

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MSM51V4223C

262,263-Word × 4-Bit Field Memory

GENERAL DESCRIPTION

The OKI MSM51V4223C is a high performance 1-Mbit, 256 K × 4-bit, Field Memory. It is designed for high-speed serial access applications such as HDTVs, conventional NTSC TVs, VTRs, digital movies and Multi-media systems. It is a FRAM for wide or low end use as general commodity TVs and VTRs, exclusively. The MSM51V4223C is not designed for the other use or high end use in medical systems, professional graphics systems which require long term picture, and data storage systems and others. The 1-Mbit capacity fits one field of a conventional NTSC TV screen and cascaded two MSM51V4223Cs make one frame of the screen: more than two MSM51V4223Cs can be cascaded directly without any delay devices among the MSM51V4223Cs. (Cascading of MSM51V4223C provides larger storage depth or a longer delay).

Each of the 4-bit planes has separate serial write and read ports that employ independent control clocks to support asynchronous read and write operations. Different clock rates are also supported that allow alternate data rates between write and read data streams.

The MSM51V4223C provides high speed FIFO, First-In First-Out, operation without external refreshing: it refreshes its DRAM storage cells automatically, so that it appears fully static to the users.
Moreover, fully static type memory cells and decoders for serial access enable refresh free serial access operation, so that the serial read and/or write control clock can be halted high or low for any duration as long as the power is on. Internal conflicts of memory access and refreshing operations are prevented by special arbitration logic.

The MSM51V4223C's function is simple, and similar to a digital delay device whose delay-bit-length is easily set by reset timing. The delay length, number of read delay clocks between write and read, is determined by externally controlled write and read reset timings.

Additional SRAM serial registers, or line buffers for the initial access of 256 × 4-bit enable high speed first-bit-access with no clock delay just after the write or read reset timings.

The MSM51V4223C is similar in operation and functionality to OKI 1-Mbit Field Memory MSM51V4221C besides direct cascade capability. (As for MSM51V4221C operation compatible 2-Mbit Field Memory, OKI has MSM51V8221A as a sister device of MSM51V8222A).

Additionally, the MSM51V4223C has write mask function or input enable function (IE), and read-data skipping function or output enable function (OE). The differences between write enable (WE) and input enable (IE), and between read enable (RE) and output enable (OE) are that WE and RE can stop serial write/read address increments, but IE and OE cannot stop the increment, when write/read clocking is continuously applied to MSM51V4223C. The input enable (IE) function allows the user to write into selected locations of the memory only, leaving the rest of the memory contents unchanged. This facilitate data processing to display a "picture in picture" on a TV screen.

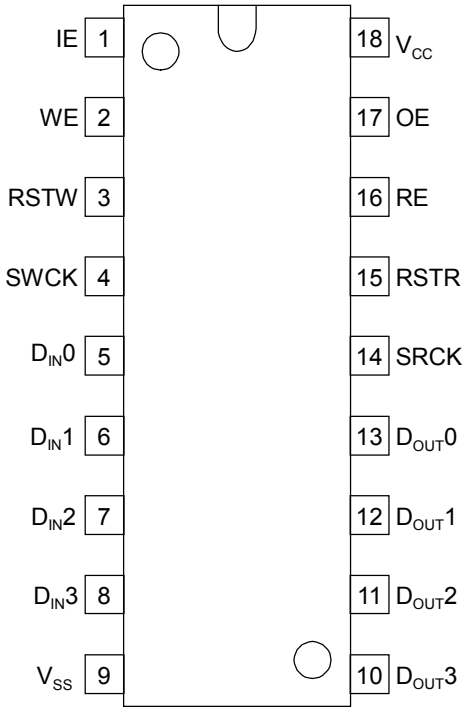
FEATURES

- Single power supply: 3.3 V ± 0.3 V
- 512 Rows × 512 Column × 4 bits
- Fast FIFO (First-in First-out) operation
- High speed asynchronous serial access
  Read/Write cycle time 30 ns/40 ns
  Access time 30 ns/35 ns
- Direct cascading capability
- Write mask function (Input enable control)
- Data skipping function (Output enable control)
- Self refresh (No refresh control is required)
- Package:
  18-pin 300 mil plastic DIP (DIP18-P-300-2.54) (Product: MSM51V4223C-xxRA)
  xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)	Cycle Time (Min.)	Package
MSM51V4223C-30RA	30 ns	30 ns	300 mil 18-pin DIP
MSM51V4223C-40RA	35 ns	40 ns	

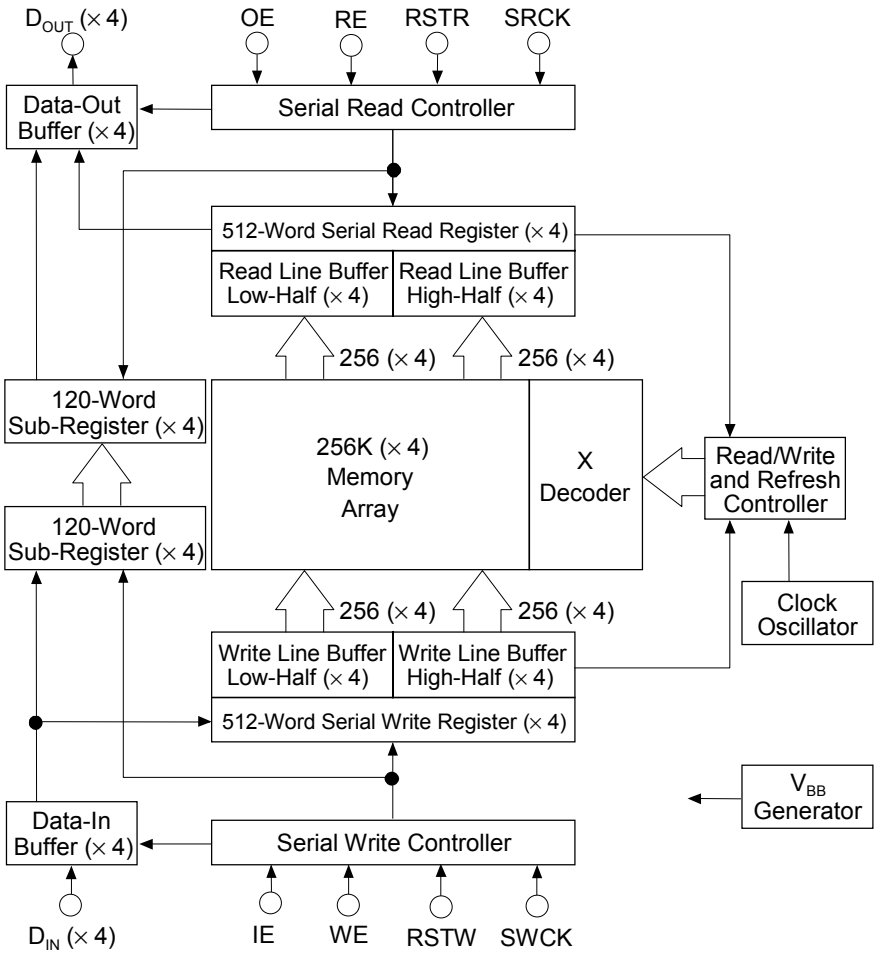
PIN CONFIGURATION (TOP VIEW)



18-Pin Plastic DIP

Pin Name	Function
SWCK	Serial Write Clock
SRCK	Serial Read Clock
WE	Write Enable
RE	Read Enable
IE	Input Enable
OE	Output Enable
RSTW	Write Reset Clock
RSTR	Read Reset Clock
$D_{IN}0$ to 3	Data Input
$D_{OUT}0$ to 3	Data Output
V_{CC}	Power Supply (3.3 V)
V_{SS}	Ground (0 V)

BLOCK DIAGRAM



OPERATION

Write Operation

The write operation is controlled by three clocks, SWCK, RSTW, and WE. Write operation is accomplished by cycling SWCK, and holding WE high after the write address pointer reset operation or RSTW.
Each write operation, which begins after RSTW, must contain at least 130 active write cycles, i.e. SWCK cycles while WE is high. To transfer the last data to the DRAM array, which at that time is stored in the serial data registers attached to the DRAM array, an RSTW operation is required after the last SWCK cycle.
Note that every write timing of MSM51V4223C is delayed by one clock compared with read timings for easy cascading without any interface delay devices.

Write Reset: RSTW

The first positive transition of SWCK after RSTW becomes high resets the write address counters to zero. RSTW setup and hold times are referenced to the rising edge of SWCK. Because the write reset function is solely controlled by the SWCK rising edge after the high level of RSTW, the states of WE and IE are ignored in the write reset cycle.
Before RSTW may be brought high again for a further reset operation, it must be low for at least two SWCK cycles.

Data Inputs: D_{IN}0 to 3

Write Clock: SWCK

The SWCK latches the input data on chip when WE is high, and also increments the internal write address pointer. Data-in setup time t_{DS}, and hold time t_{DH} are referenced to the rising edge of SWCK.

Write Enable: WE

WE is used for data write enable/disable control. WE high level enables the input, and WE low level disables the input and holds the internal write address pointer. There are no WE disable time (low) and WE enable time (high) restrictions, because the MSM51V4223C is in fully static operation as long as the power is on. Note that WE setup and hold times are referenced to the rising edge of SWCK.

Input Enable: IE

IE is used to enable/disable writing into memory. IE high level enables writing. The internal write address pointer is always incremented by cycling SWCK regardless of the IE level. Note that IE setup and hold times are referenced to the rising edge of SWCK.

Read Operation

The read operation is controlled by three clocks, SRCK, RSTR, and RE. Read operation is accomplished by cycling SRCK, and holding RE high after the read address pointer reset operation or RSTR.
Each read operation, which begins after RSTR, must contain at least 130 active read cycles, i.e. SRCK cycles while RE is high.

Read Reset: RSTR

The first positive transition of SRCK after RSTR becomes high resets the read address counters to zero. RSTR setup and hold times are referenced to the rising edge of SRCK. Because the read reset function is solely controlled by the SRCK rising edge after the high level of RSTR, the states of RE and OE are ignored in the read reset cycle.Before RSTR may be brought high again for a further reset operation, it must be low for at least two SRCK cycles.

Data Out: D_{OUT}0 to 3

Read Clock: SRCK

Data is shifted out of the data registers. It is triggered by the rising edge of SRCK when RE is high during a read operation. The SRCK input increments the internal read address pointer when RE is high.
The three-state output buffer provides direct TTL compatibility (no pullup resistor required). Data out is the same polarity as data in. The output becomes valid after the access time interval t_{AC} that begins with the rising edge of SRCK. There are no output valid time restriction on MSM51V4223C.

Read Enable: RE

The function of RE is to gate of the SRCK clock for incrementing the read pointer. When RE is high before the rising edge of SRCK, the read pointer is incremented. When RE is low, the read pointer is not incremented. RE setup times (t_{RENS} and t_{RDSS}) and RE hold times (t_{RENH} and t_{RDSH}) are referenced to the rising edge of the SRCK clock.

Output Enable: OE

OE is used to enable/disable the outputs. OE high level enables the outputs. The internal read address pointer is always incremented by cycling SRCK regardless of the OE level. Note that OE setup and hold times are referenced to the rising edge of SRCK.

Power-up and Initialization

On power-up, the device is designed to begin proper operation after at least 100 μs after V_{CC} has stabilized to a value within the range of recommended operating conditions. After this 100 μs stabilization interval, the following initialization sequence must be performed.
Because the read and write address counters are not valid after power-up, a minimum of 130 dummy write operations (SWCK cycles) and read operations (SRCK cycles) must be performed, followed by an RSTW operation and an RSTR operation, to properly initialize the write and the read address pointer. Dummy write cycles/RSTW and dummy read cycles/RSTR may occur simultaneously.
If these dummy read and write operations start while V_{CC} and/or the substrate voltage has not stabilized, it is necessary to perform an RSTR operation plus a minimum of 130 SRCK cycles plus another RSTR operation, and an RSTW operation plus a minimum of 130 SRCK cycles plus another RSTW operation to properly initialize read and write address pointers.

Old/New Data Access

There must be a minimum delay of 600 SWCK cycles between writing into memory and reading out from memory. If reading from the first field starts with an RSTR operation, before the start of writing the second field (before the next RSTW operation), then the data just written will be read out.
The start of reading out the first field of data may be delayed past the beginning of writing in the second field of data for as many as 119 SWCK cycles. If the RSTR operation for the first field read-out occurs less than 119 SWCK cycles after the RSTW operation for the second field write-in, then the internal buffering of the device assures that the first field will still be read out. The first field of data that is read out while the second field of data is written is called “old data”.
In order to read out “new data”, i.e., the second field written in, the delay between an RSTW operation and an RSTR operation must be at least 600 SRCK cycles. If the delay between RSTW and RSTR operations is more than 120 but less than 600 cycles, then the data read out will be undetermined. It may be “old data” or “new” data, or a combination of old and new data. Such a timing should be avoided.

Cascade Operation

The MSM51V4223C is designed to allow easy cascading of multiple memory devices. This provides higher storage depth, or a longer delay than can be achieved with only one memory device.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Input Output Voltage	V_T	at Ta = 25°C, V_{SS}	–1.0 to 4.6	V
Output Current	I_{OS}	Ta = 25°C	50	mA
Power Dissipation	P_D	Ta = 25°C	1	W
Operating Temperature	T_{opr}	—	0 to 70	°C
Storage Temperature	T_{stg}	—	–55 to 150	°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Power Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	V_{CC}	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	–0.3	0	0.8	V

DC Characteristics

Parameter	Symbol	Condition	Min.	Max.	Unit
Input Leakage Current	I_{LI}	$0 < V_I < V_{CC}$, Other Pins Tested at V = 0 V	–10	10	µA
Output Leakage Current	I_{LO}	$0 < V_O < V_{CC}$	–10	10	µA
Output “H” Level Voltage	V_{OH}	I_{OH} = –1 mA	2.4	—	V
Output “L” Level Voltage	V_{OL}	I_{OL} = 2 mA	—	0.4	V
Operating Current	I_{CC1}	Minimum Cycle Time, Output Open	—	30	mA
Standby Current	I_{CC2}	Input Pin = V_{IH}/V_{IL}	—	3	mA

Capacitance

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance (D_{IN}, SWCK, SRCK, RSTW, RSTR, WE, RE, IE, OE)	C_I	7	pF
Output Capacitance (D_{OUT})	C_O	7	pF

AC Characteristics

(V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to 70°C)

Parameter	Symbol	MSM51V4223C-30		MSM51V4223C-40		Unit
		Min.	Max.	Min.	Max.	
Access Time from SRCK	t_{AC}	—	30	—	35	ns
D_{OUT} Hold Time from SRCK	t_{DDCK}	6	—	6	—	ns
D_{OUT} Enable Time from SRCK	t_{DECK}	6	30	6	35	ns
SWCK "H" Pulse Width	t_{WSWH}	12	—	17	—	ns
SWCK "L" Pulse Width	t_{WSWL}	12	—	17	—	ns
Input Data Setup Time	t_{DS}	3	—	5	—	ns
Input Data Hold Time	t_{DH}	6	—	6	—	ns
WE Enable Setup Time	t_{WENS}	0	—	0	—	ns
WE Enable Hold Time	t_{WENH}	5	—	5	—	ns
WE Disable Setup Time	t_{WDSS}	0	—	0	—	ns
WE Disable Hold Time	t_{WDSH}	5	—	5	—	ns
IE Enable Setup Time	t_{IENS}	0	—	0	—	ns
IE Enable Hold Time	t_{IENH}	5	—	5	—	ns
IE Disable Setup Time	t_{IDSS}	0	—	0	—	ns
IE Disable Hold Time	t_{IDSH}	5	—	5	—	ns
WE "H" Pulse Width	t_{WWEH}	5	—	10	—	ns
WE "L" Pulse Width	t_{WWEL}	5	—	10	—	ns
IE "H" Pulse Width	t_{WIEH}	5	—	10	—	ns
IE "L" Pulse Width	t_{WIEL}	5	—	10	—	ns
RSTW Setup Time	t_{RSTWS}	0	—	0	—	ns
RSTW Hold Time	t_{RSTWH}	10	—	10	—	ns
SRCK "H" Pulse Width	t_{WSRH}	12	—	17	—	ns
SRCK "L" Pulse Width	t_{WSRL}	12	—	17	—	ns
RE Enable Setup Time	t_{RENS}	0	—	0	—	ns
RE Enable Hold Time	t_{RENH}	5	—	5	—	ns
RE Disable Setup Time	t_{RDSS}	0	—	0	—	ns
RE Disable Hold Time	t_{RDSH}	5	—	5	—	ns
OE Enable Setup Time	t_{OENS}	0	—	0	—	ns
OE Enable Hold Time	t_{OENH}	5	—	5	—	ns
OE Disable Setup Time	t_{ODSS}	0	—	0	—	ns
OE Disable Hold Time	t_{ODSH}	5	—	5	—	ns
RE "H" Pulse Width	t_{WREH}	5	—	10	—	ns
RE "L" Pulse Width	t_{WREL}	5	—	10	—	ns
OE "H" Pulse Width	t_{WOEH}	5	—	10	—	ns
OE "L" Pulse Width	t_{WOEL}	5	—	10	—	ns
RSTR Setup Time	t_{RSTRS}	0	—	0	—	ns
RSTR Hold Time	t_{RSTRH}	10	—	10	—	ns
SWCK Cycle Time	t_{SWC}	30	—	40	—	ns
SRCK Cycle Time	t_{SRC}	30	—	40	—	ns
Transition Time (Rise and Fall)	t_T	3	30	3	30	ns

Notes: 1. Input signal reference levels for the parameter measurement are V_{IH} = 3.0 V and V_{IL} = 0 V. The transition time t_T is defined to be a transition time that signal transfers between V_{IH} = 3.0 V and V_{IL} = 0 V.

2. AC measurements assume t_T = 3 ns.

3. Read address must have more than a 600 address delay than write address in every cycle when asynchronous read/write is performed.

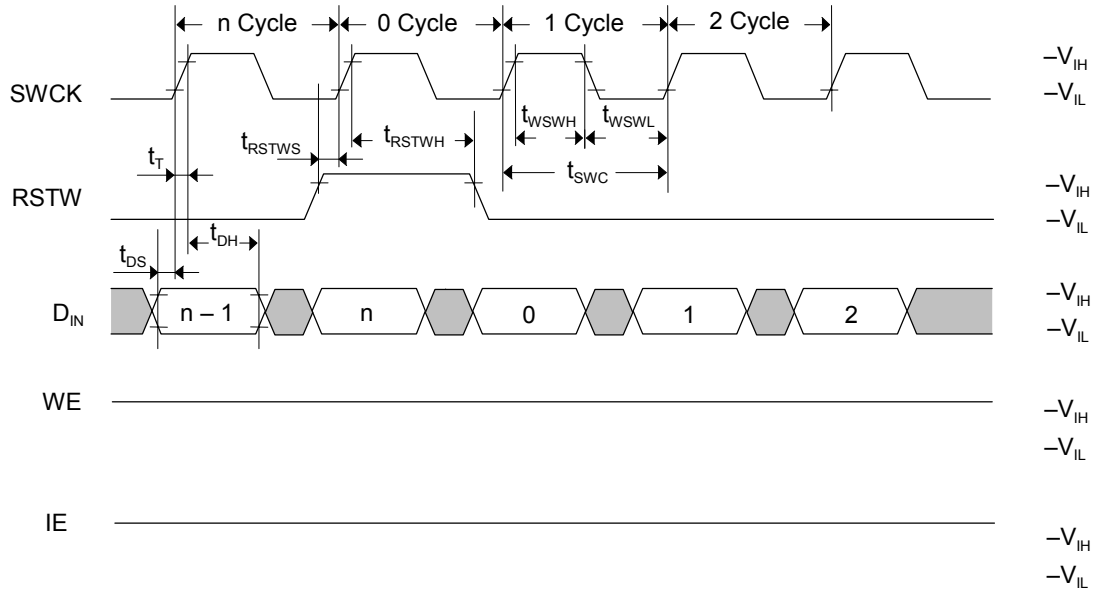
4. Read must have more than a 600 address delay than write in order to read the data written in a current series of write cycles which has been started at last write reset cycle: this is called “new data read”.
   When read has less than a 119 address delay than write, the read data are the data written in a previous series of write cycles which had been written before at last write reset cycle: this is called “old data read”.

5. When the read address delay is between more than 120 and less than 599, read data will be undetermined. However, normal write is achieved in this address condition.

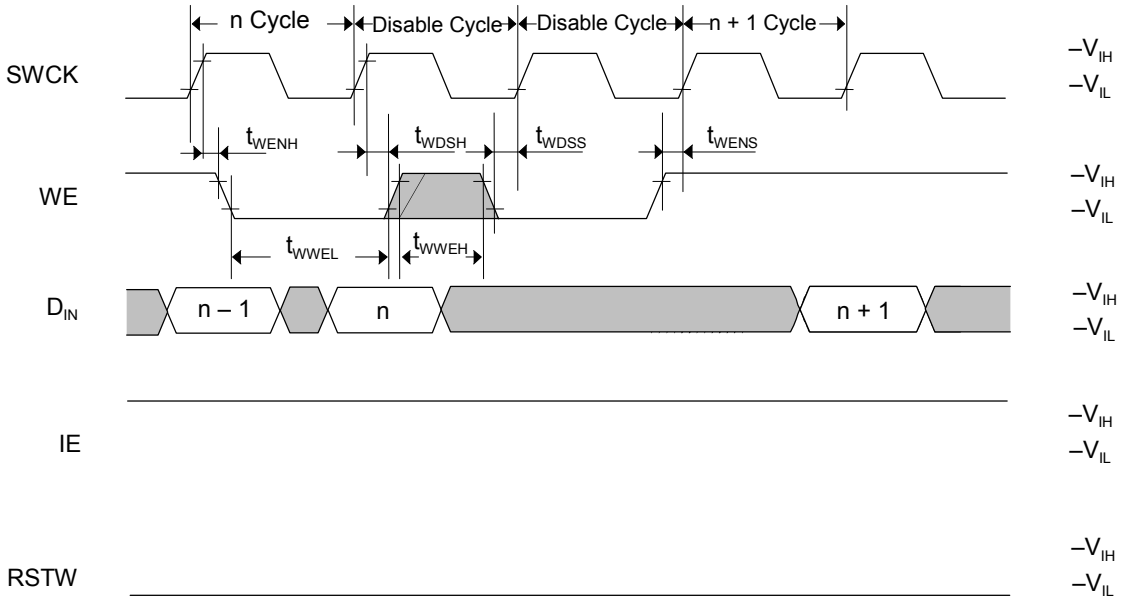
6. Outputs are measured with a load equivalent to 1 TTL load and 30 pF.
   Output reference levels are V_{OH} = 2.0 V and V_{OL} = 0.8 V.

TIMING WAVEFORM

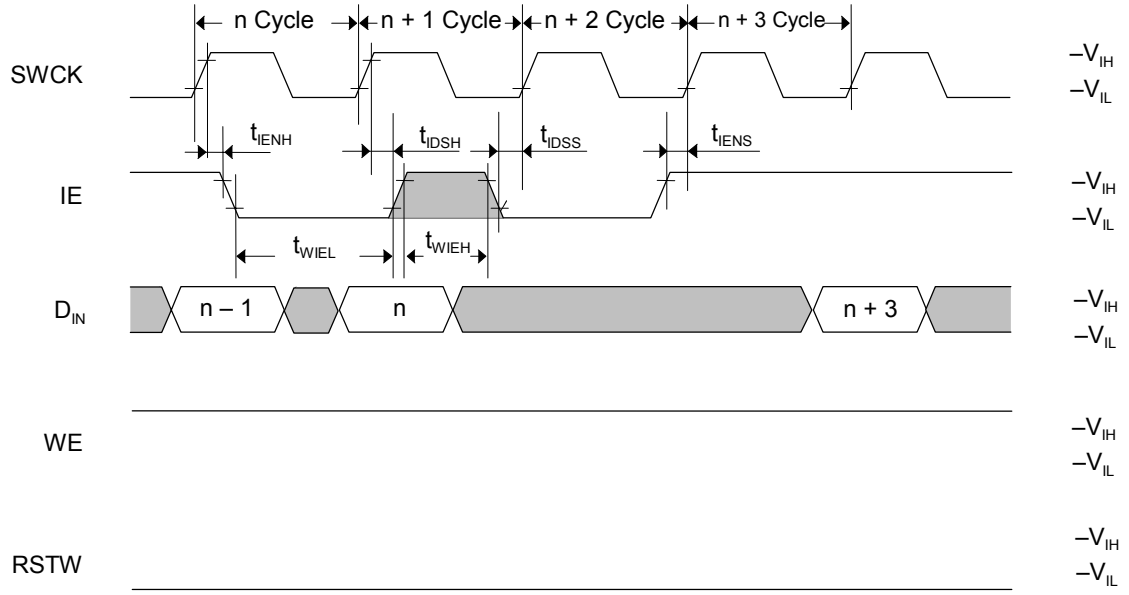
Write Cycle Timing (Write Reset)



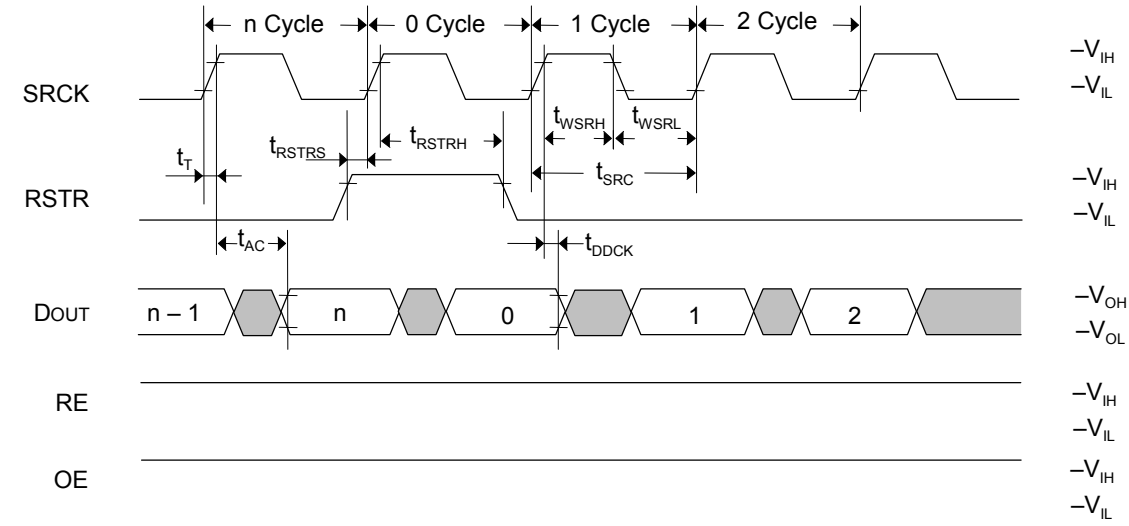
Write Cycle Timing (Write Enable)



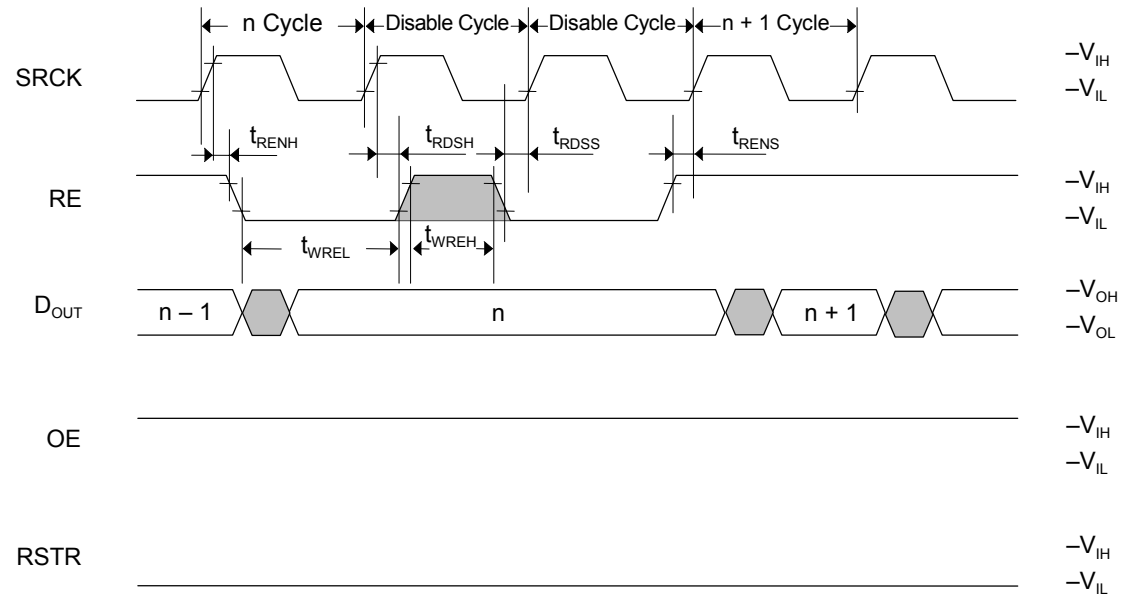
Write Cycle Timing (Input Enable)



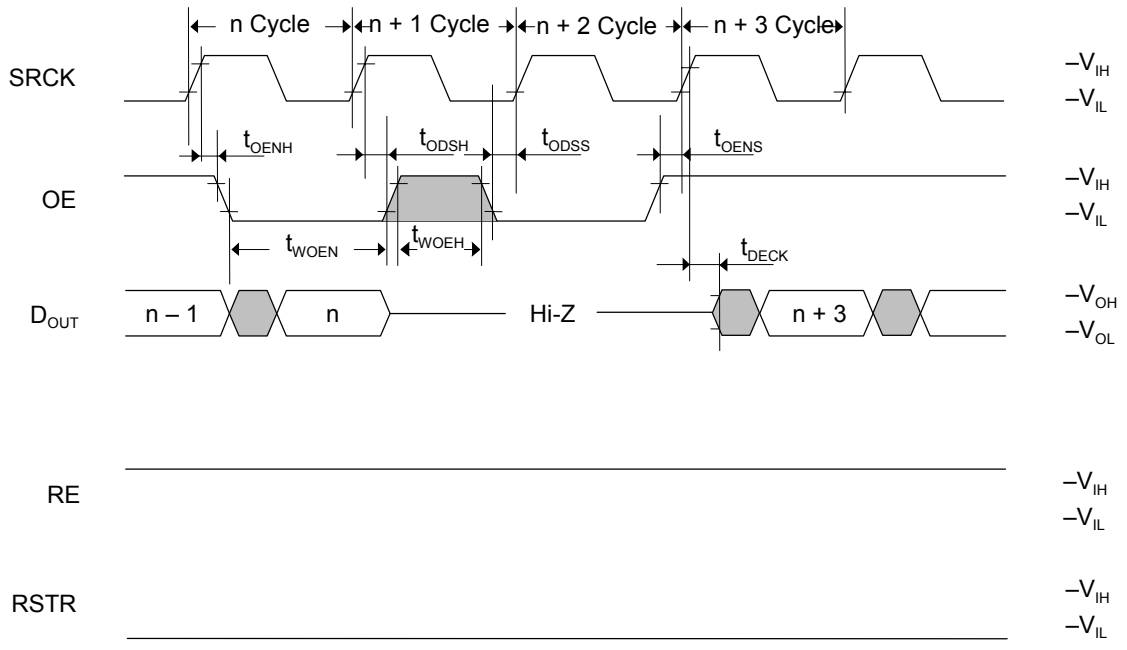
Read Cycle Timing (Read Reset)



Read Cycle Timing (Read Enable)



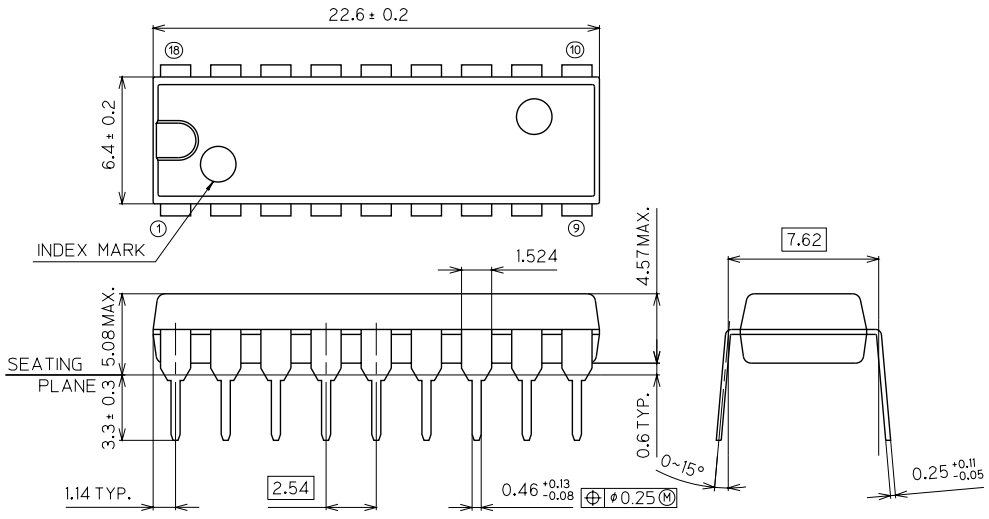
Read Cycle Timing (Output Enable)



PACKAGE DIMENSIONS

(Unit: mm)

DIP18-P-300-2.54



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	1.30 TYP.
Rev. No./Last Revised	2/Dec. 11, 1996

Oki Electric Industry Co., Ltd.

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