OKI Semiconductor MR27V3202E

2,097,152-Word × 16-Bit or 4,194,304-Word × 8-Bit Production Programmed Read Only Memory (P2ROM)

GENERAL DESCRIPTION

The MR27V3202E is a 32 Mbit Production Programmed Read Only Memory (P2ROM) that can be electrically switched between 2,097,152-word \times 16-bit and 4,194,304-word \times 8-bit by the state of the BYTE pin. The MR27V3202E supports high speed asynchronous read operation using a single 3.3V power supply.

FEATURES

 \cdot 2097,152-word \times 16-bit/4,194,304-word \times 8-bit electrically switchable configuration

 \cdot +3.3 V power supply

- Access time 90 ns MAX
- Operating current 50 mA MAX
- · Standby current 50 µA MAX

· Input/Output TTL compatible

· Three-state output

· Packages:

44-pin plastic SOP (SOP44-P-600-1.27-K) (Product Name : MR27V3202EMA) 44-pin plastic TSOP (TSOP II 44-P-400-0.80-K) (Product Name : MR27V3202ETP)

MR27V3202E

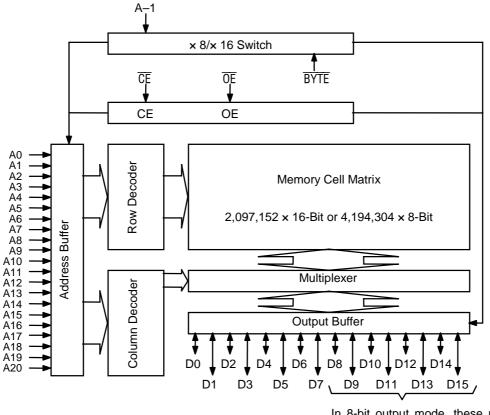
PIN CONFIGURATION (TOP VIEW)

| NC 1 \bigcirc 44 A20 A18 2 43 A19 A17 3 42 A8 A7 4 41 A9 A6 5 40 A10 A5 6 39 A11 A4 7 38 A12 A3 8 37 A13 A2 9 36 A14 A1 10 35 A15 A0 11 34 A16 CE 12 33 BYTE V _{ss} 13 32 V _{ss} 0E 14 31 D15/A-1 D0 15 30 D7 D8 16 29 D14 D1 17 28 D6 D9 18 27 D13 D2 19 26 D5 D10 20 25 D12 D3 21 24 D4 D11 22 23 V _{cc} | | r | 1 |
|--|--------------------|---|--------------------|
| A17 3 42 A8A7 4 41 A9A6 5 40 A10A5 6 39 A11A4 7 38 A12A3 8 37 A13A2 9 36 A14A1 10 35 A15A0 11 34 A16 CE 12 33 BYTE V_{ss} 13 32 V_{ss} $\overline{0E}$ 14 31 D15/A-1D0 15 30 D7D8 16 29 D14D1 17 28 D6D9 18 27 D13D2 19 26 D5D10 20 25 D12D3 21 24 D4 | NC 1 | 0 | 44 A20 |
| A7441A9A6540A10A5639A11A4738A12A3837A13A2936A14A11035A15A01134A16CE1233BYTE V_{ss} 1332 V_{ss} 0E1431D15/A-1D01530D7D81629D14D11728D6D91827D13D21926D5D102025D12D32124D4 | A18 2 | | 43 A19 |
| A6 5 40 A10 A5 6 39 A11 A4 7 38 A12 A3 8 37 A13 A2 9 36 A14 A1 10 35 A15 A0 11 34 A16 CE 12 33 BYTE V _{ss} 13 32 V _{ss} 0E 14 31 D15/A-1 D0 15 30 D7 D8 16 29 D14 D1 17 28 D6 D9 18 27 D13 D2 19 26 D5 D10 20 25 D12 D3 21 24 D4 | A17 3 | | 42 A8 |
| A5 6 39 A11 A4 7 38 A12 A3 8 37 A13 A2 9 36 A14 A1 10 35 A15 A0 11 34 A16 \overline{CE} 12 33 BYTE V_{ss} 13 32 V_{ss} \overline{OE} 14 31 D15/A-1 D0 15 30 D7 D8 16 29 D14 D1 17 28 D6 D9 18 27 D13 D2 19 26 D5 D10 20 25 D12 D3 21 24 D4 | A7 4 | | 41 A9 |
| A4 7 38 A12 A3 8 37 A13 A2 9 36 A14 A1 10 35 A15 A0 11 34 A16 \overline{CE} 12 33 BYTE V_{ss} 13 32 V_{ss} \overline{OE} 14 31 D15/A–1 $D0$ 15 30 D7 $D8$ 16 29 D14 $D1$ 17 28 D6 $D9$ 18 27 D13 $D2$ 19 26 D5 $D10$ 20 25 D12 $D3$ 21 24 D4 | A6 5 | | 40 A10 |
| A3 8 37 A13 A2 9 36 A14 A1 10 35 A15 A0 11 34 A16 \overline{CE} 12 33 BYTE V_{ss} 13 32 V_{ss} \overline{OE} 14 31 D15/A-1 D0 15 30 D7 D8 16 29 D14 D1 17 28 D6 D9 18 27 D13 D2 19 26 D5 D10 20 25 D12 D3 21 24 D4 | A5 6 | | 39 A11 |
| A2 9 36 A14 A1 10 35 A15 A0 11 34 A16 CE 12 33 BYTE V _{ss} 13 32 V _{ss} OE 14 31 D15/A-1 D0 15 30 D7 D8 16 29 D14 D1 17 28 D6 D9 18 27 D13 D2 19 26 D5 D10 20 25 D12 D3 21 24 D4 | A4 7 | | 38 A12 |
| A1 10 35 A15 A0 11 34 A16 CE 12 33 BYTE V _{SS} 13 32 V _{SS} OE 14 31 D15/A-1 D0 15 30 D7 D8 16 29 D14 D1 17 28 D6 D9 18 27 D13 D2 19 26 D5 D10 20 25 D12 D3 21 24 D4 | A3 8 | | 37 A13 |
| A0 11 34 A16 CE 12 33 BYTE V _{SS} 13 32 V _{SS} OE 14 31 D15/A–1 D0 15 30 D7 D8 16 29 D14 D1 17 28 D6 D9 18 27 D13 D2 19 26 D5 D10 20 25 D12 D3 21 24 D4 | A2 9 | | 36 A14 |
| CE 12 33 BYTE V _{ss} 13 32 V _{ss} OE 14 31 D15/A-1 D0 15 30 D7 D8 16 29 D14 D1 17 28 D6 D9 18 27 D13 D2 19 26 D5 D10 20 25 D12 D3 21 24 D4 | A1 10 | | 35 A15 |
| V _{ss} 13 32 V _{ss} 0E 14 31 D15/A-1 D0 15 30 D7 D8 16 29 D14 D1 17 28 D6 D9 18 27 D13 D2 19 26 D5 D10 20 25 D12 D3 21 24 D4 | A0 11 | | 34 A16 |
| OE 14 31 D15/A-1 D0 15 30 D7 D8 16 29 D14 D1 17 28 D6 D9 18 27 D13 D2 19 26 D5 D10 20 25 D12 D3 21 24 D4 | <u>CE</u> 12 | | 33 BYTE |
| D0 15 30 D7 D8 16 29 D14 D1 17 28 D6 D9 18 27 D13 D2 19 26 D5 D10 20 25 D12 D3 21 24 D4 | V _{SS} 13 | | 32 V _{ss} |
| D8 16 29 D14 D1 17 28 D6 D9 18 27 D13 D2 19 26 D5 D10 20 25 D12 D3 21 24 D4 | 0E 14 | | 31 D15/A–1 |
| D1 17 28 D6 D9 18 27 D13 D2 19 26 D5 D10 20 25 D12 D3 21 24 D4 | D0 15 | | 30 D7 |
| D9 18 27 D13 D2 19 26 D5 D10 20 25 D12 D3 21 24 D4 | D8 16 | | 29 D14 |
| D2 19 26 D5 D10 20 25 D12 D3 21 24 D4 | D1 17 | | 28 D6 |
| D10 20 25 D12 D3 21 24 D4 | D9 18 | | 27 D13 |
| D3 21 24 D4 | D2 19 | | 26 D5 |
| | D10 20 | | 25 D12 |
| D11 22 23 V _{cc} | D3 21 | | 24 D4 |
| | D11 22 | | 23 V _{cc} |

44-pin SOP, TSOP(II)

| Pin name | Functions | |
|-----------------|---------------------------|--|
| D15/A–1 | Data output/Address input | |
| A0 to A20 | Address input | |
| D0 to D14 | Data output | |
| CE | Chip enable | |
| ŌĒ | Output enable | |
| BYTE | Mode switch | |
| V _{cc} | Power supply voltage | |
| V _{ss} | GND | |
| NC | Non connection | |

BLOCK DIAGRAM



In 8-bit output mode, these pins are placed in a high-Z state and pin D15 functions as the A-1 address pin.

FUNCTION TABLE

| Mode | CE | ŌĒ | BYTE | V _{cc} | D0 to D7 | D8 to D14 | D15/A–1 |
|----------------|----|----|------|-----------------|------------------|------------------|---------|
| Read (16-Bit) | L | L | Н | | | D _{OUT} | |
| Read (8-Bit) | L | L | L | | D _{OUT} | Hi–Z | L/H |
| Output disable | L | Н | Н | 0.0.1/ | | Hi–Z | |
| | | | L | 3.3 V | | 111-2 | * |
| Standby | | | Н | | | Hi–Z | |
| | Н | * | L | | | | |

*: Don't Care (H or L)

MR27V3202E

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Value | Unit |
|----------------------------------|-----------------|----------------------|------------------------------|------|
| Operating temperature under bias | Та | | 0 to 70 | °C |
| Storage temperature | Tstg | _ | -55 to 125 | °C |
| Input voltage | V | | –0.5 to V _{cc} +0.5 | V |
| Output voltage | Vo | relative to V_{ss} | –0.5 to V _{cc} +0.5 | V |
| Power supply voltage | V _{cc} | | –0.5 to 5 | V |
| Power dissipation per package | P _D | _ | 1.0 | W |

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to 70°C)

| Parameter | Symbol | Condition | Min. | Тур. | Max. | Unit |
|--------------------------------------|-----------------|-----------------------------|--------|------|-----------------------|------|
| V _{cc} power supply voltage | V _{cc} | | 3.0 | _ | 3.6 | V |
| Input "H" level | V _{IH} | $V_{\rm CC}$ = 3.0 to 3.6 V | 2.2 | _ | V _{cc} +0.5* | V |
| Input "L" level | V _{IL} | | -0.5** | _ | 0.6 | V |

Voltage is relative to V_{SS} .

* : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.

**: -1.5V(Min.) when pulse width of undershoot is less than 10ns.

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ELECTRICAL CHARACTERISTICS

DC Characteristics

| | | | | (V _{cc} = 3.3 \ | / ± 0.3 V, Ta | = 0 to 70°C) |
|---|-------------------|---|--------|--------------------------|-----------------------|--------------|
| parameter | Symbol | Condition | Min. | Тур. | Max. | Unit |
| Input leakage current | I _{LI} | $V_{I} = 0$ to V_{CC} | — | — | 10 | μA |
| Output leakage current | I _{LO} | $V_{\rm O} = 0$ to $V_{\rm CC}$ | — | — | 10 | μA |
| V _{cc} power supply current | I _{ccsc} | $\overline{CE} = V_{CC}$ | — | — | 50 | μA |
| (Standby) | I _{CCST} | $\overline{CE} = V_{IH}$ | — | — | 1 | mA |
| V _{cc} power supply current (Read) | I _{CCA} | $\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$ $tc = 90 \text{ ns}$ | — | — | 50 | mA |
| Input "H" level | V _{IH} | — | 2.2 | _ | V _{cc} +0.5* | V |
| Input "L" level | V _{IL} | — | -0.5** | — | 0.6 | V |
| Output "H" level | V _{OH} | I _{он} = –2 mA | 2.4 | _ | | V |
| Output "L" level | V _{OL} | $I_{OL} = 4 \text{ mA}$ | _ | _ | 0.4 | V |

Voltage is relative to V_{ss}.

* : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.

** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

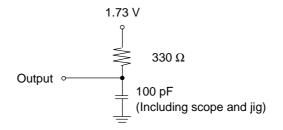
AC Characteristics

| | | | $(V_{CC} = 3.3 V \pm 0.3 V, 1a = 0.070)$ | | | | |
|---------------------|------------------|--|--|------|------|--|--|
| Parameter | Symbol | Condition | Min. | Max. | Unit | | |
| Address cycle time | t _C | — | 90 | — | ns | | |
| Address access time | t _{ACC} | $\overline{CE} = \overline{OE} = V_{IL}$ | — | 90 | ns | | |
| CE access time | t _{CE} | $\overline{OE} = V_{IL}$ | — | 90 | ns | | |
| OE access time | t _{oe} | $\overline{CE} = V_{IL}$ | — | 45 | ns | | |
| Output disable time | t _{CHZ} | $\overline{OE} = V_{IL}$ | 0 | 30 | ns | | |
| Output disable time | t _{OHZ} | $\overline{CE} = V_{IL}$ | 0 | 25 | ns | | |
| Output hold time | t _{oH} | $\overline{CE} = \overline{OE} = V_{IL}$ | 0 | _ | ns | | |

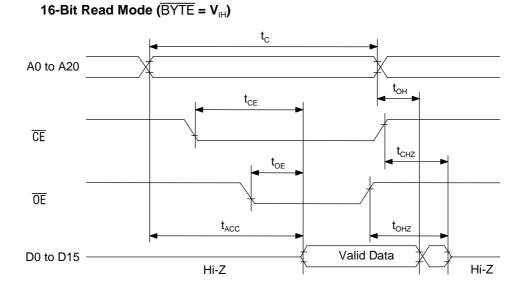
$(V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, \text{ Ta} = 0 \text{ to } 70^{\circ}\text{C})$

Measurement conditions

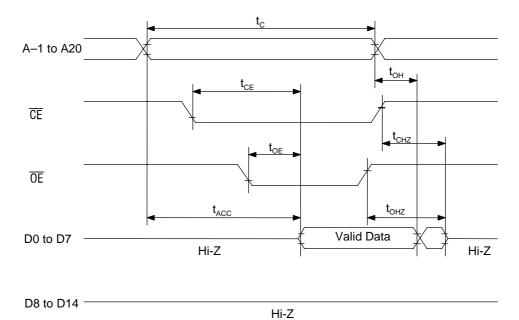
| Input signal level | 0 V/3 V |
|-------------------------------|-------------|
| Input timing reference level | 0.8 V/2.0 V |
| Output load | 100 pF |
| Output timing reference level | 0.8 V/2.0 V |



Timing Chart (Read Cycle)



8-Bit Read Mode (BYTE = V_{IL})



OKI Semiconductor

MR27V3202E

Pin Capacitance

(V_{cc} = 3.3 V, Ta = 25°C, f = 1 MHz)

| Parameter | Symbol | Condition | Min. | Тур. | Max. | Unit |
|-----------|------------------|-------------|------|------|------|------|
| Input | C _{IN1} | | — | — | 8 | |
| BYTE | C _{IN2} | $V_1 = 0 V$ | _ | — | 120 | pF |
| Output | C _{OUT} | $V_0 = 0 V$ | — | _ | 10 | |

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