OKI

ML63187/189B/193

User's Manual

NOTICE: ML63187 is replaced by ML63189B. Order stop for new masks for ML63187

FIRST EDITION
ISSUE DATE: Mar. 2000

FEUL63193-01

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

5. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.

6. The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans. Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.

7. Certain products in this document may need government approval before they can be exported to particular countries. The purchaser assumes the responsibility of determining the legality of export of these products and will take appropriate and necessary steps at their own expense for these.

8. No part of the contents contained herein may be reprinted or reproduced without our prior permission.

9. MS-DOS is a registered trademark of Microsoft Corporation.

Printed in Japan

Preface

This manual describes the hardware of Oki's original CMOS 4-bit microcontrollers ML63187, ML63189B, and ML63193.

Refer to the "nX-4/250 Core Instruction Manual" for details of the 4-bit CPU core nX-4/250 which is built in the ML63187, ML63189B, and ML63193.

The manuals related to the ML63187, ML63189B, and ML63193 are shown below.

- nX-4/250 Core Instruction Manual:
  Describes the base architecture and instruction set of nX-4/250 core.

- SASM63K User's Manual:
  Describes the structured assembler operation and assembler language specification.

- EASE63180 User's Manual:
  Describes the hardware of the emulator.

- DT63K Debugger/DTS63K Simulator User's Manual:
  Describes the debugger commands and the hardware of the simulator.

This document is subject to change without notice.

Notation

Classification	Notation	Description
■ Numeric value	xxh, xxH	Represents a hexadecimal number.
	xxb	Represents a binary number.
■ Unit	word, W	1 word = 16 bits
	byte, B	1 byte = 2 nibbles = 8 bits
	nibble, N	1 nibble = 4 bits
	mega-, M	10^6
	kilo-, K	$2^{10} = 1024$
	kilo-, k	$10^3 = 1000$
	milli-, m	10^{-3}
	micro-, μ	10^{-6}
	nano-, n	10^{-9}
	second, s (lower case)	second
	KB	1 KB = 1 kilobyte = 1024 bytes
	MB	1 MB = 1 megabyte = 2^{20} bytes = 1,048,576 bytes
■ Symbol	⚠ Note:	Gives more information about mistakable items.
	M187	A chapter or page with this symbol describes the ML63187.
	M189B	A chapter or page with this symbol describes the ML63189B.
	M193	A chapter or page with this symbol describes the ML63193.
■ Terminology	"H" level	Indicates high side voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics.
	"L" level	Indicates low side voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.

■ Register description

Invalid bit : When read, a value of "1" is always obtained. Write operations are invalid.
R/W attribute : "R" indicates data can be read and "W" indicates data can be written.

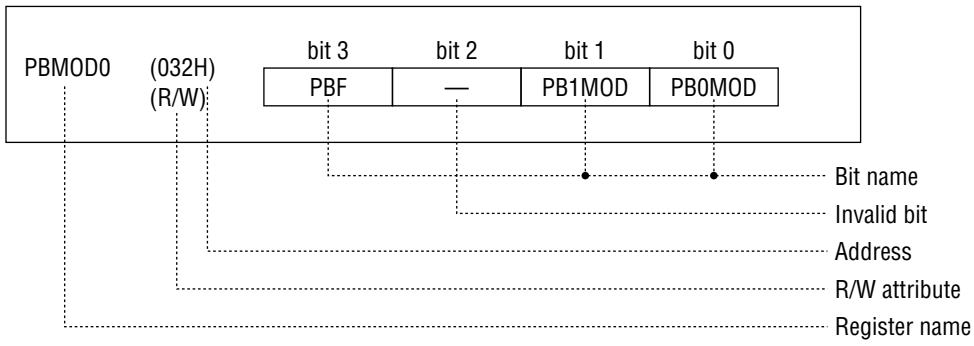


Table of Contents

Chapter 1 Overview

Chapter 2 CPU and Memory Spaces

Chapter 3 CPU Control Functions

Chapter 4 ML63187 Interrupt (INT187)

Chapter 5 ML63189B Interrupt (INT189)

Chapter 6 ML63193 Interrupt (INT193)

Chapter 7 Clock Generator Circuit (OSC)

Chapter 8 Time Base Counter (TBC)

Chapter 9 Timers (TIMER)

Chapter 10 100 Hz Timer Counter (100HzTC)

Chapter 11 Watchdog Timer (WDT)

Chapter 12 Ports (INPUT, I/O PORT)

Chapter 13 Melody Driver (MELODY)

Chapter 14 Serial Port (SIO)

Chapter 15 Shift Register (SFT)

Chapter 16 LCD Driver (LCD)

Chapter 17 Multiplication/Division Circuit (MULDIV)

Chapter 18 Battery Low Detect Circuit (BLD)

Chapter 19 Backup Circuit (BACKUP)

Appendixes

Chapter 1

Overview

Chapter 1 Overview

1.1 Overview

The ML63187, ML63189B, and ML63193 are CMOS 4-bit microcontrollers that guarantee operation at 0.9 V.

With an internal dot matrix LCD driver, these devices are well suited for applications having liquid-crystal display (LCD) such as games, toys, watches, etc.

The ML63187, ML63189B, and ML63193 are masked-ROM devices belonging to the M6318x series of the OLMS-63K family with an internal Oki's original CPU core nX-4/250.

Compared to other products of the M6318x series (MSM63184A), the ML63187 and ML63189B have slimmer functions, more memory capacity and a greater number of LCD drivers. Also, the reference voltage value of the battery low detect circuit has been optimized, and to accommodate requirements for low power consumption, supply current has decreased compared to other devices in the same series.

The ML63193 is a higher-end model over the ML63187 and ML63189B, featuring enlarged memory capacity and additional I/O ports. It also has the multiplication/division circuit and a serial port.

1.2 Features

The ML63187, ML63189B, and ML63193 have the following features.

a. Extensive instruction set
- 408 instructions
  Transfer, rotate, increment/decrement, arithmetic operations, compare, logic operations, mask operations, bit operations, ROM table reference, stack operations, flag operations, jump, conditional branch, call/return, control

b. Wide variety of addressing modes
- Indirect addressing mode for 4 types of data memory with current bank register, extra bank register, HL register and XY register
- Data memory bank internal direct addressing mode

c. Processing speed
- 2 clocks per machine cycle, with most instructions executed in 1 machine cycle
- Minimum instruction execution time: 61 µs (@ 32.768 kHz system clock)
  1 µs (@ 2 MHz system clock)

d. Clock generation circuit
- Low-speed clock:
  Crystal oscillation or RC oscillation selected with mask option (30 kHz to 80 kHz)
- High-speed clock:
  Ceramic oscillation or RC oscillation selected with software (2 MHz max.)

e. Program memory space
- ML63187: 16K words
- ML63189B: 32K words
- ML63193: 64K words
- The basic instruction length is 16 bits per word.

f. Data memory space
- ML63187: 1024 nibbles
- ML63189B: 1536 nibbles
- ML63193: 2048 nibbles

g. Stack level

	Call stack level	Register stack level
ML63187	16	16
ML63189B	16	16
ML63193	16	16

h. Ports
- Input ports:
  Selectable as input with pull-up resistor, input with pull-down resistor or high impedance input.
- I/O ports:
  Selectable as input with pull-up resistor, input with pull-down resistor or high impedance input.
  Selectable as p-channel open drain output, n-channel open drain output, high impedance output or CMOS output.
- Can be interfaced to external devices having different power supplies.
  V_{DDI} is the power supply pin for ports.
- Number of ports:

	Input ports	I/O ports
ML63187	—	2 ports × 4 bits
ML63189B	1 port × 4 bits	4 ports × 4 bits
ML63193	1 port × 4 bits	5 ports × 4 bits

i. Melody output
- Melody frequency: 529 Hz to 2979 Hz
- Tone length: 63 varieties
- Tempo: 15 varieties
- Melody data: Stored in program memory
- Buzzer driver signal output: 4 kHz

j. LCD driver
- Number of segments: 1024 segments max. (64 seg. × 16 com.)
- 1/1 to 1/16 duty
- 1/4 or 1/5 bias (internal regulator)
- Selectable as all-ON mode, all-OFF mode, power down mode, and normal display mode
- Adjustable contrast

k. Multiplication/division circuit
- Multiplication: (8-bit) × (8-bit) = product (16-bit)
- Division: (16-bit) ÷ (8-bit) = quotient (16-bit), remainder (8-bit)

l. System reset function
- System reset by RESET pin (Built-in 2 kHz RESET sampling circuit can be selected by mask option)
- System reset by power-on detection (When not using 2 kHz RESET sampling circuit)
- System reset by detection that low-speed clock has stopped oscillation

m. Battery check

- Function that detects battery low voltage
- Selection of judgment voltage by software (LD1 and LD0 bit settings of BLDCON)

LD1	LD0	Judgment voltage (V)	Comments
0	0	1.05 ±0.10	Ta = 25°C
0	1	1.20 ±0.10	Ta = 25°C
1	0	1.80 ±0.10	Ta = 25°C
1	1	2.40 ±0.10	Ta = 25°C

n. Power supply backup

- Turning on the backup circuit (multiplied voltage circuit) enables operation at the low voltage of 0.9 V.

o. Timers, counters

- 8-bit timer: 4 channels
  Selectable as auto-reload mode, capture mode, clock frequency measurement mode
- Watchdog timer: 1 channel
- 100 Hz timer: 1 channel
  1/100 sec. measurement possible
- 15-bit TBC: 1 channel
  1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz,128 Hz signals can be read

p. Serial port (ML63193 only)

- Mode: UART mode, synchronous mode
- Communication speed in UART mode: 1200 bps, 2400 bps, 4800 bps, 9600 bps
- Clock frequency in synchronous mode: 32.768 kHz (internal clock mode); external clock frequency
- Data length: 5 to 8 bits

q. Shift register

- Shift clock: System clock ×1 or ×1/2, external clock
- Data length: 8 bits

r. Interrupt factors

	External factors	Internal factors
ML63187	2	12
ML63189B	3	12
ML63193	4	14

s. Shipping products

Package	Product
ML63187	
• Chip (111 pads)	ML63187-xxxWA
• 128-pin flat package (128QFP) QFP128-P-1420-0.50-K	ML63187-xxxGA
ML63189B	
• Chip (123 pads)	ML63189B-xxxWA
• 128-pin flat package (128QFP) QFP128-P-1420-0.50-K	ML63189B-xxxGA
ML63193	
• Chip (128 pads)	ML63193-xxxWA
• 144-pin flat package (144LQFP) LQFP144-P-2020-0.50-K	ML63193-xxxTC

xxx indicates the ROM code number.

t. Operating temperature

- –20 to +70°C

u. Power supply voltage

- When using backup: 0.9 V to 2.7 V (30 to 80 kHz operating frequency)
  1.2 V to 2.7 V (500 kHz max. operating frequency)
  1.5 V to 2.7 V (1 MHz max. operating frequency)
- When not using backup: 1.8 V to 5.5 V (2 MHz max. operating frequency)

1.3 Function List

Table 1-1 lists the ML63187, ML63189B, and ML63193 functions. The solid black circles within the chart indicate that the product has the particular function.

Table 1-1 Function List

Function		Symbol	ML63187	ML63189B	ML63193	Reference page
ROM (× 16 bits)		ROM	16352	32736	65504	→2-7
RAM (× 4 bits)		RAM	1024	1536	2048	→2-8
STACK RAM	Call	STACK	16 levels	16 levels	16 levels	→2-5
	Register		16 levels	16 levels	16 levels	→2-6
System reset generation circuit		RST	●	●	●	→3-2
Interrupt	ML63187 interrupt	INT187	●	—	—	→4-1
	ML63189B interrupt	INT189	—	●	—	→5-1
	ML63193 interrupt	INT193	—	—	●	→6-1
Clock generator circuit		OSC	●	●	●	→7-1
Time base counter		TBC	●	●	●	→8-1
Timers		TIMER	●	●	●	→9-1
100 Hz timer counter		100HzTC	●	●	●	→10-1
Watchdog timer		WDT	●	●	●	→11-1
Input port		INPUT PORT	—	1 port × 4 bits	1 port × 4 bits	—
	Port 0	P0	—	●	●	→12-2
I/O port		I/O PORT	2 ports × 4 bits	4 ports × 4 bits	5 ports × 4 bits	—
	Port 9	P9	—	●	●	→12-7
	Port A	PA	—	●	●	
	Port B	PB	●	●	●	→12-12
	Port C	PC	—	—	●	→12-18
	Port E	PE	●	●	●	→12-25
Melody driver		MELODY	●	●	●	→13-1
Serial port		SIO	—	—	●	→14-1
Shift register		SFT	●	●	●	→15-1
LCD driver	COM	LCD	16 lines	16 lines	16 lines	→16-1
	SEG		64 lines	64 lines	64 lines	
Display register (× 4 bits)		DSPR	256	256	256	→16-4
Bias generator		BIAS	●	●	●	→16-6
Multiplication/division circuit		MULDIV	—	—	●	→17-1
Battery low detect circuit		BLD	●	●	●	→18-1
Backup circuit		BACKUP	●	●	●	→19-1

1.4 Block Diagram

Block diagrams of the ML63187, ML63189B, and ML63193 are shown in Figures 1-1, 1-2, and 1-3 respectively.

Asterisks (*) indicate port secondary functions. Signal names enclosed by chain lines (----) indicate interface signals of the V_{DDI} power supply system.

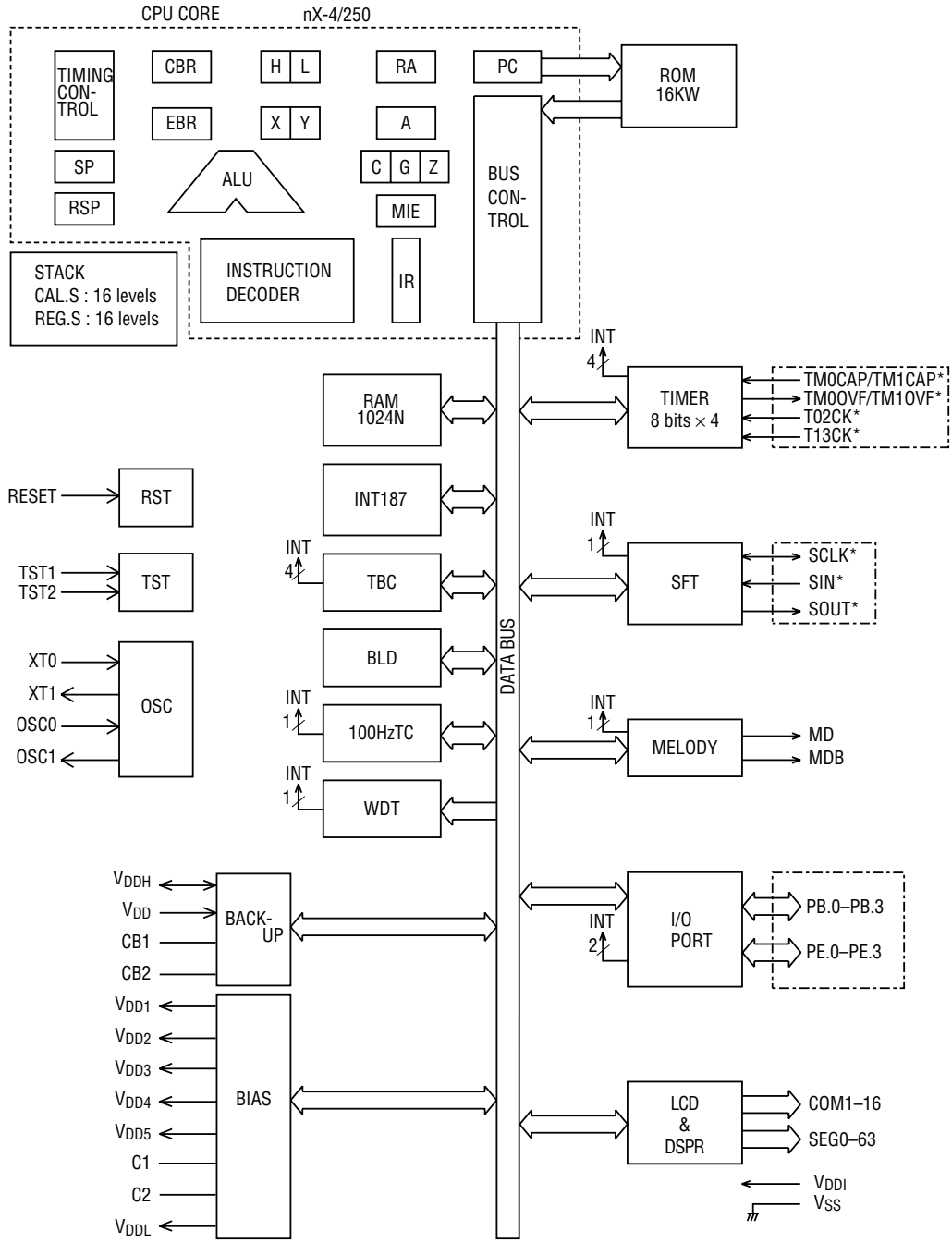


Figure 1-1 ML63187 Block Diagram

Asterisks (*) indicate port secondary functions. Signal names enclosed by chain lines (-·-) indicate interface signals of the V_{DDI} power supply system.

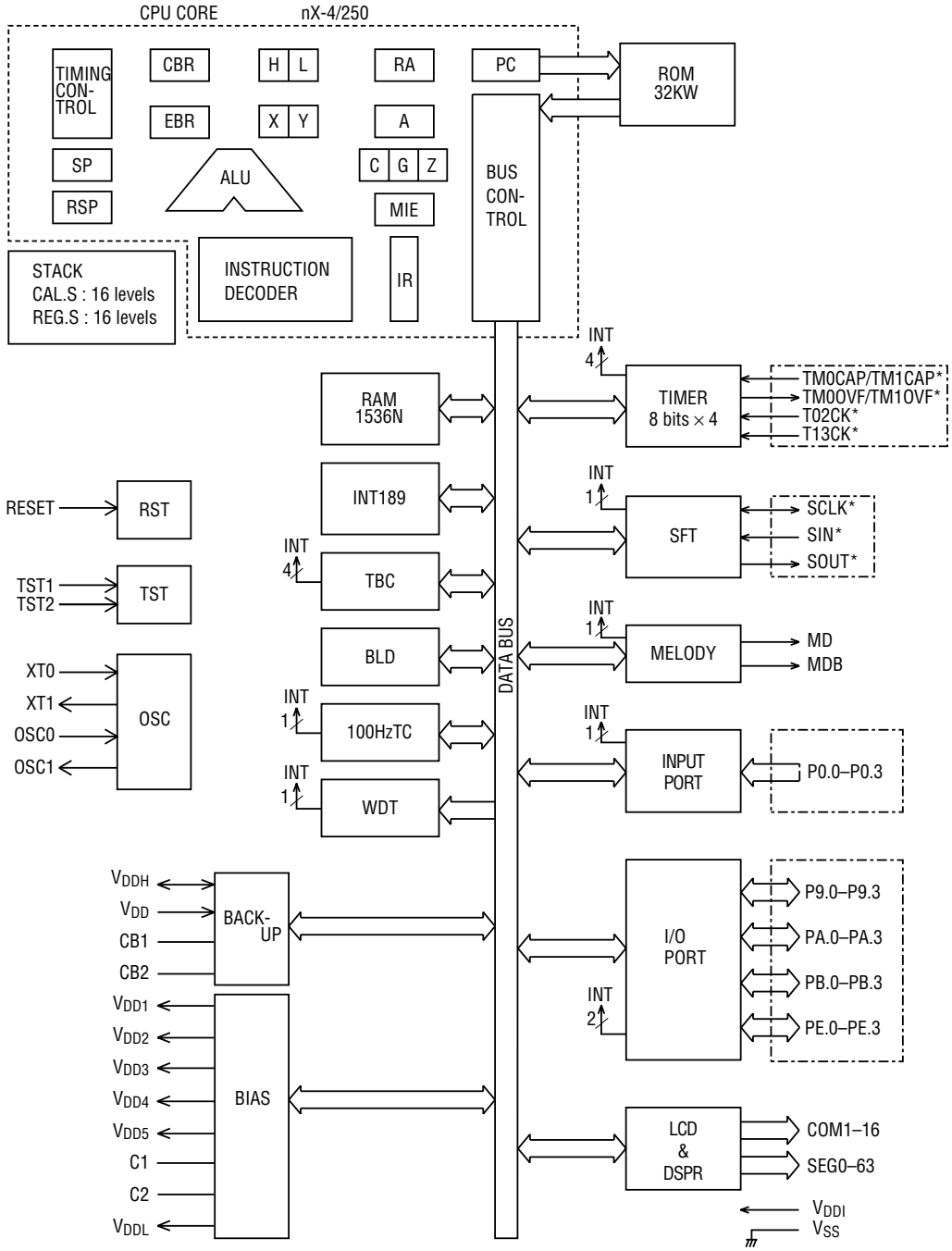


Figure 1-2 ML63189B Block Diagram

Asterisks (*) indicate port secondary functions. Signal names enclosed by chain lines (-·-·-) indicate interface signals of the V_{DDI} power supply system.

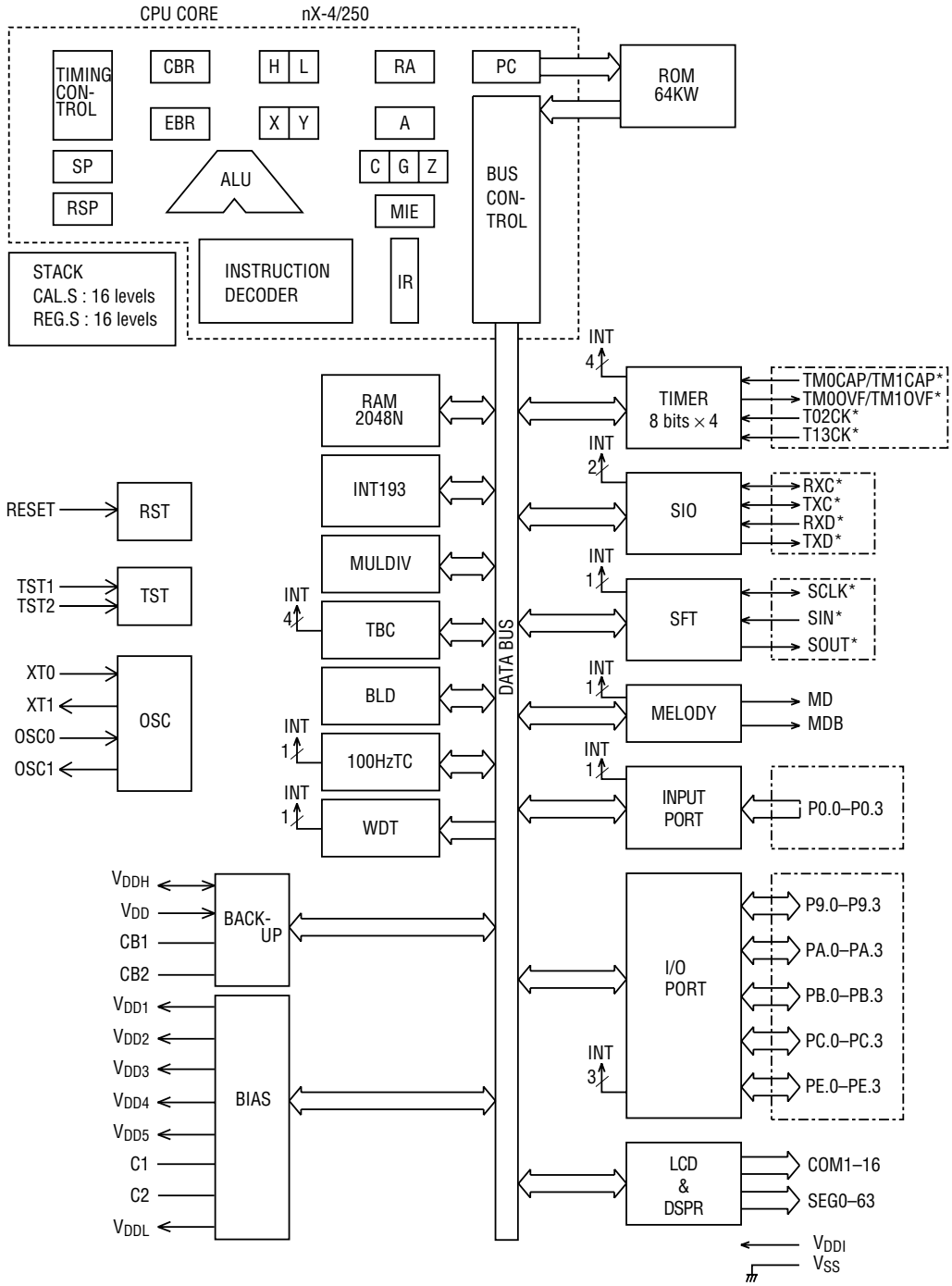


Figure 1-3 ML63193 Block Diagram

1.5 Pin Configuration

1.5.1 ML63187 Pin Configuration

The ML63187 pin configuration, chip pin configuration, and pad coordinates are shown in Figures 1-4, 1-5, and Table 1-2, respectively.

NC (not connected) indicates an unused pin that is left unconnected (open).

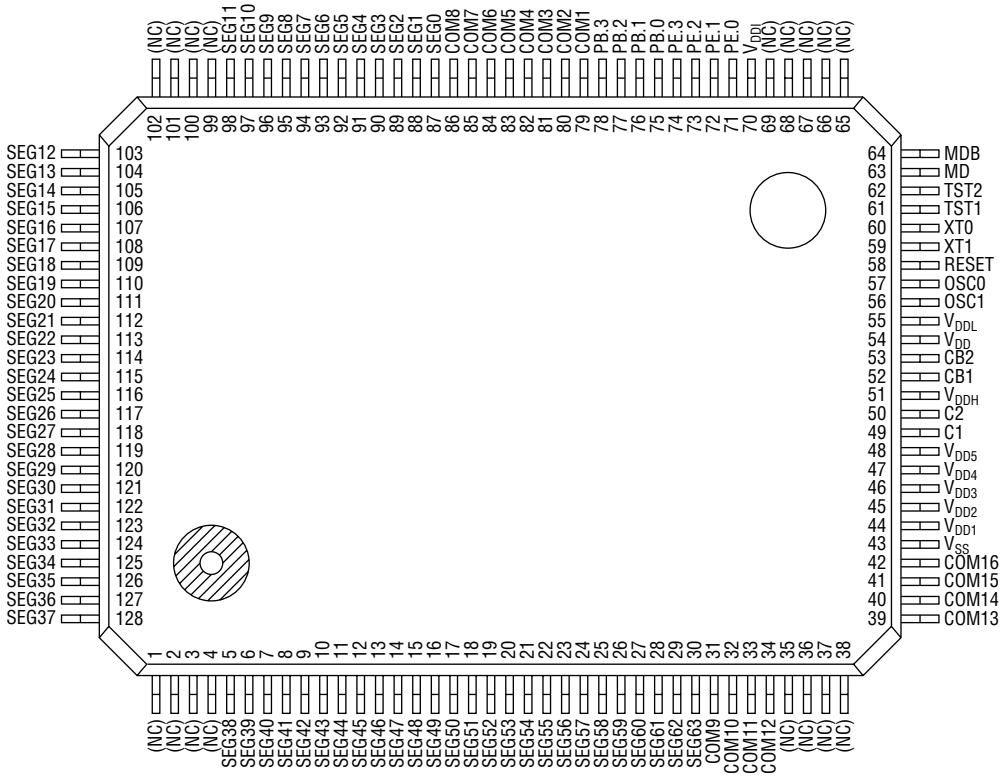
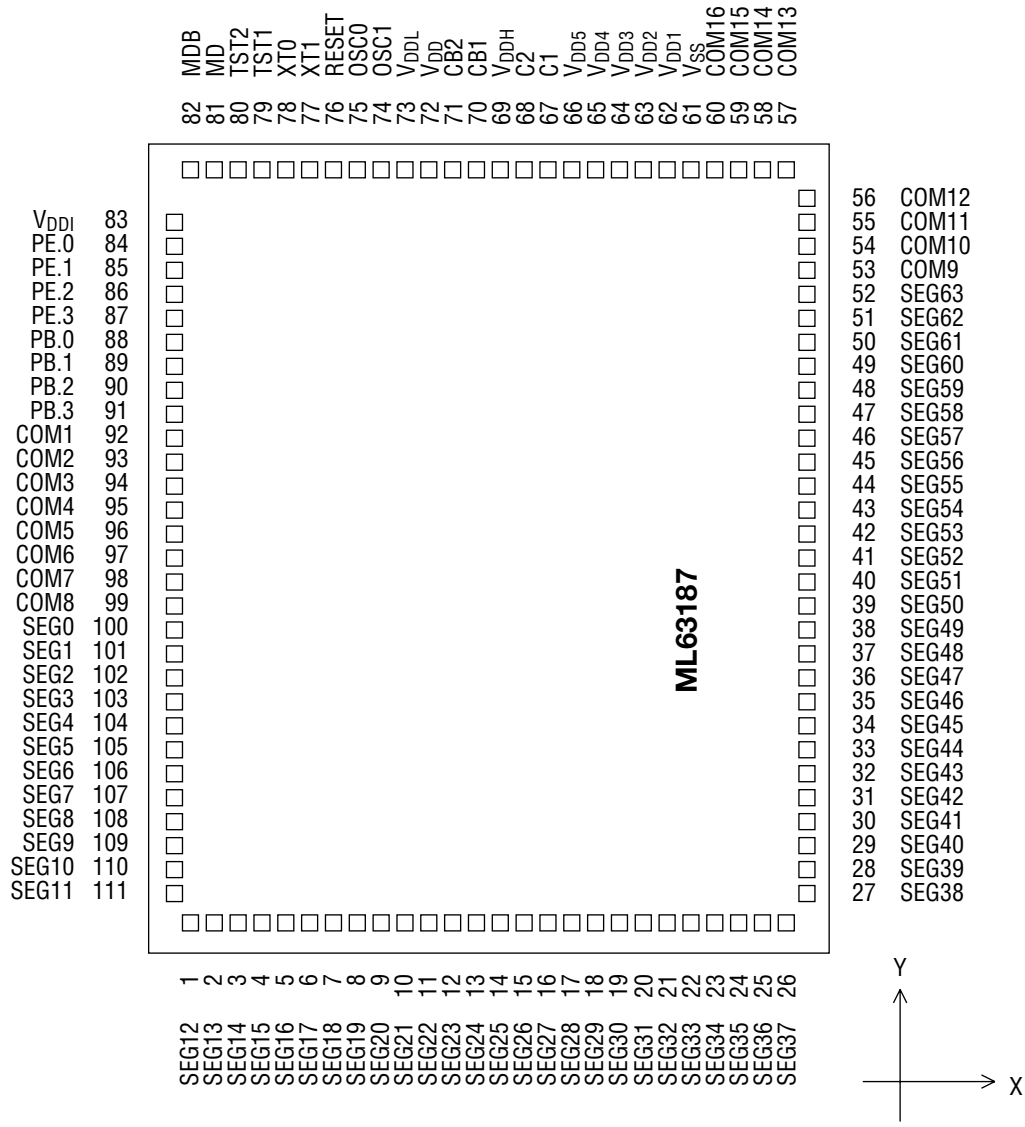


Figure 1-4 ML63187 128-Pin QFP Pin Configuration (Top View)



- Chip size : 4.238 mm × 4.914 mm
- Chip thickness : 350 µm (280 µm: available as required)
- Coordinate origin : center of chip
- Pad hole size : 100 µm × 100 µm
- Pad size : 110 µm × 110 µm
- Minimum pad pitch : 140 µm

Note: The chip substrate voltage is V_{SS}.

Figure 1-5 ML63187 Chip Pin Configuration (Top View)

Table 1-2 ML63187 Pad Coordinates

Center of chip: x = 0, y = 0

Pad No.	Pad name	X (μm)	Y (μm)	Pad No.	Pad name	X (μm)	Y (μm)
1	SEG12	–1755	–2311	41	SEG52	1969	–70
2	SEG13	–1615	–2311	42	SEG53	1969	70
3	SEG14	–1474	–2311	43	SEG54	1969	211
4	SEG15	–1334	–2311	44	SEG55	1969	351
5	SEG16	–1193	–2311	45	SEG56	1969	491
6	SEG17	–1053	–2311	46	SEG57	1969	632
7	SEG18	–913	–2311	47	SEG58	1969	772
8	SEG19	–772	–2311	48	SEG59	1969	913
9	SEG20	–632	–2311	49	SEG60	1969	1053
10	SEG21	–491	–2311	50	SEG61	1969	1193
11	SEG22	–351	–2311	51	SEG62	1969	1334
12	SEG23	–211	–2311	52	SEG63	1969	1474
13	SEG24	–70	–2311	53	COM9	1969	1615
14	SEG25	70	–2311	54	COM10	1969	1755
15	SEG26	211	–2311	55	COM11	1969	1895
16	SEG27	351	–2311	56	COM12	1969	2036
17	SEG28	491	–2311	57	COM13	1755	2311
18	SEG29	632	–2311	58	COM14	1615	2311
19	SEG30	772	–2311	59	COM15	1474	2311
20	SEG31	913	–2311	60	COM16	1334	2311
21	SEG32	1053	–2311	61	V_{SS}	1193	2311
22	SEG33	1193	–2311	62	V_{DD1}	1053	2311
23	SEG34	1334	–2311	63	V_{DD2}	913	2311
24	SEG35	1474	–2311	64	V_{DD3}	772	2311
25	SEG36	1615	–2311	65	V_{DD4}	632	2311
26	SEG37	1755	–2311	66	V_{DD5}	491	2311
27	SEG38	1969	–2036	67	C1	351	2311
28	SEG39	1969	–1895	68	C2	211	2311
29	SEG40	1969	–1755	69	V_{DDH}	70	2311
30	SEG41	1969	–1615	70	CB1	–70	2311
31	SEG42	1969	–1474	71	CB2	–211	2311
32	SEG43	1969	–1334	72	V_{DD}	–351	2311
33	SEG44	1969	–1193	73	V_{DDL}	–491	2311
34	SEG45	1969	–1053	74	OSC1	–632	2311
35	SEG46	1969	–913	75	OSC0	–772	2311
36	SEG47	1969	–772	76	RESET	–913	2311
37	SEG48	1969	–632	77	XT1	–1053	2311
38	SEG49	1969	–491	78	XT0	–1193	2311
39	SEG50	1969	–351	79	TST1	–1334	2311
40	SEG51	1969	–211	80	TST2	–1474	2311

Table 1-2 ML63187 Pad Coordinates (continued)

Center of chip: x = 0, y = 0

Pad No.	Pad name	X (μm)	Y (μm)	Pad No.	Pad name	X (μm)	Y (μm)
81	MD	–1615	2311	97	COM6	–1969	–70
82	MDB	–1755	2311	98	COM7	–1969	–211
83	V_{DDI}	–1969	1895	99	COM8	–1969	–351
84	PE.0	–1969	1755	100	SEG0	–1969	–491
85	PE.1	–1969	1615	101	SEG1	–1969	–632
86	PE.2	–1969	1474	102	SEG2	–1969	–772
87	PE.3	–1969	1334	103	SEG3	–1969	–913
88	PB.0	–1969	1193	104	SEG4	–1969	–1053
89	PB.1	–1969	1053	105	SEG5	–1969	–1193
90	PB.2	–1969	913	106	SEG6	–1969	–1334
91	PB.3	–1969	772	107	SEG7	–1969	–1474
92	COM1	–1969	632	108	SEG8	–1969	–1615
93	COM2	–1969	491	109	SEG9	–1969	–1755
94	COM3	–1969	351	110	SEG10	–1969	–1895
95	COM4	–1969	211	111	SEG11	–1969	–2036
96	COM5	–1969	70				

1.5.2 ML63189B Pin Configuration

The ML63189B pin configuration, chip pin configuration, and pad coordinates are shown in Figures 1-6, 1-7, and Table 1-3, respectively.

NC (not connected) indicates an unused pin that is left unconnected (open).

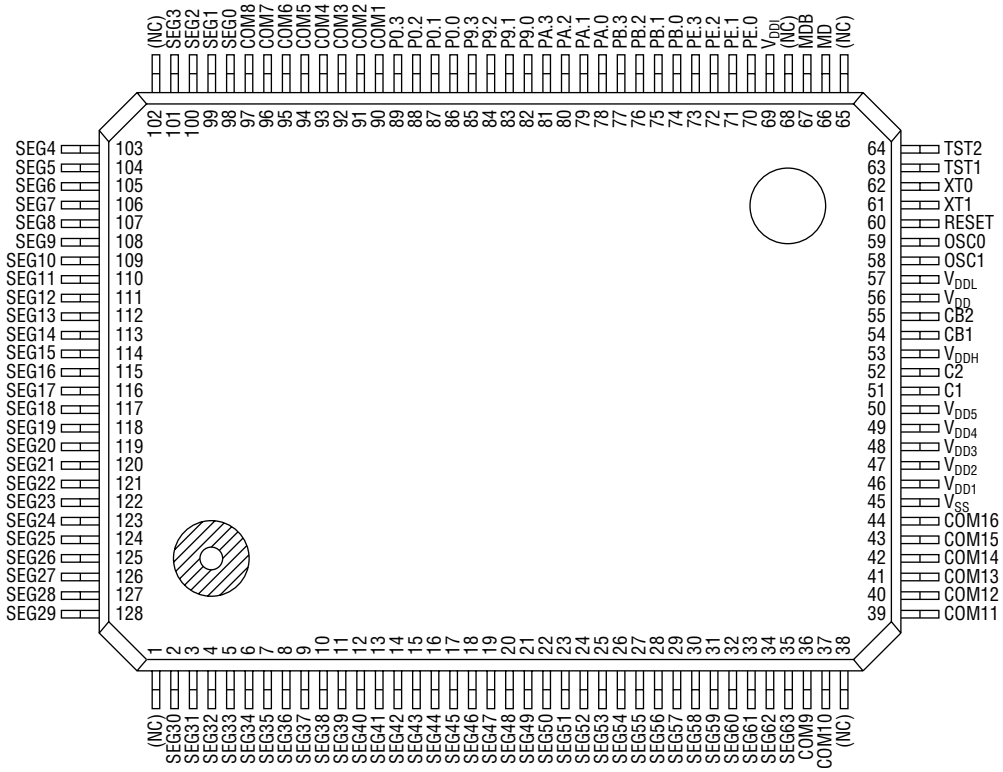
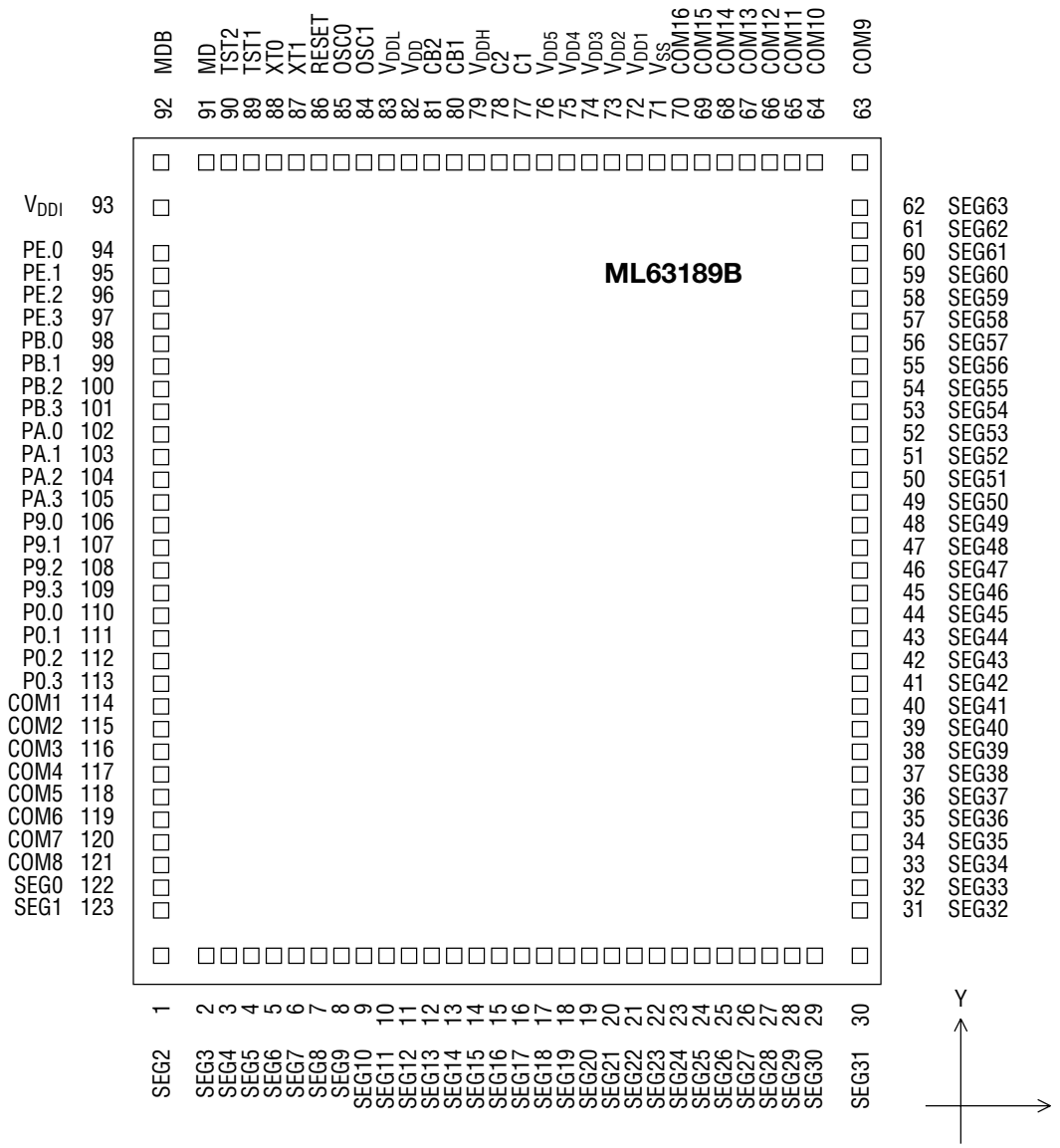


Figure 1-6 ML63189B 128-Pin QFP Pin Configuration (Top View)



- Chip size : 4.81 mm × 5.20 mm
- Chip thickness : 350 µm (280 µm: available as required)
- Coordinate origin : center of chip
- Pad hole size : 100 µm × 100 µm
- Pad size : 110 µm × 110 µm
- Minimum pad pitch : 140 µm

Note: The chip substrate voltage is V_{SS}.

Figure 1-7 ML63189B Chip Pin Configuration (Top View)

Table 1-3 ML63189B Pad Coordinates

Center of chip: x = 0, y = 0

Pad No.	Pad name	X (μm)	Y (μm)	Pad No.	Pad name	X (μm)	Y (μm)
1	SEG2	–2259	–2438	41	SEG42	2259	–772
2	SEG3	–1895	–2438	42	SEG43	2259	–632
3	SEG4	–1755	–2438	43	SEG44	2259	–491
4	SEG5	–1615	–2438	44	SEG45	2259	–351
5	SEG6	–1474	–2438	45	SEG46	2259	–211
6	SEG7	–1334	–2438	46	SEG47	2259	–70
7	SEG8	–1193	–2438	47	SEG48	2259	70
8	SEG9	–1053	–2438	48	SEG49	2259	211
9	SEG10	–913	–2438	49	SEG50	2259	351
10	SEG11	–772	–2438	50	SEG51	2259	491
11	SEG12	–632	–2438	51	SEG52	2259	632
12	SEG13	–491	–2438	52	SEG53	2259	772
13	SEG14	–351	–2438	53	SEG54	2259	913
14	SEG15	–211	–2438	54	SEG55	2259	1053
15	SEG16	–70	–2438	55	SEG56	2259	1193
16	SEG17	70	–2438	56	SEG57	2259	1334
17	SEG18	211	–2438	57	SEG58	2259	1474
18	SEG19	351	–2438	58	SEG59	2259	1615
19	SEG20	491	–2438	59	SEG60	2259	1755
20	SEG21	632	–2438	60	SEG61	2259	1895
21	SEG22	772	–2438	61	SEG62	2259	2036
22	SEG23	913	–2438	62	SEG63	2259	2176
23	SEG24	1053	–2438	63	COM9	2259	2438
24	SEG25	1193	–2438	64	COM10	1895	2438
25	SEG26	1334	–2438	65	COM11	1755	2438
26	SEG27	1474	–2438	66	COM12	1615	2438
27	SEG28	1615	–2438	67	COM13	1474	2438
28	SEG29	1755	–2438	68	COM14	1334	2438
29	SEG30	1895	–2438	69	COM15	1193	2438
30	SEG31	2259	–2438	70	COM16	1053	2438
31	SEG32	2259	–2176	71	V_{SS}	913	2438
32	SEG33	2259	–2036	72	V_{DD1}	772	2438
33	SEG34	2259	–1895	73	V_{DD2}	632	2438
34	SEG35	2259	–1755	74	V_{DD3}	491	2438
35	SEG36	2259	–1615	75	V_{DD4}	351	2438
36	SEG37	2259	–1474	76	V_{DD5}	211	2438
37	SEG38	2259	–1334	77	C1	70	2438
38	SEG39	2259	–1193	78	C2	–70	2438
39	SEG40	2259	–1053	79	V_{DDH}	–211	2438
40	SEG41	2259	–913	80	CB1	–351	2438

Table 1-3 ML63189B Pad Coordinates (continued)

Center of chip: x = 0, y = 0

Pad No.	Pad name	X (μm)	Y (μm)	Pad No.	Pad name	X (μm)	Y (μm)
81	CB2	–491	2438	103	PA.1	–2259	632
82	V_{DD}	–632	2438	104	PA.2	–2259	491
83	V_{DDL}	–772	2438	105	PA.3	–2259	351
84	OSC1	–913	2438	106	P9.0	–2259	211
85	OSC0	–1053	2438	107	P9.1	–2259	70
86	RESET	–1193	2438	108	P9.2	–2259	–70
87	XT1	–1334	2438	109	P9.3	–2259	–211
88	XT0	–1474	2438	110	P0.0	–2259	–351
89	TST1	–1615	2438	111	P0.1	–2259	–491
90	TST2	–1755	2438	112	P0.2	–2259	–632
91	MD	–1895	2438	113	P0.3	–2259	–772
92	MDB	–2259	2438	114	COM1	–2259	–913
93	V_{DDI}	–2259	2132	115	COM2	–2259	–1053
94	PE.0	–2259	1895	116	COM3	–2259	–1193
95	PE.1	–2259	1755	117	COM4	–2259	–1334
96	PE.2	–2259	1615	118	COM5	–2259	–1474
97	PE.3	–2259	1474	119	COM6	–2259	–1615
98	PB.0	–2259	1334	120	COM7	–2259	–1755
99	PB.1	–2259	1193	121	COM8	–2259	–1895
100	PB.2	–2259	1053	122	SEG0	–2259	–2036
101	PB.3	–2259	913	123	SEG1	–2259	–2176
102	PA.0	–2259	772				

1.5.3 ML63193 Pin Configuration

The ML63193 pin configuration, chip pin configuration, and pad coordinates are shown in Figures 1-8, 1-9, and Table 1-4, respectively.

NC (not connected) indicates an unused pin that is left unconnected (open).

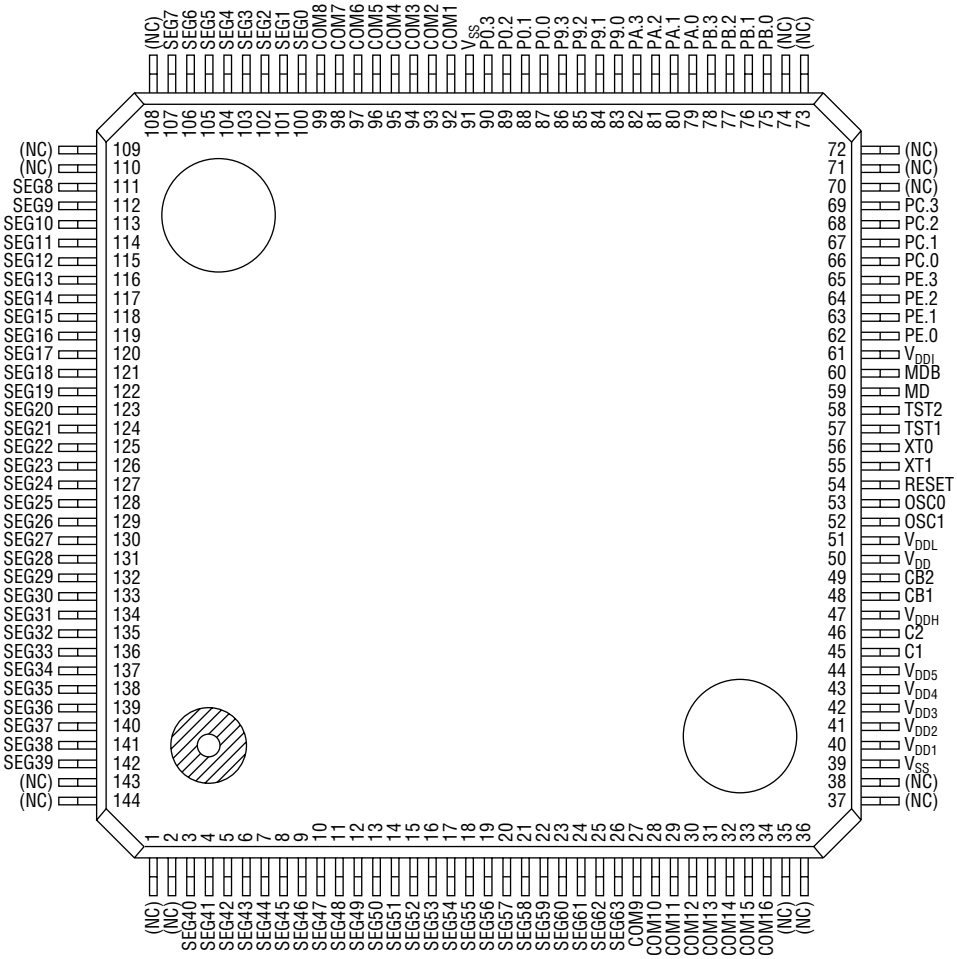
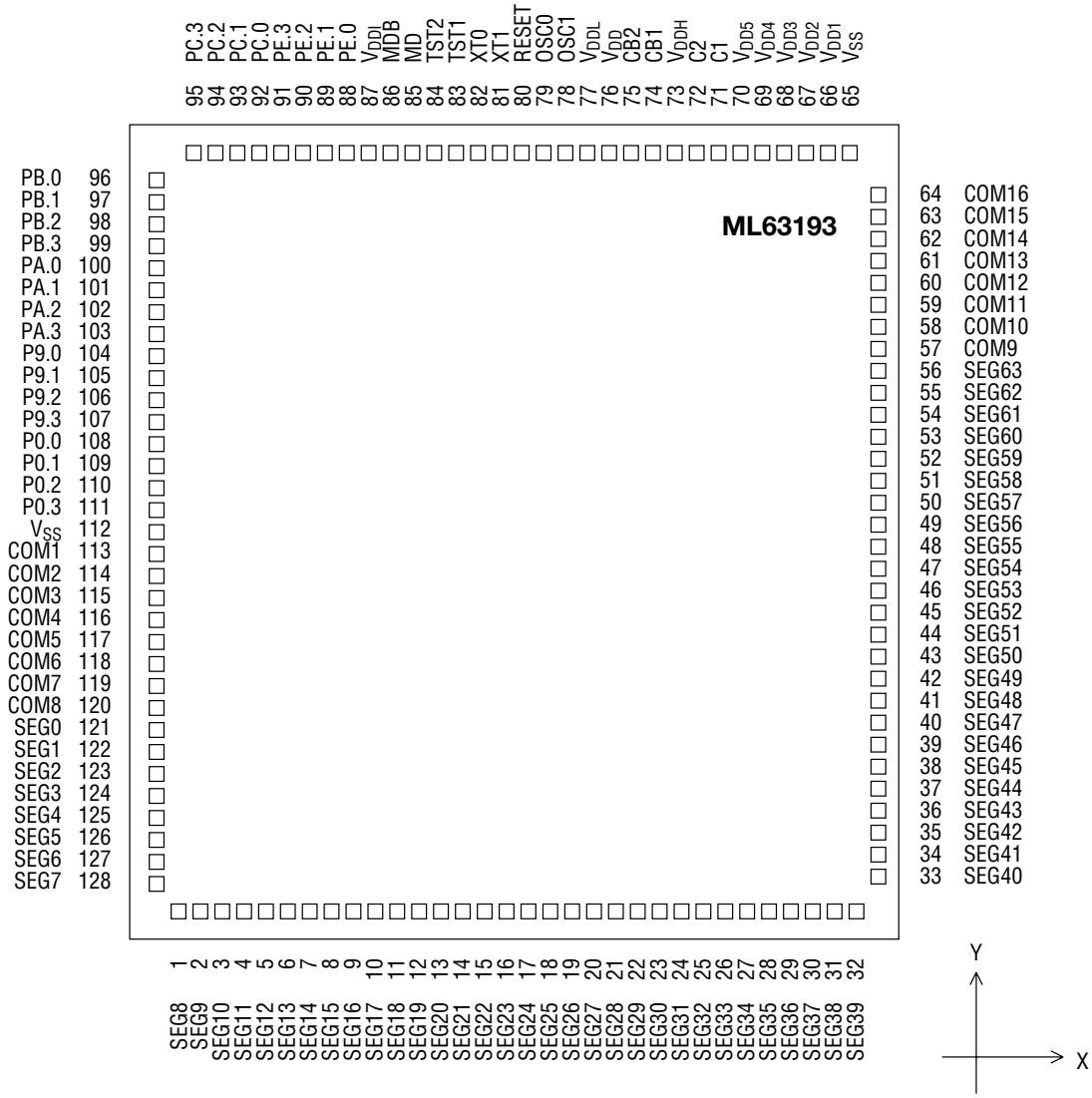


Figure 1-8 ML63193 144-Pin LQFP Pin Configuration (Top View)



- Chip size : 5.72 mm × 5.72 mm
- Chip thickness : 350 µm (280 µm: available as required)
- Coordinate origin : center of chip
- Pad hole size : 100 µm × 100 µm
- Pad size : 110 µm × 110 µm
- Minimum pad pitch : 140 µm

Note: The chip substrate voltage is V_{SS}.

Figure 1-9 ML63193 Chip Pin Configuration (Top View)

Table 1-4 ML63193 Pad Coordinates

Center of chip: x = 0, y = 0

Pad No.	Pad name	X (μm)	Y (μm)	Pad No.	Pad name	X (μm)	Y (μm)
1	SEG8	–2204	–2714	41	SEG48	2714	–1025
2	SEG9	–2063	–2714	42	SEG49	2714	–885
3	SEG10	–1923	–2714	43	SEG50	2714	–745
4	SEG11	–1783	–2714	44	SEG51	2714	–604
5	SEG12	–1642	–2714	45	SEG52	2714	–464
6	SEG13	–1502	–2714	46	SEG53	2714	–323
7	SEG14	–1361	–2714	47	SEG54	2714	–183
8	SEG15	–1221	–2714	48	SEG55	2714	–43
9	SEG16	–1081	–2714	49	SEG56	2714	98
10	SEG17	–940	–2714	50	SEG57	2714	238
11	SEG18	–800	–2714	51	SEG58	2714	379
12	SEG19	–659	–2714	52	SEG59	2714	519
13	SEG20	–519	–2714	53	SEG60	2714	659
14	SEG21	–379	–2714	54	SEG61	2714	800
15	SEG22	–238	–2714	55	SEG62	2714	940
16	SEG23	–98	–2714	56	SEG63	2714	1081
17	SEG24	43	–2714	57	COM9	2714	1221
18	SEG25	183	–2714	58	COM10	2714	1361
19	SEG26	323	–2714	59	COM11	2714	1502
20	SEG27	464	–2714	60	COM12	2714	1642
21	SEG28	604	–2714	61	COM13	2714	1783
22	SEG29	745	–2714	62	COM14	2714	1923
23	SEG30	885	–2714	63	COM15	2714	2063
24	SEG31	1025	–2714	64	COM16	2714	2204
25	SEG32	1166	–2714	65	V_{SS}	2152	2714
26	SEG33	1306	–2714	66	V_{DD1}	2011	2714
27	SEG34	1447	–2714	67	V_{DD2}	1871	2714
28	SEG35	1587	–2714	68	V_{DD3}	1730	2714
29	SEG36	1727	–2714	69	V_{DD4}	1590	2714
30	SEG37	1868	–2714	70	V_{DD5}	1450	2714
31	SEG38	2008	–2714	71	C1	1309	2714
32	SEG39	2149	–2714	72	C2	1169	2714
33	SEG40	2714	–2149	73	V_{DDH}	1028	2714
34	SEG41	2714	–2008	74	CB1	888	2714
35	SEG42	2714	–1868	75	CB2	748	2714
36	SEG43	2714	–1727	76	V_{DD}	607	2714
37	SEG44	2714	–1587	77	V_{DDL}	467	2714
38	SEG45	2714	–1447	78	OSC1	326	2714
39	SEG46	2714	–1306	79	OSC0	186	2714
40	SEG47	2714	–1166	80	RESET	46	2714

Table 1-4 ML63193 Pad Coordinates (continued)

Center of chip: x = 0, y = 0

Pad No.	Pad name	X (μm)	Y (μm)	Pad No.	Pad name	X (μm)	Y (μm)
81	XT1	–95	2714	105	P9.1	–2714	983
82	XT0	–235	2714	106	P9.2	–2714	842
83	TST1	–376	2714	107	P9.3	–2714	702
84	TST2	–516	2714	108	P0.0	–2714	562
85	MD	–656	2714	109	P0.1	–2714	421
86	MDB	–797	2714	110	P0.2	–2714	281
87	V_{DDI}	–937	2714	111	P0.3	–2714	140
88	PE.0	–1078	2714	112	V_{SS}	–2714	0
89	PE.1	–1218	2714	113	COM1	–2714	–140
90	PE.2	–1358	2714	114	COM2	–2714	–281
91	PE.3	–1499	2714	115	COM3	–2714	–421
92	PC.0	–1639	2714	116	COM4	–2714	–562
93	PC.1	–1780	2714	117	COM5	–2714	–702
94	PC.2	–1920	2714	118	COM6	–2714	–842
95	PC.3	–2060	2714	119	COM7	–2714	–983
96	PB.0	–2714	2246	120	COM8	–2714	–1123
97	PB.1	–2714	2106	121	SEG0	–2714	–1264
98	PB.2	–2714	1966	122	SEG1	–2714	–1404
99	PB.3	–2714	1825	123	SEG2	–2714	–1544
100	PA.0	–2714	1685	124	SEG3	–2714	–1685
101	PA.1	–2714	1544	125	SEG4	–2714	–1825
102	PA.2	–2714	1404	126	SEG5	–2714	–1966
103	PA.3	–2714	1264	127	SEG6	–2714	–2106
104	P9.0	–2714	1123	128	SEG7	–2714	–2246

1.6 Pin Descriptions

1.6.1 Descriptions of the Basic Functions of Each Pin

The basic functions of each pin of the ML63187, ML63189B, and ML63193 are listed in Table 1-5. Use of a slash ("/") in a pin name indicates that the pin has a secondary function. Refer to section 1.6.2, "Descriptions of the Secondary Functions of Each Pin."

In the I/O column, "—" indicates a power supply pin, "I" indicates an input pin, "O" indicates an output pin, and "I/O" indicates an input/output pin.

Table 1-5 Pin Description (Basic Functions)

Classification	Pin name	ML63187		ML63189B		ML63193		I/O	Function
		Pin	Pad	Pin	Pad	Pin	Pad		
Power Supply	V_{DD}	54	72	56	82	50	76	—	Positive power supply pin
	V_{SS}	43	61	45	71	39 91	65 112	—	Negative power supply pin
	V_{DD1}	44	62	46	72	40	66	—	Power supply pins for LCD bias (internally generated): Connect capacitors (0.1 µF) between these pins and V_{SS}.
	V_{DD2}	45	63	47	73	41	67		
	V_{DD3}	46	64	48	74	42	68		
	V_{DD4}	47	65	49	75	43	69		
	V_{DD5}	48	66	50	76	44	70		
	C1	49	67	51	77	45	71	—	Capacitor connection pins for LCD bias generation: Connect a capacitor (0.1 µF) between C1 and C2.
	C2	50	68	52	78	46	72		
	V_{DDI}	70	83	69	93	61	87	—	Positive power supply pin for external interface (Power supply for input and I/O ports)
	V_{DDL}	55	73	57	83	51	77	—	Positive power supply pin for internal logic (internally generated): Connect a capacitor (0.1 µF) between pin and V_{SS}.
	V_{DDH}	51	69	53	79	47	73	—	Multiplied power supply pin for power supply backup (internally generated): Connect a capacitor (1.0 µF) between pin and V_{SS}.
	CB1	52	70	54	80	48	74	—	Capacitor connection pins for multiplied power supply: Connect a capacitor (1.0 µF) between CB1 and CB2.
	CB2	53	71	55	81	49	75		
Oscillator	XT0	60	78	62	88	56	82	I	Low-speed clock oscillation pins: Crystal oscillation or RC oscillation is selected by the mask option. • If crystal oscillation is selected, connect a crystal between XT0 and XT1, and connect capacitor (C_G) between XT0 and V_{SS}. • If RC oscillation is selected, connect external oscillation resistor (R_{OSL}) between XT0 and XT1.
	XT1	59	77	61	87	55	81	O	
	OSC0	57	75	59	85	53	79	I	High-speed clock oscillation pins: Connect a ceramic resonator and capacitors (C_{L0}, C_{L1}) or external oscillation resistor (R_{OSH}) to these pins.
	OSC1	56	74	58	84	52	78	O	

Table 1-5 Pin Description (Basic Functions) (continued)

Classification	Pin name	ML63187		ML63189B		ML63193		I/O	Function
		Pin	Pad	Pin	Pad	Pin	Pad		
Test	TST1	61	79	63	89	57	83	I	Input pins for testing: Pull-down resistors are built-in.
	TST2	62	80	64	90	58	84		
Reset	RESET	58	76	60	86	54	80	I	Reset input pin: Setting this pin to a "H" level causes internal circuitry settings and values to be initialized. Next, if this pin is set to a "L" level, the execution of instructions will begin from address 0000H. A pull-down resistor is built-in. An option of using RESET sampling circuit or not is chosen by the mask option. When using RESET sampling circuit, the system reset mode is entered by holding the RESET pin at a "H" level for 1 ms or more.
Melody	MD	63	81	66	91	59	85	O	Melody output pin (positive phase)
	MDB	64	82	67	92	60	86	O	Melody output pin (reversed phase)
Port	P0.0/INT5	—	—	86	110	87	108	I	4-bit input port: Each bit can be selected as the following. • Input with pull-up resistor • Input with pull-down resistor • High-impedance input
	P0.1/INT5			87	111	88	109		
	P0.2/INT5			88	112	89	110		
	P0.3/INT5			89	113	90	111		
	P9.0	—	—	82	106	83	104	I/O	4-bit I/O port: During the input mode, each bit can be selected as the following. • Input with pull-up resistor • Input with pull-down resistor • High-impedance input During the output mode, each bit can be selected as the following. • P-channel open drain output • N-channel open drain output • CMOS output • High-impedance output
	P9.1			83	107	84	105		
	P9.2			84	108	85	106		
	P9.3			85	109	86	107		

Table 1-5 Pin Description (Basic Functions) (continued)

Classification	Pin name	ML63187		ML63189B		ML63193		I/O	Function
		Pin	Pad	Pin	Pad	Pin	Pad		
Port	PA.0	—	—	78	102	79	100	I/O	4-bit I/O port: During the input mode, each bit can be selected as the following. • Input with pull-up resistor • Input with pull-down resistor • High-impedance input During the output mode, each bit can be selected as the following. • P-channel open drain output • N-channel open drain output • CMOS output • High-impedance output
	PA.1			79	103	80	101		
	PA.2			80	104	81	102		
	PA.3			81	105	82	103		
	PB.0/INT0/ TM0CAP/ TM00VF/	75	88	74	98	75	96	I/O	4-bit I/O port: During the input mode, each bit can be selected as the following. • Input with pull-up resistor • Input with pull-down resistor • High-impedance input During the output mode, each bit can be selected as the following. • P-channel open drain output • N-channel open drain output • CMOS output • High-impedance output
	PB.1/INT0/ TM1CAP/ TM10VF	76	89	75	99	76	97		
	PB.2/INT0/ T02CK	77	90	76	100	77	98		
	PB.3/INT0/ T13CK	78	91	77	101	78	99		
	PC.0/INT1/ RXD	—	—	—	—	66	92	I/O	4-bit I/O port: During the input mode, each bit can be selected as the following. • Input with pull-up resistor • Input with pull-down resistor • High-impedance input During the output mode, each bit can be selected as the following. • P-channel open drain output • N-channel open drain output • CMOS output • High-impedance output
	PC.1/INT1/ TXC					67	93		
	PC.2/INT1/ RXC					68	94		
	PC.3/INT1/ TXD					69	95		
	PE.0/SIN	71	84	70	94	62	88	I/O	4-bit I/O port: During the input mode, each bit can be selected as the following. • Input with pull-up resistor • Input with pull-down resistor • High-impedance input During the output mode, each bit can be selected as the following. • P-channel open drain output • N-channel open drain output • CMOS output • High-impedance output
	PE.1/SOUT	72	85	71	95	63	89		
	PE.2/SCLK	73	86	72	96	64	90		
	PE.3/INT2	74	87	73	97	65	91		

Table 1-5 Pin Description (Basic Functions) (continued)

Classification	Pin name	ML63187		ML63189B		ML63193		I/O	Function
		Pin	Pad	Pin	Pad	Pin	Pad		
LCD	COM1	79	92	90	114	92	113	O	LCD common signal output pins (COM1 to COM16)
	COM2	80	93	91	115	93	114		
	COM3	81	94	92	116	94	115		
	COM4	82	95	93	117	95	116		
	COM5	83	96	94	118	96	117		
	COM6	84	97	95	119	97	118		
	COM7	85	98	96	120	98	119		
	COM8	86	99	97	121	99	120		
	COM9	31	53	36	63	27	57		
	COM10	32	54	37	64	28	58		
	COM11	33	55	39	65	29	59		
	COM12	34	56	40	66	30	60		
	COM13	39	57	41	67	31	61		
	COM14	40	58	42	68	32	62		
	COM15	41	59	43	69	33	63		
	COM16	42	60	44	70	34	64		
	SEG0	87	100	98	122	100	121	O	LCD segment signal output pins (SEG0 to SEG26)
	SEG1	88	101	99	123	101	122		
	SEG2	89	102	100	1	102	123		
	SEG3	90	103	101	2	103	124		
	SEG4	91	104	103	3	104	125		
	SEG5	92	105	104	4	105	126		
	SEG6	93	106	105	5	106	127		
	SEG7	94	107	106	6	107	128		
	SEG8	95	108	107	7	111	1		
	SEG9	96	109	108	8	112	2		
	SEG10	97	110	109	9	113	3		
	SEG11	98	111	110	10	114	4		
	SEG12	103	1	111	11	115	5		
	SEG13	104	2	112	12	116	6		
	SEG14	105	3	113	13	117	7		
	SEG15	106	4	114	14	118	8		
	SEG16	107	5	115	15	119	9		
	SEG17	108	6	116	16	120	10		
	SEG18	109	7	117	17	121	11		
	SEG19	110	8	118	18	122	12		
	SEG20	111	9	119	19	123	13		
	SEG21	112	10	120	20	124	14		
	SEG22	113	11	121	21	125	15		
	SEG23	114	12	122	22	126	16		
	SEG24	115	13	123	23	127	17		
	SEG25	116	14	124	24	128	18		
	SEG26	117	15	125	25	129	19		

Table 1-5 Pin Description (Basic Functions) (continued)

Classification	Pin name	ML63187		ML63189B		ML63193		I/O	Function
		Pin	Pad	Pin	Pad	Pin	Pad		
LCD	SEG27	118	16	126	26	130	20	O	LCD segment signal output pins (SEG27 to SEG63)
	SEG28	119	17	127	27	131	21		
	SEG29	120	18	128	28	132	22		
	SEG30	121	19	2	29	133	23		
	SEG31	122	20	3	30	134	24		
	SEG32	123	21	4	31	135	25		
	SEG33	124	22	5	32	136	26		
	SEG34	125	23	6	33	137	27		
	SEG35	126	24	7	34	138	28		
	SEG36	127	25	8	35	139	29		
	SEG37	128	26	9	36	140	30		
	SEG38	5	27	10	37	141	31		
	SEG39	6	28	11	38	142	32		
	SEG40	7	29	12	39	3	33		
	SEG41	8	30	13	40	4	34		
	SEG42	9	31	14	41	5	35		
	SEG43	10	32	15	42	6	36		
	SEG44	11	33	16	43	7	37		
	SEG45	12	34	17	44	8	38		
	SEG46	13	35	18	45	9	39		
	SEG47	14	36	19	46	10	40		
	SEG48	15	37	20	47	11	41		
	SEG49	16	38	21	48	12	42		
	SEG50	17	39	22	49	13	43		
	SEG51	18	40	23	50	14	44		
	SEG52	19	41	24	51	15	45		
	SEG53	20	42	25	52	16	46		
	SEG54	21	43	26	53	17	47		
	SEG55	22	44	27	54	18	48		
	SEG56	23	45	28	55	19	49		
	SEG57	24	46	29	56	20	50		
	SEG58	25	47	30	57	21	51		
	SEG59	26	48	31	58	22	52		
	SEG60	27	49	32	59	23	53		
	SEG61	28	50	33	60	24	54		
	SEG62	29	51	34	61	25	55		
	SEG63	30	52	35	62	26	56		

1.6.2 Descriptions of the Secondary Functions of Each Pin

The secondary functions of each pin of the ML63187, ML63189B, and ML63193 are listed in Table 1-6.

Table 1-6 Pin Description (Secondary Functions)

Classification	Pin name	ML63187		ML63189B		ML63193		I/O	Function
		Pin	Pad	Pin	Pad	Pin	Pad		
External interrupt	PB.0/INT0	75	88	74	98	75	96	I	External interrupt 0 input pins: Changes in the input signal level cause interrupts to be generated. Interrupts can be enabled or disabled for each bit by the port B interrupt enable register (PBIE).
	PB.1/INT0	76	89	75	99	76	97		
	PB.2/INT0	77	90	76	100	77	98		
	PB.3/INT0	78	91	77	101	78	99		
	PC.0/INT1	—	—	—	—	66	92	I	External interrupt 1 input pins: Changes in the input signal level cause interrupts to be generated. Interrupts can be enabled or disabled for each bit by the port C interrupt enable register (PCIE).
	PC.1/INT1					67	93		
	PC.2/INT1					68	94		
	PC.3/INT1					69	95		
	PE.3/INT2	74	87	73	97	65	91	I	External interrupt 2 input pin: Changes in the input signal level cause interrupts to be generated.
	P0.0/INT5	—	—	86	110	87	108	I	External interrupt 5 input pins: Changes in the input signal level cause interrupts to be generated. Interrupts can be enabled or disabled for each bit by the port 0 interrupt enable register (P0IE).
	P0.1/INT5			87	111	88	109		
	P0.2/INT5			88	112	89	110		
	P0.3/INT5			89	113	90	111		
Capture	PB.0/TM0CAP	75	88	74	98	75	96	I	Timer 0 capture trigger input pin
	PB.1/TM1CAP	76	89	75	99	76	97	I	Timer 1 capture trigger input pin
Timer	PB.0/TM0OVF	75	88	74	98	75	96	O	Timer 0 overflow flag output pin
	PB.1/TM1OVF	76	89	75	99	76	97	O	Timer 1 overflow flag output pin
	PB.2/T02CK	77	90	76	100	77	98	I	Timer 0, timer 2 external clock input pin
	PB.3/T13CK	78	91	77	101	78	99	I	Timer 1, timer 3 external clock input pin

Table 1-6 Pin Description (Secondary Functions) (continued)

Classification	Pin name	ML63187		ML63189B		ML63193		I/O	Function
		Pin	Pad	Pin	Pad	Pin	Pad		
Serial port	PC.0/RXD	—	—	—	—	66	92	I	Serial port receive data input pin
	PC.1/TXC					67	93	I/O	Synchronous serial port clock input/output pin: This pin should be configured as the clock output for transmit when this device is used as the master processor, or as the clock input for transmit when used as a slave.
	PC.2/RXC					68	94	I/O	Synchronous serial port clock input/output pin: This pin should be configured as the clock output for receive when this device is used as the master processor, or as the clock input for receive when used as a slave.
	PC.3/TXD					69	95	O	Serial port transmit data output pin
Shift register	PE.0/SIN	71	84	70	94	62	88	I	Shift register receive data input pin
	PE.1/SOUT	72	85	71	95	63	89	O	Shift register transmit data output pin
	PE.2/SCLK	73	86	72	96	64	90	I/O	Shift register clock input/output pin: This pin should be configured as the clock output when this device is used as the master processor, or as the clock input when used as a slave.

1.6.3 Handling of Unused Pins

Table 1-7 shows how unused pins should be handled.

Table 1-7 Handling of Unused Pins

Pin	Recommended pin handling
OSC0, OSC1	Open
CB1, CB2	Open
C1, C2	Open
V_{DD1}, V_{DD3}, V_{DD4}, V_{DD5}	Open
TST1, TST2	Open or connect to V_{SS}
P0.0–P0.3	Open
P9.0–P9.3	Open
PA.0–PA.3	Open
PB.0–PB.3	Open
PC.0–PC.3	Open
PE.0–PE.3	Open
MD, MDB	Open
COM1–COM16	Open
SEG0–SEG63	Open

Notes:

1. If a pin set as a high impedance input is left unconnected, the supply current may become excessive. Therefore, it is recommended that unused input ports and input/output ports be set as inputs with either a pull-down or pull-up resistor.
2. When test pins TST1 and TST2 are left unconnected, malfunction may result if there is a large amount of external noise. Therefore, it is recommended to permanently connect TST1 and TST2 to V_{SS}.
3. Connect a capacitor (0.1 µF) between the V_{DD2} pin and the V_{SS} pin when the LCD drivers are not used.

1.7 Basic Timing

1.7.1 Basic Timing of CPU Operation

The low-speed oscillation clock from the XT0/XT1 pins or the high-speed oscillation clock from the OSC0/OSC1 pins are used without frequency division as the system clock (CLK). The system clock signal is in phase with the signal from the XT1 pin or the OSC1 pin.

As shown in Figure 1-10, a single machine cycle is composed of two states, S1 and S2. One state is the interval from a falling edge of CLK to the falling edge of the next CLK.

Instructions are processed in machine cycle units and each instruction is executed in 1 to 3 machine cycles. Instructions are classified according to the number of machine cycles: 1 machine cycle instructions (M1), 2 machine cycle instructions (M1 + M2), and 3 machine cycle instructions (M1 + M2 + M3).

Most instructions are executed in 1 machine cycle.

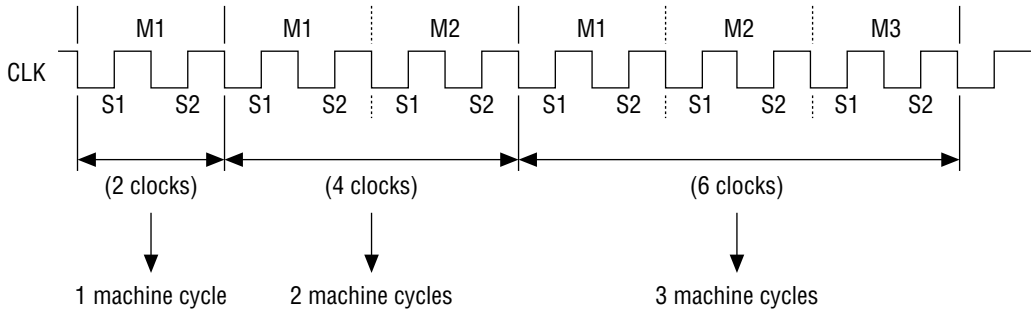


Figure 1-10 Clock Configuration of Each Machine Cycle

1.7.2 Port I/O Basic Timing

Figure 1-11 shows the basic I/O timing.

During the execution of an instruction that outputs data to a port, setting data (data A) is output at the rising edge of the clock in the S2 state during the machine cycle of that instruction.

During the execution of an instruction that inputs data from a port, data at the input pin (data B) is captured internally while the clock is at a "H" level in the S1 state during the machine cycle of that instruction. That data is transferred to the accumulator at the start of the next machine cycle.

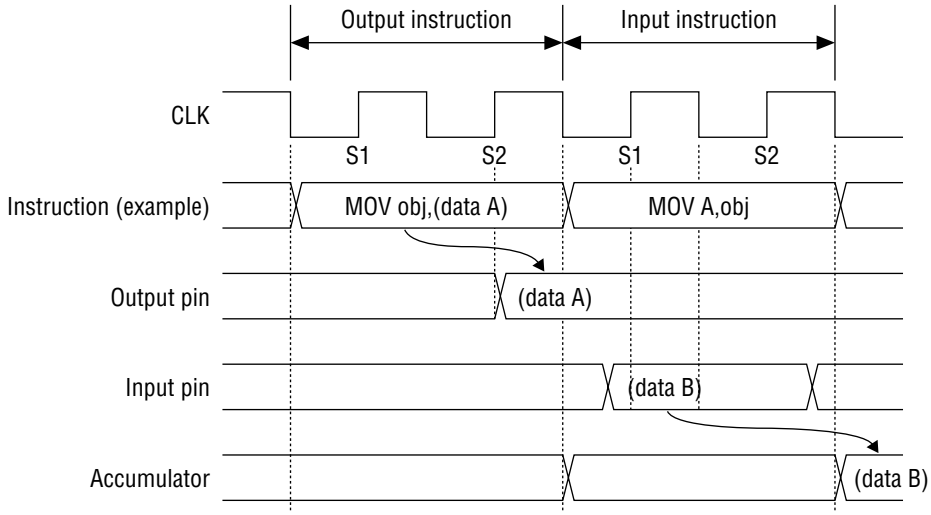


Figure 1-11 Port I/O Basic Timing

Note:

Regarding input signals

"0" will be captured in the internal register if a "L" level is input to the input pin even once (① of Figure 1-12) during the data capture interval.

"1" will be captured in the internal register only if a "H" level is maintained (② of Figure 1-12) throughout the data capture interval.

Therefore, if noise occurs in the input data, implement noise reduction measures with the program and peripheral devices.

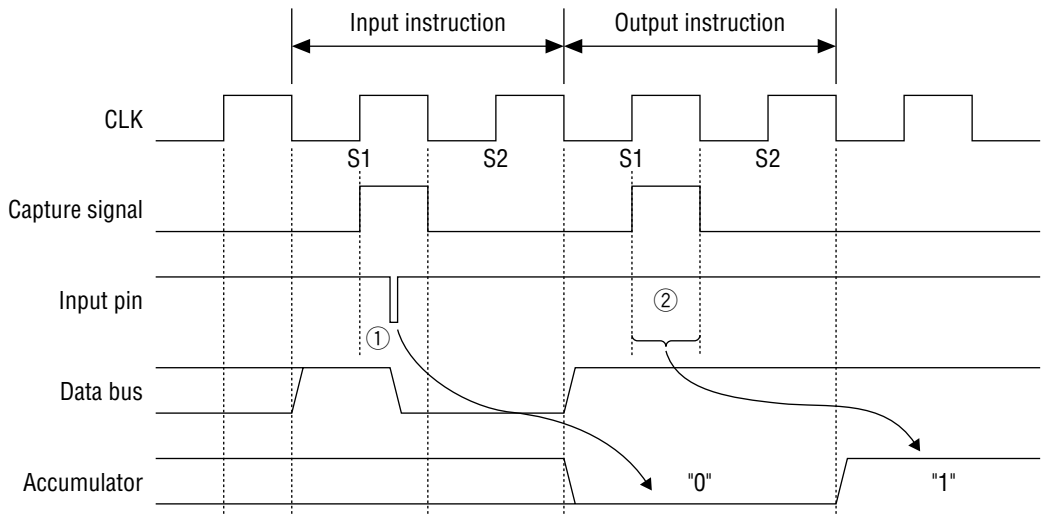


Figure 1-12 Input Data Example

1.7.3 Interrupt Basic Timing

Figure 1-13 shows the basic interrupt timing.

As shown in the figure, when an interrupt factor is generated, the interrupt factor is sampled at the falling edge of CLK and an interrupt request (IRQ) is set at the first half of S1.

When an interrupt condition is established and the CPU receives an interrupt, the interrupt routine will start beginning from the next machine cycle.

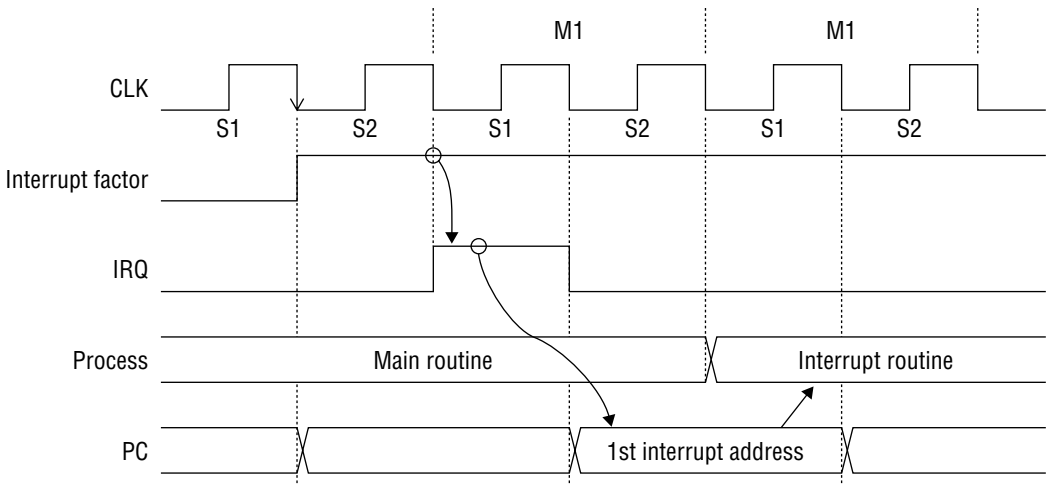


Figure 1-13 Interrupt Basic Timing

Chapter 2

CPU and Memory Spaces

Chapter 2 CPU and Memory Spaces

2.1 Overview

The ML63187, ML63189B, and ML63193 have an internal Oki's original CPU core nX-4/250 core.

The instruction set of the nX-4/250 core consists of 408 types of instructions.

The memory space consists of a 16-bit wide program memory space and a 4-bit wide data memory space. A stack for saving the program counter during a subroutine call or interrupt (call stack) and a stack for saving registers during a PUSH instruction (register stack) are provided separately from the memory space.

The program memory space is used for program data, ROM table data and melody note data.

In the data memory space, special function registers (SFRs) are located in BANK 0, the LCD display register (DSPR) in BANK 1, and data RAM in BANKS 2 to 9 (BANKS 2 to 5 for the ML63187, BANKS 2 to 7 for the ML63189B, and BANKS 2 to 9 for the ML63193).

2.2 Registers

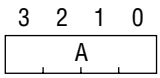
The nX-4/250 core processes data mainly with the accumulator and register set.

The register set is a programming model consisting of the HL and XY registers that store data memory addresses, the current bank register (CBR), the extra bank register (EBR), the RA register that stores program memory addresses, registers that control program flow, and registers that control flags and memory.

2.2.1 Accumulator (A)

The accumulator (A) is the central register for various arithmetic operations.

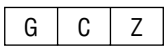
At system reset, the accumulator is initialized to "0". When an interrupt occurs, a "PUSH HL" instruction can be used if necessary to save the accumulator on the register stack. The accumulator can be restored with a "POP HL" instruction.



Accumulator

2.2.2 Flag Register

The flag register consists of 3 flags: the carry flag (C), the zero flag (Z) and the G flag (G). When an interrupt occurs, a "PUSH HL" instruction can be used if necessary to save the flag register on the register stack. The flag register can be restored with a "POP HL" instruction.



Flag register

2.2.2.1 Carry Flag (C)

The carry flag (C) is a 1-bit flag that is loaded with a carry during addition or a borrow during subtraction. At system reset, the carry flag is initialized to "0".

2.2.2.2 Zero Flag (Z)

The zero flag (Z) is a 1-bit flag that is set to "1" when the contents of the accumulator (A) are loaded with "0H". The zero flag is set to "0" when the contents of the accumulator (A) are loaded with a value other than "0H". However, the XCH instruction does not change the zero flag. At system reset, the zero flag is initialized to "0".

2.2.2.3 G Flag (G)

The G flag (G) changes to "1" when the HL, XY or RA registers overflow as the result of execution of a post-increment register indirect addressing instruction or as the result of an increment instruction for the HL, XY or RA registers. At system reset, the G flag is initialized to "0".

2.2.3 Master Interrupt Enable Flag (MIE)

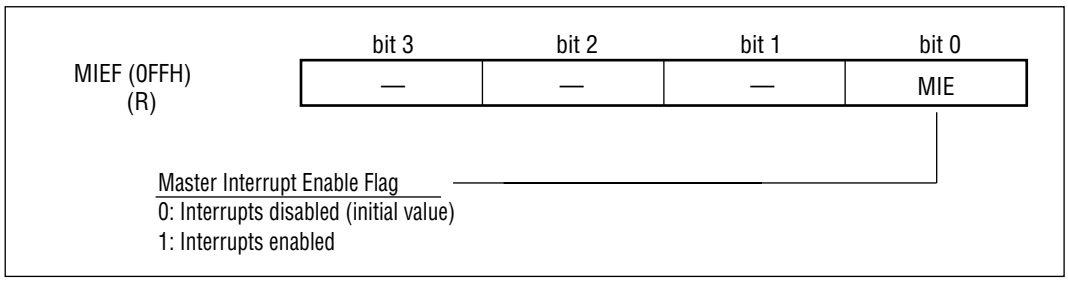
MIE (bit 0 of MIEF) is a flag that disables or enables all interrupts except for the watchdog timer interrupt. MIEF is a 4-bit register in which bit 0 is the master interrupt enable flag (MIE).

If MIE is "0", all interrupts are disabled. If MIE is "1", all interrupts are enabled (with the exception of the watchdog timer).

When any interrupt is received, MIE is cleared to "0". MIE is set to "1" by execution of a return from interrupt instruction (RTI instruction).

If multi-level interrupt processing is to be performed, execute a RTI instruction (MIE←"1") during the interrupt processing routines.

At system reset, MIE is initialized to "0". MIEF only supports data reference (R) of data memory through addressing instructions.



Note:

When setting MIE, use "EI" instructions (MIE←"1") and "DI" instructions (MIE←"0").

2.2.4 Current Bank Register (CBR), Extra Bank Register (EBR), HL Register (HL), XY Register (XY)

The CBR, EBR, HL, and XY registers are used for indirect addressing of data memory.

The CBR and EBR registers indicate the data memory bank. The HL and XY registers indicate addresses in the bank. CBR is also used in combination with 8-bit data in the instruction code for direct addressing within the current bank.

Figure 2-1 shows the various register combinations.

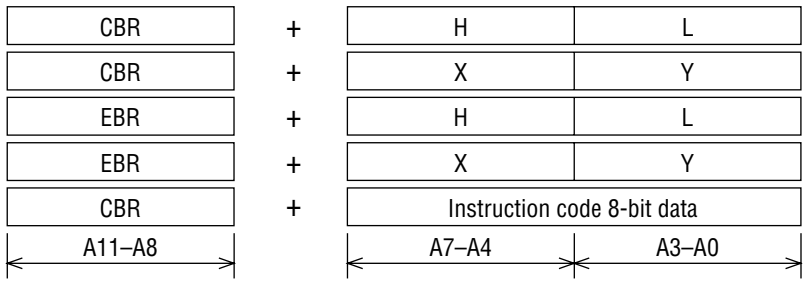


Figure 2-1 Various Register Combinations

A11 to A0 in Figure 2-1 indicate data memory addresses (4K nibbles max.).

At system reset, the CBR, EBR, HL, and XY registers are initialized to "0".

When an interrupt occurs, a "PUSH HL" or "PUSH XY" instruction can be used if necessary to save the CBR, EBR, HL, and XY registers on the register stack. These registers can be restored with a "POP HL" or "POP XY" instruction.

The CBR, EBR, HL, and XY registers are assigned to special function register (SFR) addresses 0F9H to 0FEH.

		bit 3	bit 2	bit 1	bit 0
EBR	(0FEH) (R/W)	e_3	e_2	e_1	e_0
CBR	(0FDH) (R/W)	c_3	c_2	c_1	c_0
H	(0FCH) (R/W)	h_3	h_2	h_1	h_0
L	(0FBH) (R/W)	l_3	l_2	l_1	l_0
X	(0FAH) (R/W)	x_3	x_2	x_1	x_0
Y	(0F9H) (R/W)	y_3	y_2	y_1	y_0

2.2.5 Program Counter (PC)

The program counter (PC) is a counter with 16 valid bits that specifies the program memory space.

2.2.6 RA Registers (RA3, RA2, RA1, RA0)

The RA registers are used for indirect program memory addressing (ROM table reference instructions).

Figure 2-2 shows the address configuration of the RA registers.

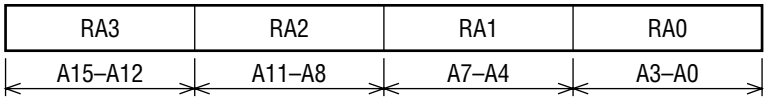


Figure 2-2 Address Configuration of RA3 to RA0 Registers

Within the A15 to A0 of Figure 2-2, A14 to A0 indicate program memory addresses (32K words max.).

RA3 to RA0 are assigned to special function register (SFR) addresses 0F2H to 0F5H.

		bit 3	bit 2	bit 1	bit 0
RA3	(0F5H) (R/W)	a_{15}	a_{14}	a_{13}	a_{12}
RA2	(0F4H) (R/W)	a_{11}	a_{10}	a_9	a_8
RA1	(0F3H) (R/W)	a_7	a_6	a_5	a_4
RA0	(0F2H) (R/W)	a_3	a_2	a_1	a_0

At system reset, RA3 to RA0 are initialized to "0".

Note:

When executing a ROM table reference instruction that uses RA registers, do not use addresses located in the SFR area to transfer ROM table data to RA registers, otherwise indirect addressing of program memory will not operate properly.

2.2.7 Stack Pointer (SP) and Call Stack

The stack pointer (SP) is a pointer that indicates the call stack address where the program counter is saved when a subroutine call or interrupt occurs.

The SP is a 4-bit up/down counter that is incremented during stack saves and is decremented during stack restores.

The call stack has 16 levels from address 0H to address 0FH. Because the hardware requires 1 level of the call stack during program execution, only 15 levels can be used for stack saves. The contents of the call stack cannot be read or written by the program.

Figure 2-3 shows the relation between SP and the call stack.

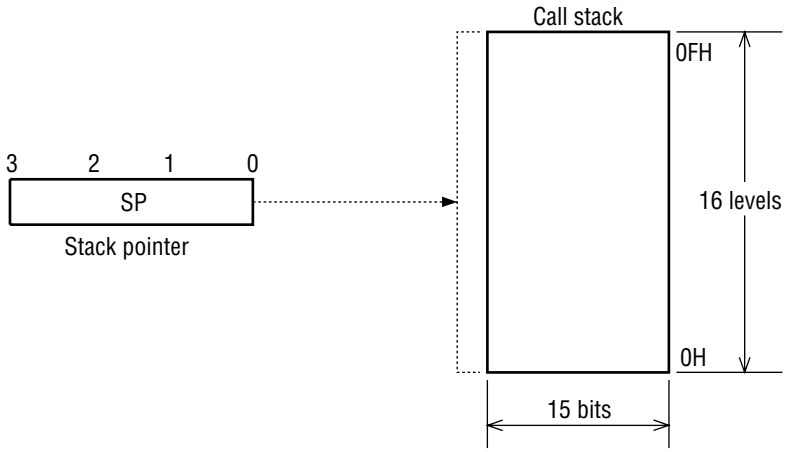


Figure 2-3 Relation Between SP and Call Stack

SP is assigned to special function register (SFR) address 0F7H.

	bit 3	bit 2	bit 1	bit 0
SP (0F7H) (R)	SP3	SP2	SP1	SP0

At system reset, SP is initialized to "0" and points to address "0H" of the call stack. SP is a read-only register and writes are invalid.

2.2.8 Register Stack Pointer (RSP) and Register Stack

The register stack pointer (RSP) is a pointer that indicates the register stack address for saving various registers.

RSP is a 4-bit up/down counter that is incremented during stack saves (execution of PUSH instructions) and is decremented during stack restores (execution of POP instructions).

The register stack has 16 levels from address 0H to address 0FH. The contents of the register stack cannot be read or written by the program.

Figure 2-4 shows the relation between RSP and the register stack.

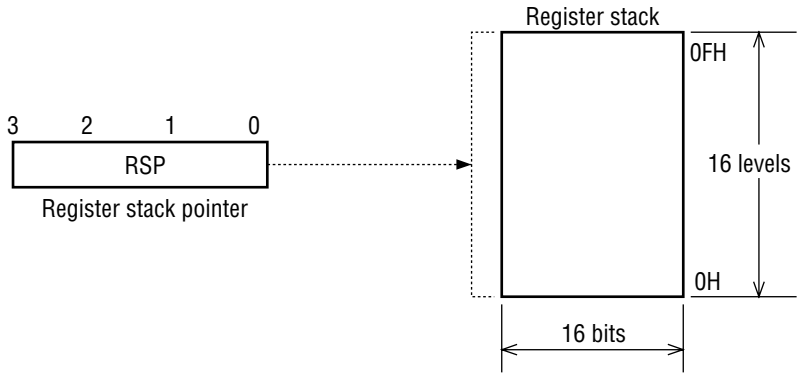


Figure 2-4 Relation Between RSP and Register Stack

The various registers shown in Figure 2-5 are saved onto and restored from the register stack by PUSH and POP instructions.

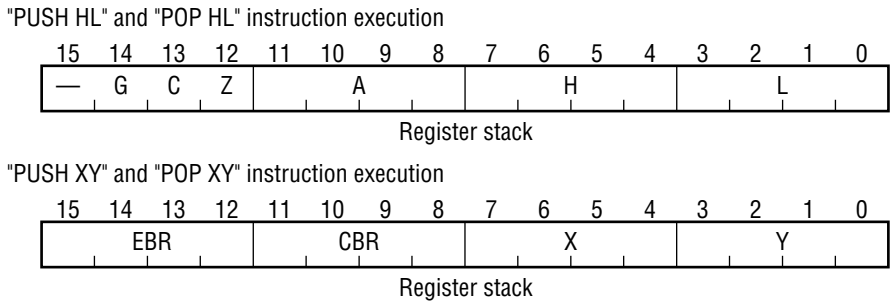


Figure 2-5 Register Save/Restore by Execution of PUSH/POP Instructions

RSP is assigned to special function register (SFR) address 0F6H.

	bit 3	bit 2	bit 1	bit 0
RSP (0F6H) (R/W)	rsp3	rsp2	rsp1	rsp0

At system reset, RSP is initialized to "0" and points to address "0H" of the register stack.

2.3 Memory Spaces

2.3.1 Program Memory Space

The program memory space is the read-only memory that stores program data.

The program memory space has a data length of 16 bits and extends from address 0000H to address 3FFFH in the ML63187, from address 0000H to address 7FFFH in the ML63189B, and from address 0000H to address FFFFH in the ML63193.

In addition to program data, the program memory can also store ROM table data and the melody data. Figure 2-6 shows the configuration of the program memory space.

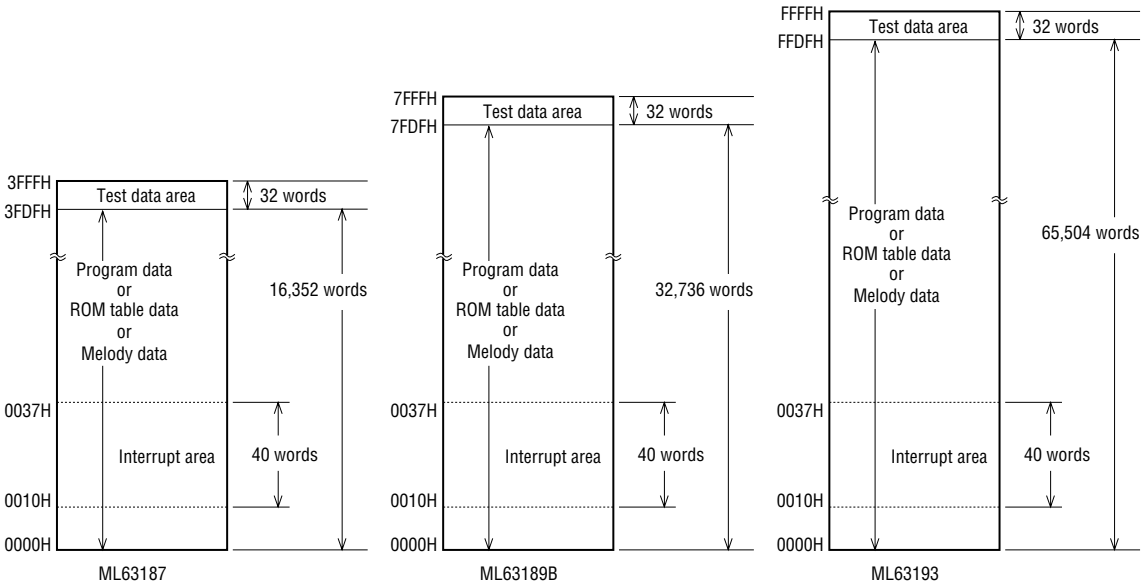


Figure 2-6 Program Memory Space Configuration

After system reset, instruction execution begins at address 0000H. The interrupt area from address 0010H to address 0037H contains starting addresses of the interrupt processing routines that are executed when interrupts are generated. (Refer to Chapter 4, "ML63187 Interrupt," Chapter 5, "ML63189B Interrupt," and Chapter 6, "ML63193 Interrupt.")

ROM table data is transferred to data memory by ROM table reference instructions.

The melody data defines the tone, tone length, and end tone used in the melody circuit of the ML63187, ML63189B, and ML63193. After an MSA instruction specifies the starting address, the melody data is automatically transferred to the melody circuit when a melody data interrupt occurs. (Refer to Chapter 13, "Melody Driver.")

Because the test data area contains program data for testing, it cannot be used as a program data area.

2.3.2 Data Memory Space

The data memory space contains data RAM and special function registers (SFRs).

The data memory consists of 10 banks. One bank unit is 256 nibbles. BANK 0 is allocated as a SFR area, BANK 1 as the LCD display register, and BANK 2 and the following BANKS are data RAM.

Figure 2-7 shows the configuration of the data memory space.

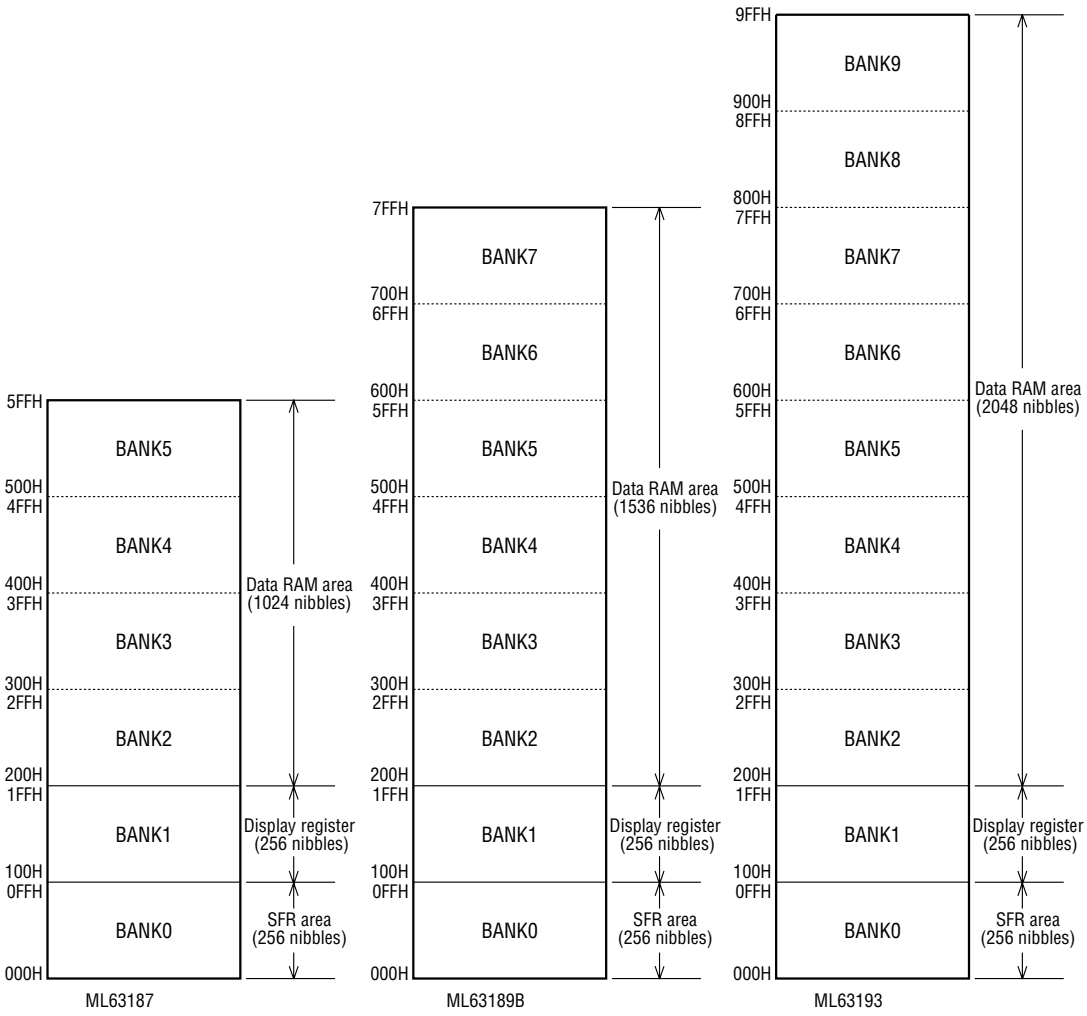


Figure 2-7 Data Memory Space Configuration

Chapter 3

CPU Control Functions

Chapter 3 CPU Control Functions

3.1 Overview

Operating states, including system reset, are classified as follows.

- Normal operation mode
- System reset mode
- Halt mode

Figure 3-1 shows the CPU operating state transition diagram.

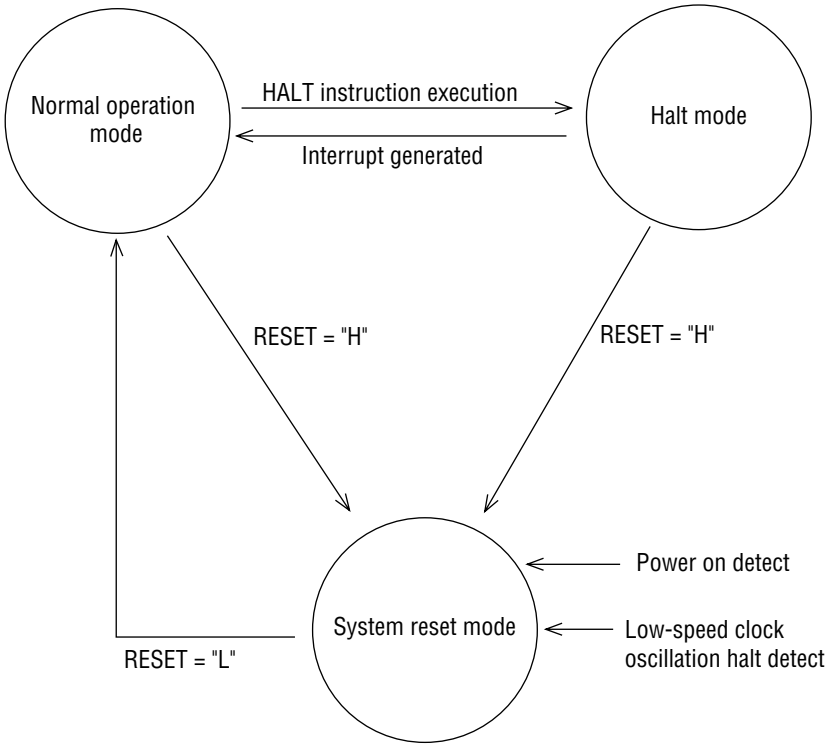


Figure 3-1 Operating State Transition Diagram

The normal operation mode is the state in which the CPU executes instructions sequentially.

The system reset mode begins when a reset input causes the CPU to begin system reset processing where registers and pins are initialized. The CPU remains in this state until instruction execution begins. After system reset processing, instruction execution begins from address 0000H.

The halt mode is the state in which the CPU is halted (instruction execution suspended) but internal peripheral functions continue to operate. During the halt mode, the PC is not incremented. Even upon entering the halt mode, port and peripheral functions will not change. Transfer to the halt mode is accomplished by executing a "HALT" instruction.

3.2 System Reset Mode (RST)

3.2.1 Transfer to and State of System Reset Mode

The following three factors cause a transfer to the system reset mode.

- Setting the RESET pin to a "H" level
  For the ML63193, since it has an internal reset sampling (2 kHz) circuit, the system reset mode is entered by holding the RESET pin at a "H" level for 1 ms or more.
  In the ML63193, whether the reset sampling circuit is used or not can be selected by mask option.
- Detection of power on (not applied if the reset sampling circuit is used in the ML63193)
- Detection that low-speed clock oscillation is halted

The following operations are performed in the system reset mode.

(1) CPU is initialized.

(2) Backup flag changes to "1" and backup circuit changes to ON state.

(3) Bias reference voltage supply (VR) is energized.

(4) All LCD driver outputs are turned OFF and the outputs change to the V_{SS} level.

(5) All special function registers (SFRs) are initialized. However, data RAM and display registers are not initialized.

After system reset processing, instruction execution begins from address 0000H.

Figures 3-2 and 3-3 show the system reset generator circuit and Figure 3-4 shows the signals when a system reset is generated.

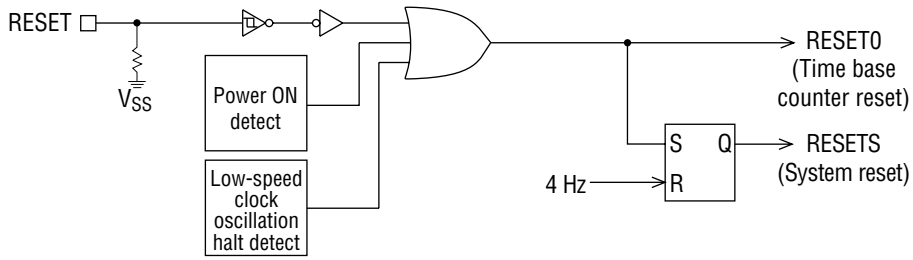


Figure 3-2 ML63187/ML63189B/ML63193 (reset sampling circuit not used) System Reset Generator Circuit

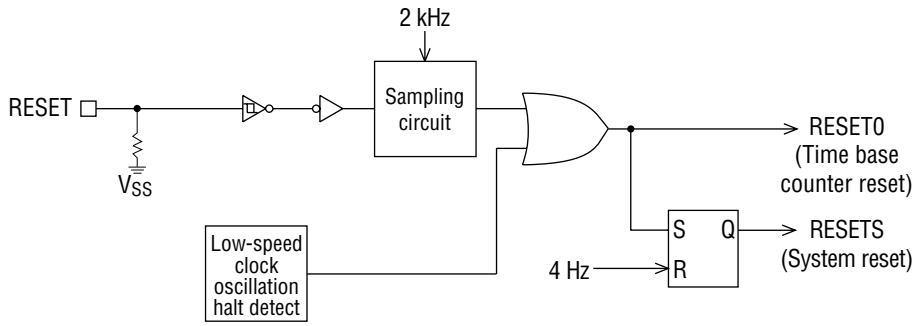


Figure 3-3 ML63193 (reset sampling circuit used) System Reset Generator Circuit

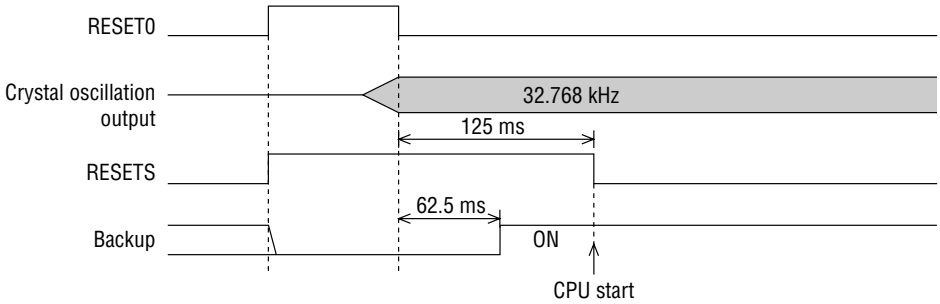


Figure 3-4 Signals When System Reset is Generated

Note:

- System reset takes priority over all other processing and terminates all processing up to that point in time. Therefore, the contents of RAM and display registers, which are not initialized, cannot be guaranteed after a system reset.
- When the reset sampling circuit is used in the ML63193:
  When setting the RESET pin to a "H" level to perform transfer to the system reset mode, set the RESET pulse width to 1 ms or more.

3.3 Halt Mode

3.3.1 Transfer to and State of Halt Mode

Transfer to the halt mode is performed by the software when a HALT instruction is executed.

When a HALT instruction is executed, the CPU enters the HALT mode at the S2 state of the HALT instruction.

Oscillation and time base counter operation continue while in the halt mode.

If an interrupt request occurs at the same time as execution of a HALT instruction, interrupt processing has priority and the HALT instruction will not be executed. After the HALT instruction performs the equivalent operation of a NOP instruction, the interrupt routine is entered. When an RTI instruction is used to complete the interrupt routine, the main routine is resumed beginning from the instruction immediately following the HALT instruction.

Figure 3-5 shows the timing when a HALT instruction and interrupt request occur simultaneously.

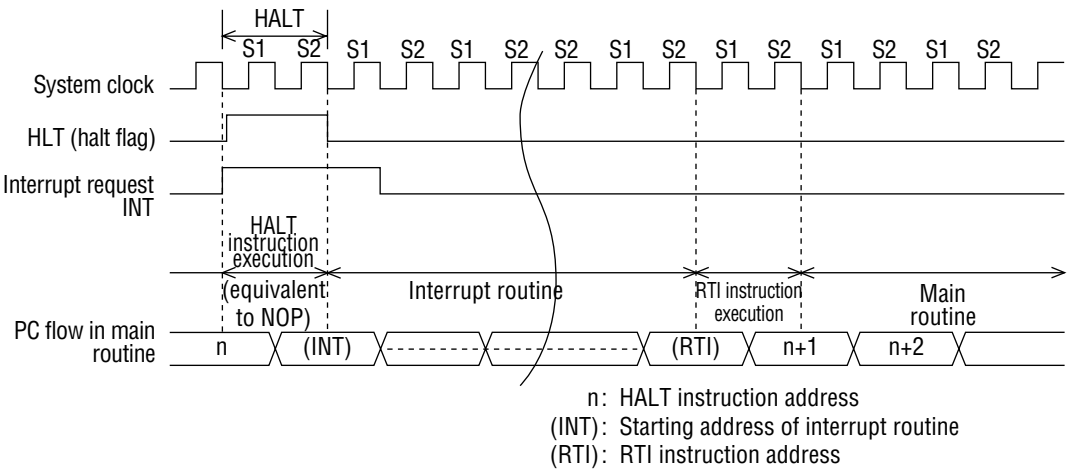


Figure 3-5 Timing of Simultaneous HALT Instruction and Interrupt Request

Note:

While an interrupt request is generated, execution of a HALT instruction will not transfer operation to the halt mode.

3.3.2 Halt Mode Release

The following two methods are available to release the halt mode.

- Release by interrupt generation (transfer to normal operation mode)
- Release by RESET pin (transfer to system reset mode)

3.3.2.1 Release of Halt Mode by Interrupt

If the halt mode is to be released by an interrupt, the enable flag of the interrupt used for release must be set to "1" prior to entering the halt mode. When the halt mode is released by an interrupt, operation transfers to the normal operation mode.

Figure 3-6 shows the timing of transferring to the halt mode by execution of a HALT instruction and of releasing the halt mode by an interrupt.

When the halt mode is released by an interrupt request, the first instruction immediately following the HALT instruction is executed and then the interrupt routine is entered. When an RTI instruction is used to complete the interrupt routine, the main routine is resumed beginning from the second instruction after the HALT instruction.

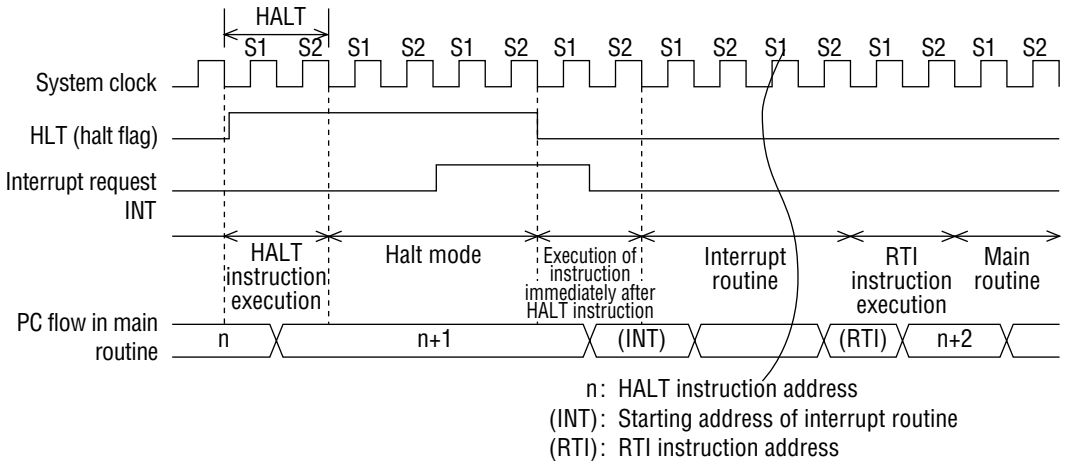


Figure 3-6 Timing of Transfer to Halt Mode and Release of Halt Mode by Interrupt

Note:

If the halt mode is to be released, set individual interrupt enable flags to "1". If an individual interrupt enable flag is "0", the corresponding interrupt request signal cannot reset the HLT flag, regardless of whether the master interrupt enable flag (MIE) is "0" or "1".

3.3.2.2 Release of Halt Mode by RESET Pin

If a high-level is input to the RESET pin, the CPU is released from the halt mode and transfers to the system reset mode.

3.3.3 Melody Data Interrupt and Halt Mode Release

The halt mode is not released by a melody data interrupt.

The melody data interrupt is different from a conventional interrupt in that the melody data interrupt is a hardware processing interrupt used for transfer of melody data to the melody circuit. It is not dependent on the program.

When this interrupt is generated, the instruction immediately after the HALT instruction is executed, then the melody data is transferred to the melody circuit, and the HALT instruction is executed again. This sequence is indicated in Figure 3-7.

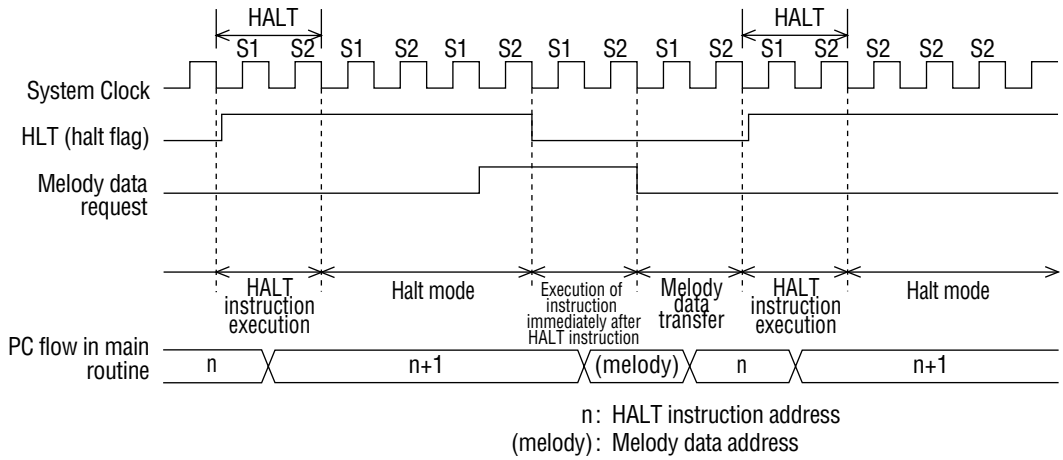


Figure 3-7 Melody Data Request Interrupt Operation

3.3.4 Note Concerning HALT Instruction

As described above, the instruction immediately after the HALT instruction may be executed any number of times. For this reason, always place an NOP instruction immediately after the HALT instruction.

(Example)

```
    •
    •
    •
  HALT
  NOP
    •
    •
    •
```

Chapter 4

ML63187 Interrupt (INT187)

Chapter 4 ML63187 Interrupt (INT187)

4.1 Overview

The ML63187 supports 14 interrupt factors: 2 external interrupts and 12 internal interrupts.

With the exception of the watchdog timer interrupt, interrupt enable/disable is controlled by the master interrupt enable flag (MIE) and the individual interrupt enable registers (IE0 to IE4). Watchdog timer interrupt is a non-maskable interrupt.

When interrupt conditions are met, the interrupt routine is executed from the interrupt start address.

Table 4-1 indicates a list of interrupt factors, and Figure 4-1 shows the interrupt control equivalent circuit.

Table 4-1 ML63187 Interrupt Factors

Priority	Interrupt factor	Symbol	Interrupt start address
1	Watchdog timer interrupt	WDTINT	0010H
2	Melody end interrupt	MDINT	0012H
3	External interrupt 0 (PB 4-bit OR input)	XI0INT	0014H
4	External interrupt 2 (PE.3)	XI2INT	0018H
5	Timer 0 interrupt	TM0INT	0020H
6	Timer 1 interrupt	TM1INT	0022H
7	Timer 2 interrupt	TM2INT	0024H
8	Timer 3 interrupt	TM3INT	0026H
9	Shift register interrupt	SFTINT	002CH
10	T10 Hz interrupt	T10HzINT	002EH
11	32 Hz interrupt	32HzINT	0030H
12	16 Hz interrupt	16HzINT	0032H
13	4 Hz interrupt	4HzINT	0034H
14	2 Hz interrupt	2HzINT	0036H

If multiple interrupts are detected simultaneously, the lowest interrupt start address is given priority.

For details on interrupt operation, refer to Chapter 8 (Time Base Counter), Chapter 9 (Timers), Chapter 10 (100 Hz Timer Counter), Chapter 11 (Watchdog Timer), Chapter 12 (Ports), Chapter 13 (Melody Driver), and Chapter 15 (Shift Register).

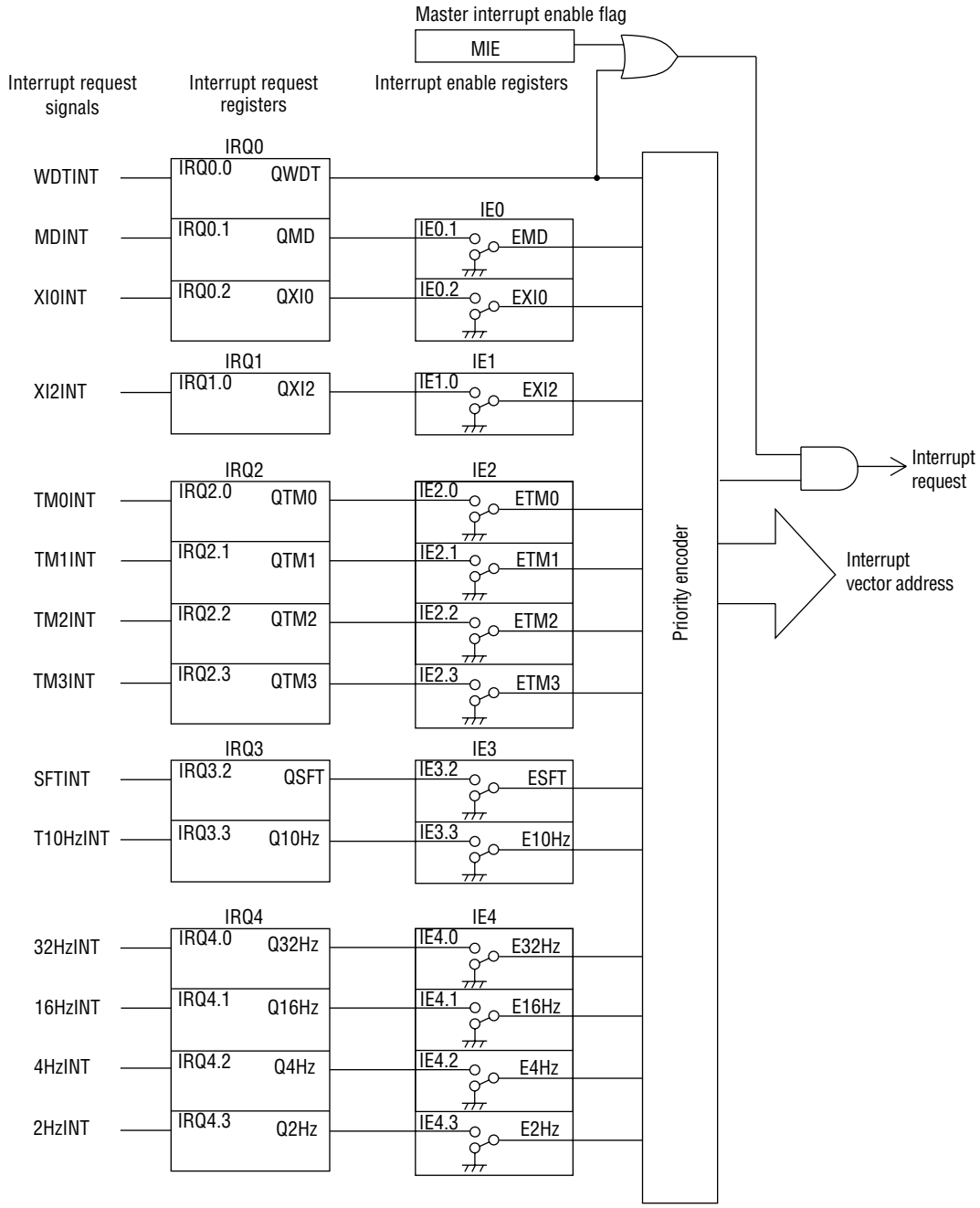


Figure 4-1 ML63187 Interrupt Control Equivalent Circuit

4.2 Interrupt Registers

The following three types of registers are used to control interrupts.

(1) Master interrupt enable register (MIEF)

(2) Interrupt enable registers (IE0 to IE4)

(3) Interrupt request registers (IRQ0 to IRQ4)

These registers are described below.

(1) Master interrupt enable register (MIEF)

MIEF is a 4-bit register in which bit 0 is the master interrupt enable flag (MIE).

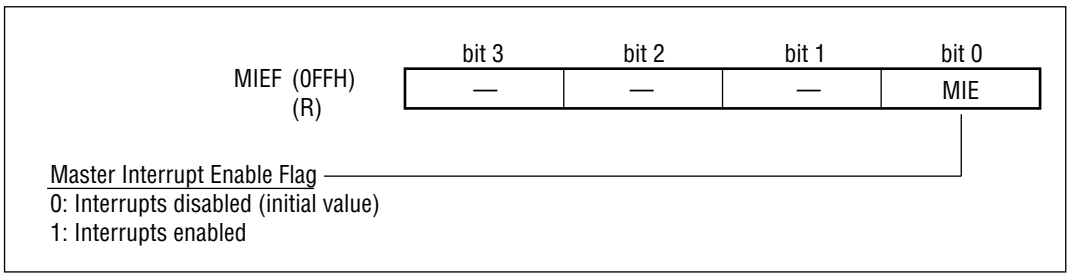
MIE (bit 0 of MIEF) is a flag that disables or enables all interrupts except for the watchdog timer interrupt.

If MIE is "0", all interrupts are disabled. If MIE is "1", all interrupts are enabled (with the exception of the watchdog timer).

When any interrupt is received, MIE is cleared to "0". MIE is set to "1" by execution of a return from interrupt instruction (RTI instruction).

If multi-level interrupt processing is to be performed, execute an RTI instruction (MIE←"1") during the interrupt processing routines.

At system reset, MIE is initialized to "0". MIEF only supports data reference (R) of data memory through addressing instructions.



Note:

When setting MIE, use "EI" instructions (MIE←"1") and "DI" instructions (MIE←"0").

(2) Interrupt enable registers (IE0 to IE4)

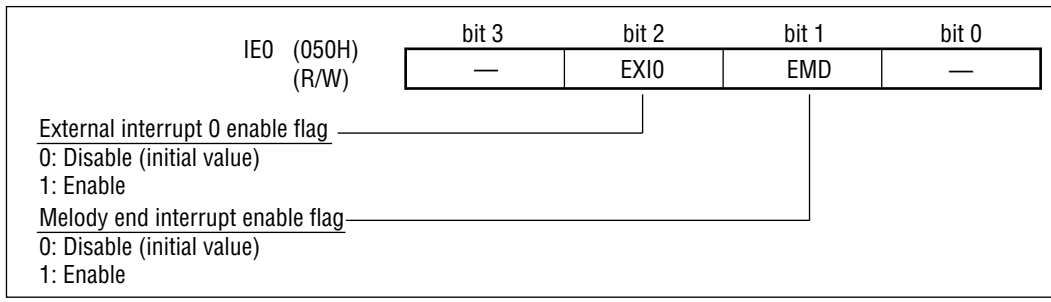
IE0, IE1, IE2, IE3, and IE4 are registers that consist of 4 bits each.

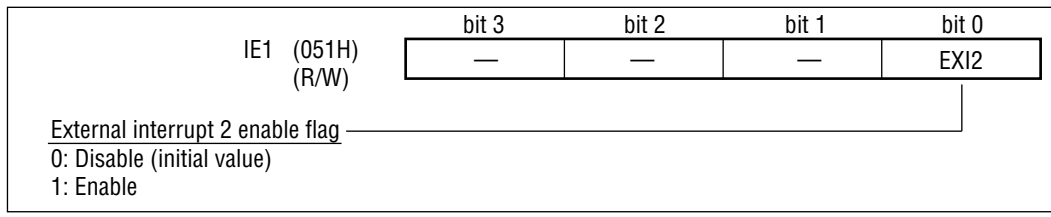
A logical AND of the corresponding bits of an interrupt enable register (IE0 to IE4) and an interrupt request register (IRQ0 to IRQ4) determines whether or not each interrupt request is issued to the CPU. The watchdog timer interrupt is non-maskable, and is therefore not dependent upon the interrupt enable registers (IE0 to IE4) and the master interrupt enable register (MIEF).

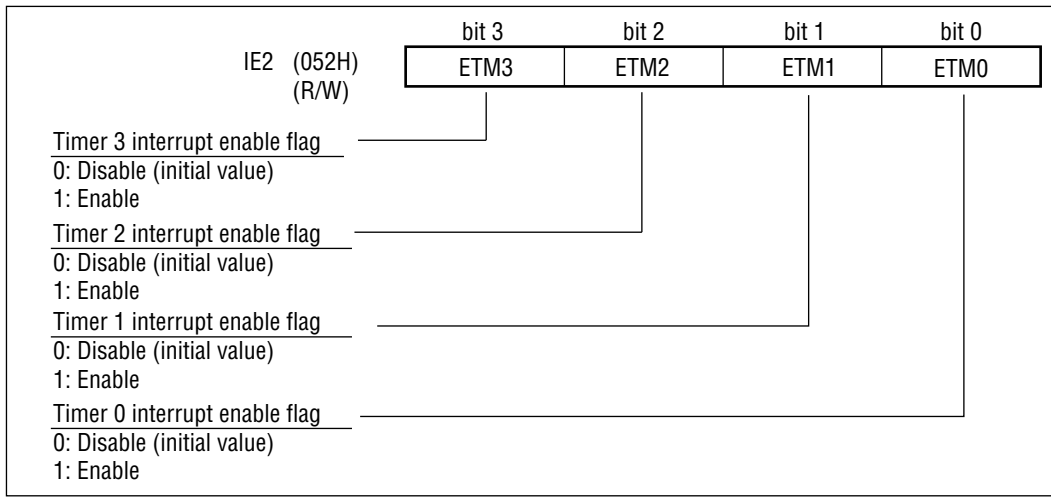
If multiple interrupts request the CPU at the same time, as shown in Table 4-1, the interrupts are accepted in order of highest priority and low priority interrupts are placed on hold.

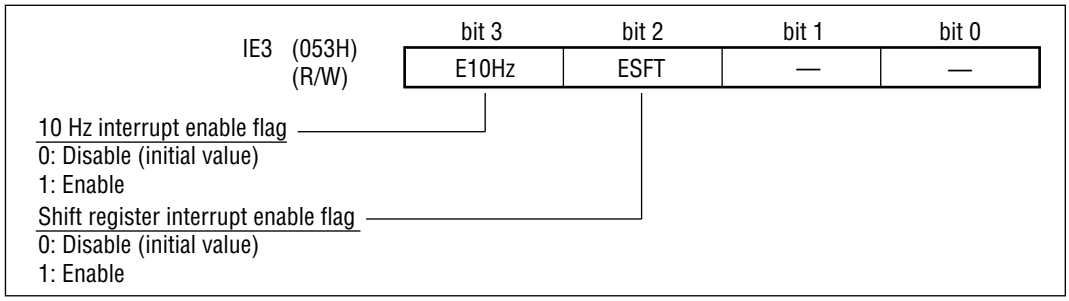
When an interrupt is received, the master interrupt enable flag (MIE) is cleared to "0". The corresponding bits in the interrupt enable registers (IE0 to IE4) do not change.

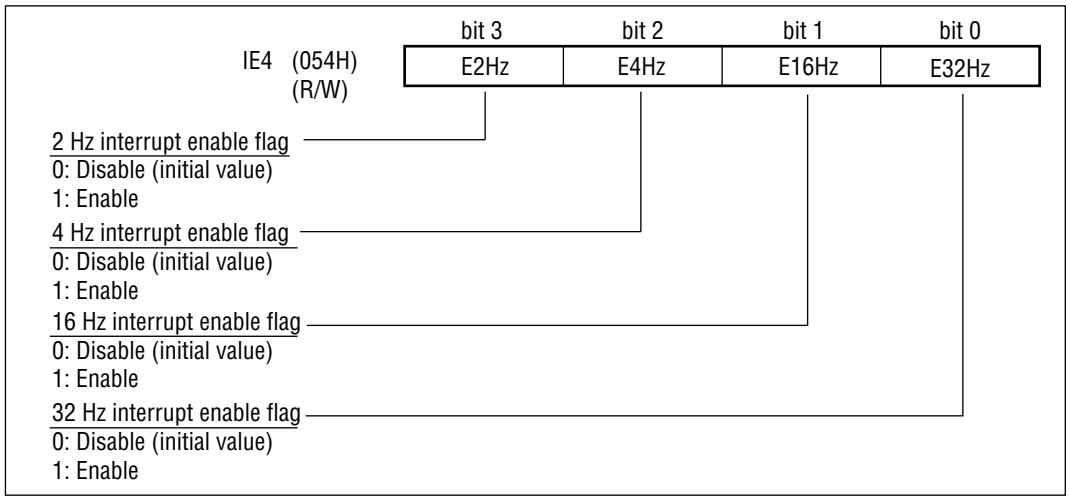
At system reset, each bit of IE0 through IE4 is initialized to "0".








IE3 (053H)
(R/W)
bit 3
bit 2
bit 1
bit 0
E10Hz
ESFT
—
—
10 Hz interrupt enable flag
0: Disable (initial value)
1: Enable
Shift register interrupt enable flag
0: Disable (initial value)
1: Enable


IE4 (054H)
(R/W)
bit 3
bit 2
bit 1
bit 0
E2Hz
E4Hz
E16Hz
E32Hz
2 Hz interrupt enable flag
0: Disable (initial value)
1: Enable
4 Hz interrupt enable flag
0: Disable (initial value)
1: Enable
16 Hz interrupt enable flag
0: Disable (initial value)
1: Enable
32 Hz interrupt enable flag
0: Disable (initial value)
1: Enable

(3) Interrupt request registers (IRQ0 to IRQ4)

IRQ0, IRQ1, IRQ2, IRQ3 and IRQ4 are registers that consist of 4 bits each.

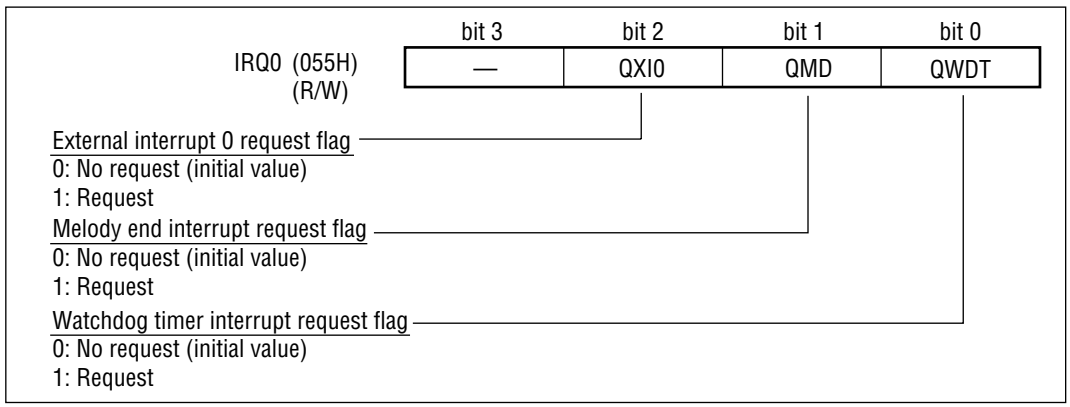
When an interrupt request is generated, the corresponding bit of the interrupt request register is set to "1" in the first half of the S1 state of the next instruction. So that the CPU can receive interrupt requests, set the master interrupt enable flag (MIE) to "1" and set the appropriate flag of the corresponding interrupt enable register (IE0 to IE4) to "1".

The watchdog timer interrupt is non-maskable and does not depend upon the interrupt enable register or the master interrupt enable register (MIEF).

Setting the appropriate bits of an interrupt request register to "1" allows software interrupts to be generated.

When an interrupt request is received, the corresponding bits of IRQ0 to IRQ4 are cleared to "0".

At system reset, each bit of IRQ0 through IRQ4 is initialized to "0".



bit 2: QXI0 (reQuest eXternal Interrupt 0)

The external interrupt 0 request flag.

The external interrupt 0 is assigned as the secondary function of each bit of port B (PB.0 to PB.3). External interrupt 0 requests are generated by a 4-bit ORed input.

bit 1: QMD (reQuest Melody Driver)

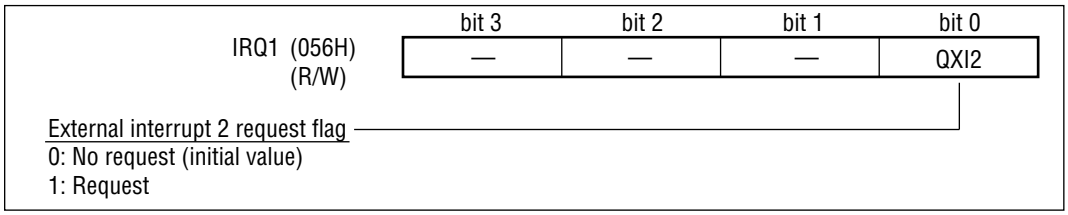
Melody end interrupt request flag.

Melody end interrupts are generated when the melody driver outputs the end note data (END bit = "1").

bit 0: QWDT (reQuest WatchDog Timer)

Watchdog timer interrupt request flag.

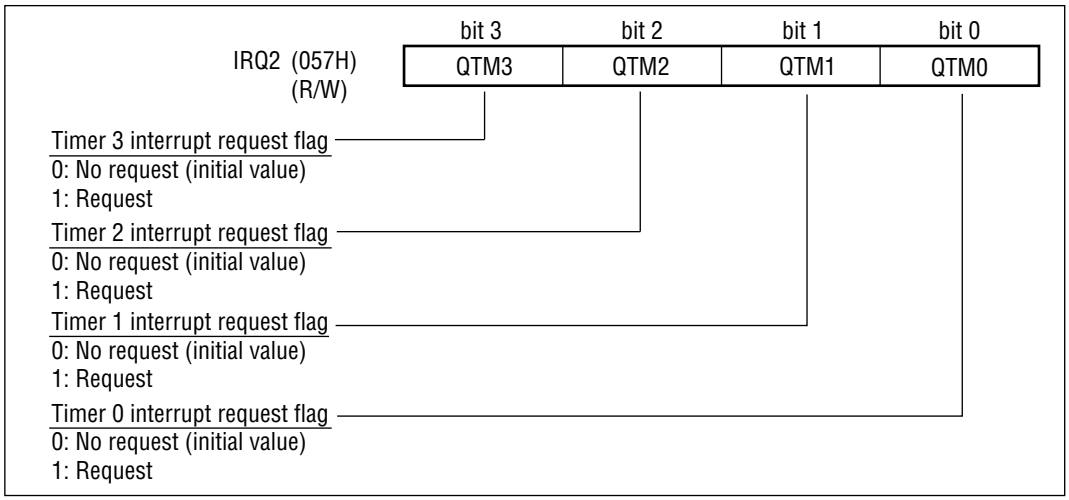
When the watchdog timer is started and then overflow occurs, an interrupt is requested. The watchdog timer interrupt is non-maskable and does not depend upon the interrupt enable registers or the master interrupt enable register (MIE).



bit 0: QXI2 (reQuest eXternal Interrupt 2)

External interrupt 2 request flag.

The external interrupt 2 is assigned as a secondary function of port E.3 (PE.3). Generation of the external interrupt 2 is triggered by the falling edge of the 128 Hz or 4 kHz output of the time base counter.



bit 3: QTM3 (reQuest TiMer 3)

Timer 3 interrupt request flag.

A timer 3 interrupt request is generated whenever timer 3 overflows.

bit 2: QTM2 (reQuest TiMer 2)

Timer 2 interrupt request flag.

A timer 2 interrupt request is generated whenever timer 2 overflows.

bit 1: QTM1 (reQuest TiMer 1)

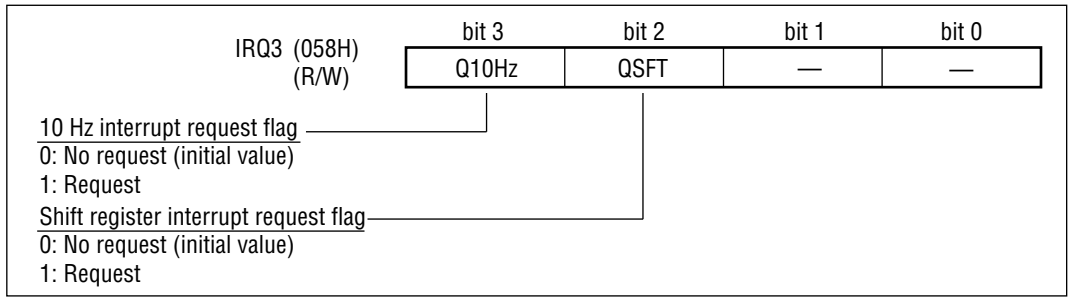
Timer 1 interrupt request flag.

A timer 1 interrupt request is generated whenever timer 1 overflows.

bit 0: QTM0 (reQuest TiMer 0)

Timer 0 interrupt request flag.

A timer 0 interrupt request is generated whenever timer 0 overflows.



bit 3: Q10Hz (reQuest 10 Hz)

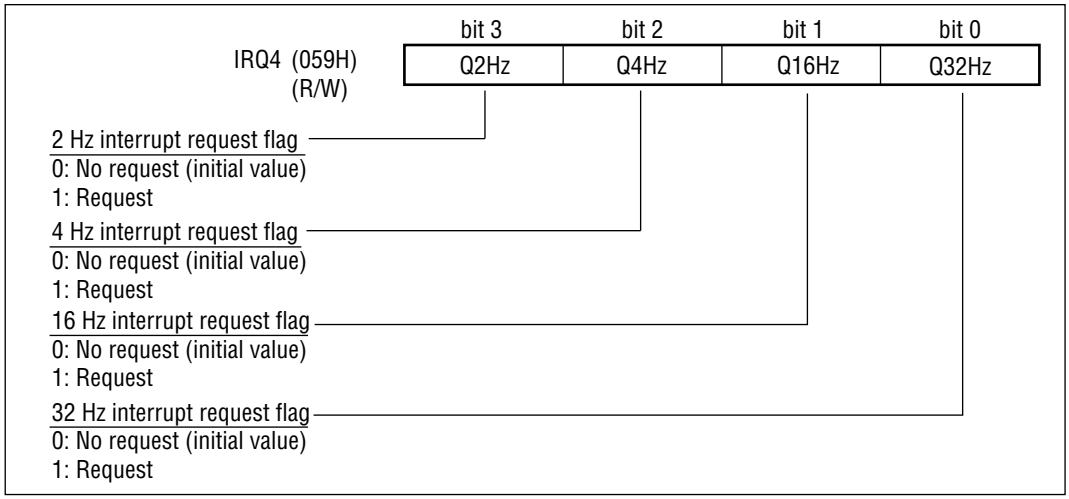
10 Hz interrupt request flag.

A 10 Hz interrupt request is generated whenever the 10 Hz carry generated by the 100 Hz timer counter is output.

bit 2: QSFT (reQuest ShiFT register)

Shift register interrupt request flag.

A shift register interrupt is generated when the 8-bit data transfer for the shift register is completed.



bit 3: Q2Hz (reQuest 2 Hz)

2 Hz interrupt request flag.

A 2 Hz interrupt request is generated at every falling edge of the 2 Hz output of the time base counter.

bit 2: Q4Hz (reQuest 4 Hz)

4 Hz interrupt request flag.

A 4 Hz interrupt request is generated at every falling edge of the 4 Hz output of the time base counter.

bit1: Q16Hz (reQuest 16 Hz)

16 Hz interrupt request flag.

A 16 Hz interrupt request is generated at every falling edge of the 16 Hz output of the time base counter.

bit 0: Q32Hz (reQuest 32 Hz)

32 Hz interrupt request flag.

A 32 Hz interrupt request is generated at every falling edge of the 32 Hz output of the time base counter.

4.3 Interrupt Sequence

4.3.1 Interrupt Processing

While MIE is "1", operation transfers to interrupt processing when individual interrupt factors are generated.

The watchdog timer interrupt is non-maskable and regardless of the MIE flag status, operation will shift to interrupt processing when the watchdog timer interrupt factor is generated.

The following processes are performed when an interrupt is generated.

(1) MIE and the corresponding interrupt request flag are cleared to "0".

(2) The program counter (PC) is saved on the call stack.

(3) The call stack pointer (SP) is incremented by 1. (SP←SP+1)

(4) The starting address of the interrupt routine is loaded into the program counter (PC).

Interrupt processing is performed in 0 machine cycles.

Figure 4-2 shows the stack contents after an interrupt is generated.

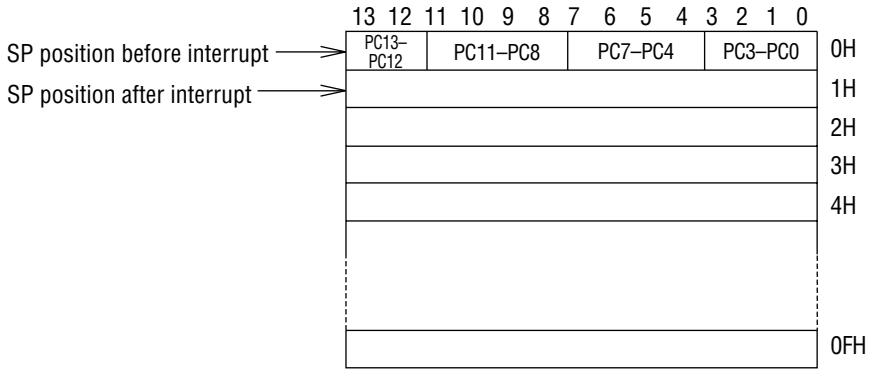


Figure 4-2 Call Stack Contents after Interrupt Generation

4.3.2 Return from an Interrupt Routine

Return from a watchdog timer interrupt routine is performed with an "RTNMI" instruction.

Return from all other interrupt routines is performed with an "RTI" instruction.

Execution of "RTI" and "RTNMI" instructions both require 1 machine cycle.

When returning from an interrupt routine, the CPU performs the following processes.

(1) The call stack pointer (SP) is decremented by 1. (SP←SP–1)

(2) MIE is set to "1" (when an "RTNMI" instruction is used, MIE is restored to its state prior to the interrupt).

(3) 1 is added to the call stack contents and that value is loaded into the program counter (PC).

Notes:

- While the MIE flag is "0" (interrupt disabled state), if a watchdog timer interrupt is processed and an "RTI" instruction is executed, the MIE flag will be set to "1" and interrupts enabled.
- Use "RTNMI" instructions to return from watchdog timer interrupts only. Use "RTI" instructions for normal interrupts.

4.3.3 Interrupt Hold Instructions

Interrupt requests are not received after execution of interrupt hold instruction.

The interrupt hold instructions follow.

- ROM table reference instructions
- Stack operation instructions
- Jump instructions
- Conditional branch instructions
- Call/return instructions
- "EI" (set MIE flag) instructions, "DI" (clear MIE flag) instructions and "MSA cadr15" (start melody output) instructions within control instructions

Note:

If interrupt hold instructions are used consecutively, even if an interrupt is generated, that interrupt may be put on hold for a considerable amount of time before the interrupt routine begins. Interrupt requests are received after execution of an instruction other than interrupt hold instructions.

Chapter 5

ML63189B Interrupt (INT189)

Chapter 5 ML63189B Interrupt (INT189)

5.1 Overview

The ML63189B supports 15 interrupt factors: 3 external interrupts and 12 internal interrupts.

With the exception of the watchdog timer interrupt, interrupt enable/disable is controlled by the master interrupt enable flag (MIE) and the individual interrupt enable registers (IE0 to IE4). Watchdog timer interrupt is a non-maskable interrupt.

When interrupt conditions are met, the interrupt routine is executed from the interrupt start address.

Table 5-1 indicates a list of interrupt factors, and Figure 5-1 shows the interrupt control equivalent circuit.

Table 5-1 ML63189B Interrupt Factors

Priority	Interrupt factor	Symbol	Interrupt start address
1	Watchdog timer interrupt	WDTINT	0010H
2	Melody end interrupt	MDINT	0012H
3	External interrupt 0 (PB 4-bit OR input)	XI0INT	0014H
4	External interrupt 2 (PE.3)	XI2INT	0018H
5	External interrupt 5 (P0 4-bit OR input)	XI5INT	001EH
6	Timer 0 interrupt	TM0INT	0020H
7	Timer 1 interrupt	TM1INT	0022H
8	Timer 2 interrupt	TM2INT	0024H
9	Timer 3 interrupt	TM3INT	0026H
10	Shift register interrupt	SFTINT	002CH
11	T10 Hz interrupt	T10HzINT	002EH
12	32 Hz interrupt	32HzINT	0030H
13	16 Hz interrupt	16HzINT	0032H
14	4 Hz interrupt	4HzINT	0034H
15	2 Hz interrupt	2HzINT	0036H

If multiple interrupts are detected simultaneously, the lowest interrupt start address is given priority.

For details on interrupt operation, refer to Chapter 8 (Time Base Counter), Chapter 9 (Timers), Chapter 10 (100 Hz Timer Counter), Chapter 11 (Watchdog Timer), Chapter 12 (Ports), Chapter 13 (Melody Driver), and Chapter 15 (Shift Register).

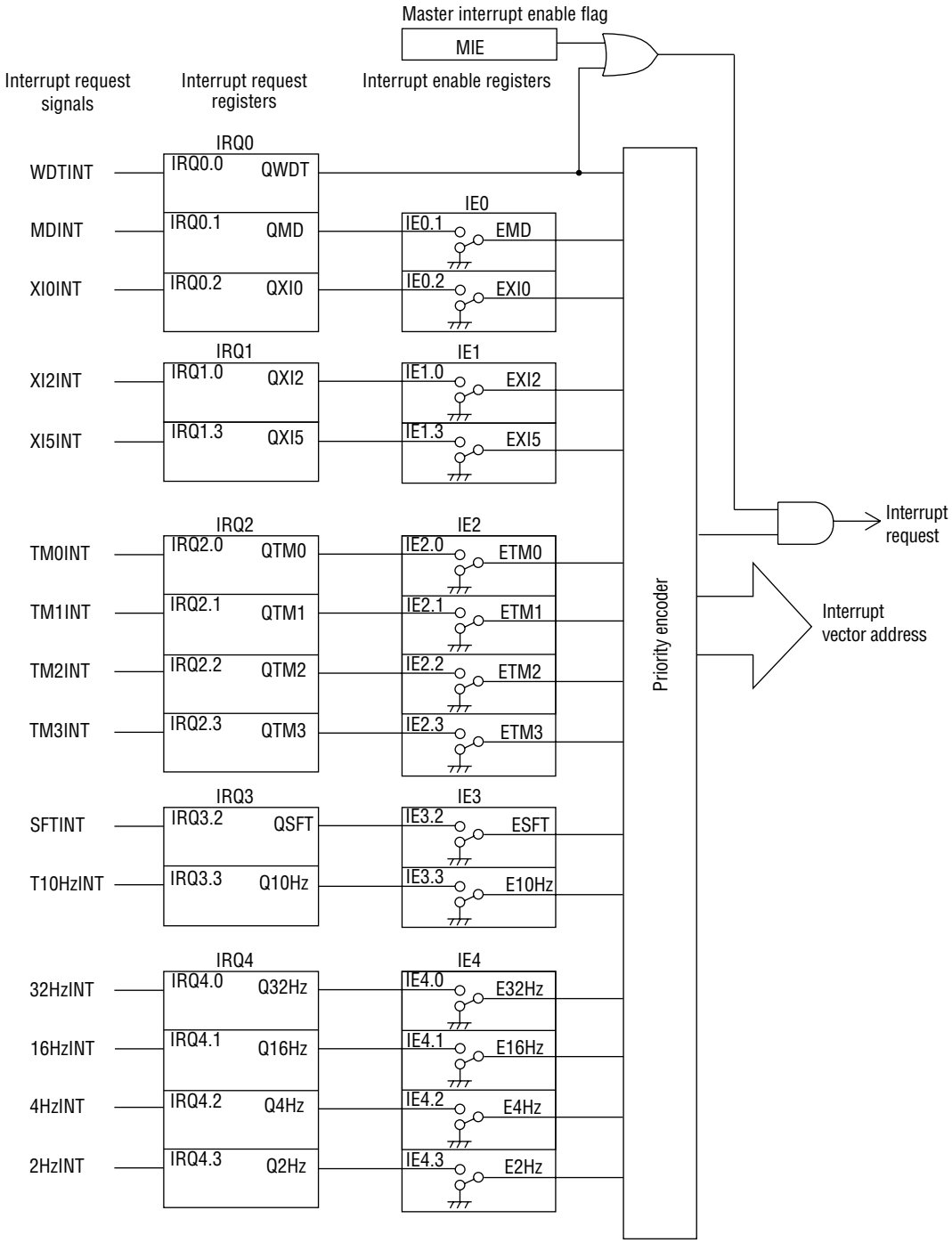


Figure 5-1 ML63189B Interrupt Control Equivalent Circuit

5.2 Interrupt Registers

The following three types of registers are used to control interrupts.

(1) Master interrupt enable register (MIEF)

(2) Interrupt enable registers (IE0 to IE4)

(3) Interrupt request registers (IRQ0 to IRQ4)

These registers are described below.

(1) Master interrupt enable register (MIEF)

MIEF is a 4-bit register in which bit 0 is the master interrupt enable flag (MIE).

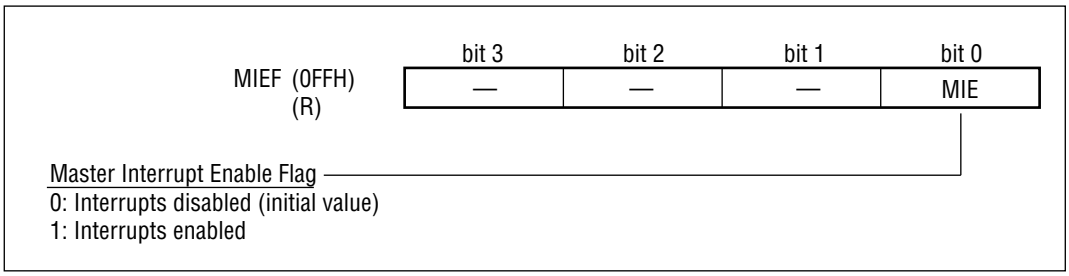
MIE (bit 0 of MIEF) is a flag that disables or enables all interrupts except for the watchdog timer interrupt.

If MIE is "0", all interrupts are disabled. If MIE is "1", all interrupts are enabled (with the exception of the watchdog timer).

When any interrupt is received, MIE is cleared to "0". MIE is set to "1" by execution of a return from interrupt instruction (RTI instruction).

If multi-level interrupt processing is to be performed, execute an RTI instruction (MIE←"1") during the interrupt processing routines.

At system reset, MIE is initialized to "0". MIEF only supports data reference (R) of data memory through addressing instructions.



Note:

When setting MIE, use "EI" instructions (MIE←"1") and "DI" instructions (MIE←"0").

(2) Interrupt enable registers (IE0 to IE4)

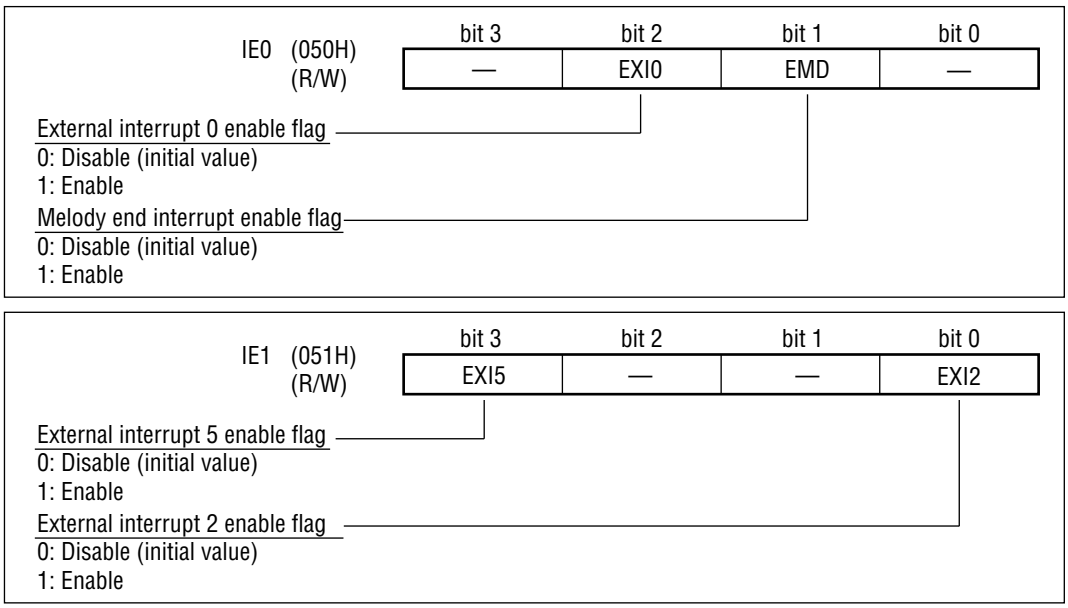
IE0, IE1, IE2, IE3, and IE4 are registers that consist of 4 bits each.

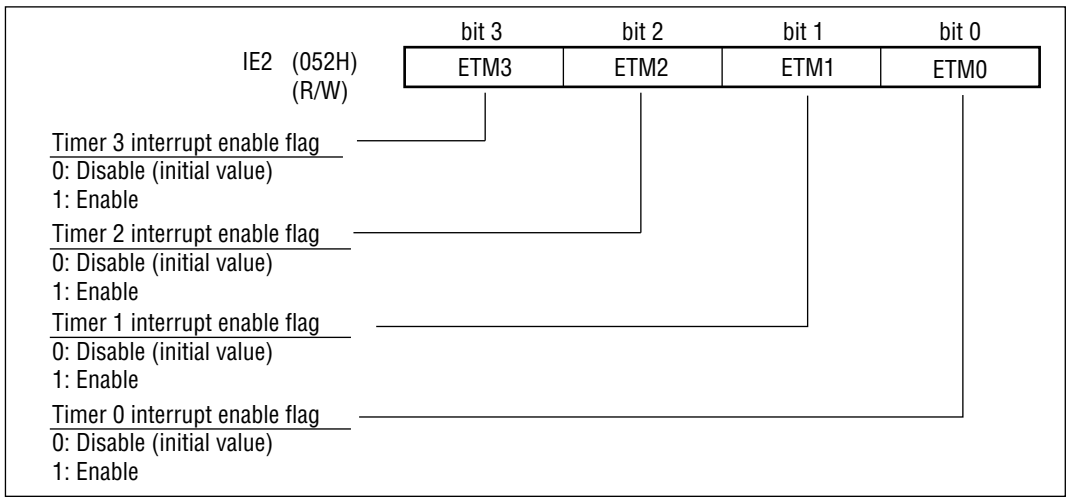
A logical AND of the corresponding bits of an interrupt enable register (IE0 to IE4) and an interrupt request register (IRQ0 to IRQ4) determines whether or not each interrupt request is issued to the CPU. The watchdog timer interrupt is non-maskable, and is therefore not dependent upon the interrupt enable registers (IE0 to IE4) and the master interrupt enable register (MIEF).

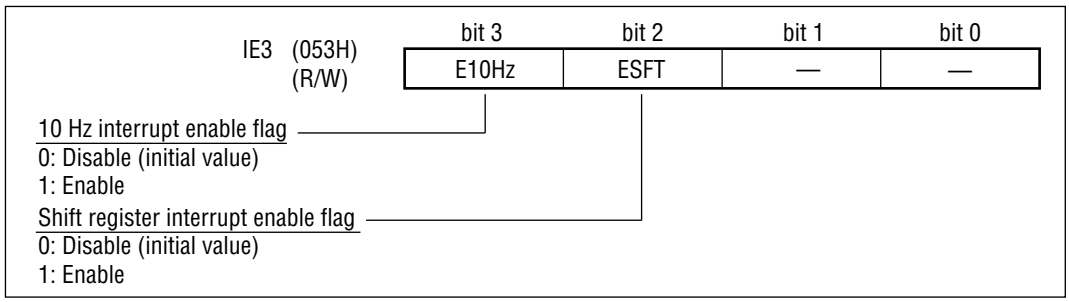
If multiple interrupts request the CPU at the same time, as shown in Table 5-1, the interrupts are accepted in order of highest priority and low priority interrupts are placed on hold.

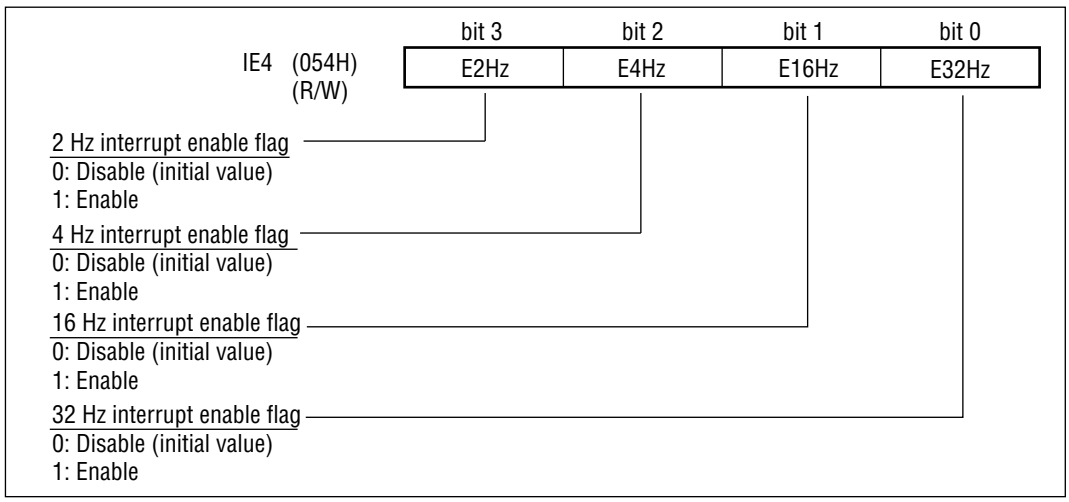
When an interrupt is received, the master interrupt enable flag (MIE) is cleared to "0". The corresponding bits in the interrupt enable registers (IE0 to IE4) do not change.

At system reset, each bit of IE0 through IE4 is initialized to "0".




IE2 (052H)
(R/W)
bit 3
bit 2
bit 1
bit 0
ETM3
ETM2
ETM1
ETM0
Timer 3 interrupt enable flag
0: Disable (initial value)
1: Enable
Timer 2 interrupt enable flag
0: Disable (initial value)
1: Enable
Timer 1 interrupt enable flag
0: Disable (initial value)
1: Enable
Timer 0 interrupt enable flag
0: Disable (initial value)
1: Enable


IE3 (053H)
(R/W)
bit 3
bit 2
bit 1
bit 0
E10Hz
ESFT
—
—
10 Hz interrupt enable flag
0: Disable (initial value)
1: Enable
Shift register interrupt enable flag
0: Disable (initial value)
1: Enable


IE4 (054H)
(R/W)
bit 3
bit 2
bit 1
bit 0
E2Hz
E4Hz
E16Hz
E32Hz
2 Hz interrupt enable flag
0: Disable (initial value)
1: Enable
4 Hz interrupt enable flag
0: Disable (initial value)
1: Enable
16 Hz interrupt enable flag
0: Disable (initial value)
1: Enable
32 Hz interrupt enable flag
0: Disable (initial value)
1: Enable

(3) Interrupt request registers (IRQ0 to IRQ4)

IRQ0, IRQ1, IRQ2, IRQ3 and IRQ4 are registers that consist of 4 bits each.

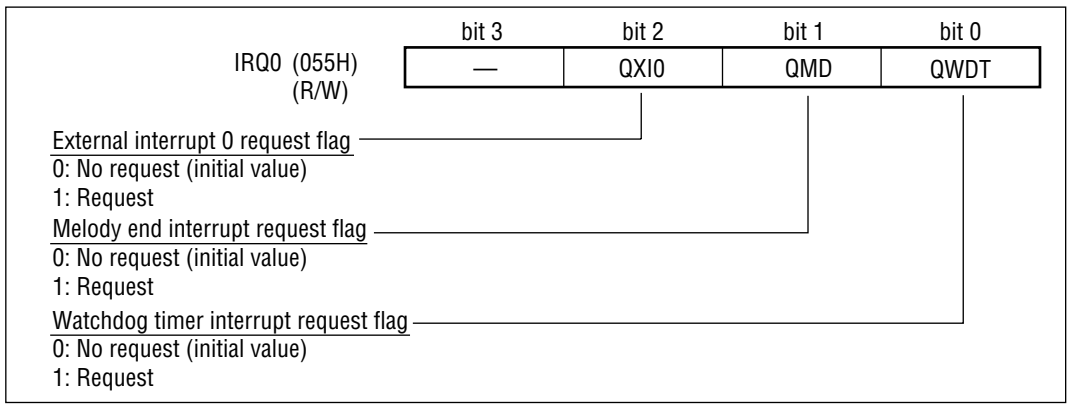
When an interrupt request is generated, the corresponding bit of the interrupt request register is set to "1" in the first half of the S1 state of the next instruction. So that the CPU can receive interrupt requests, set the master interrupt enable flag (MIE) to "1" and set the appropriate flag of the corresponding interrupt enable register (IE0 to IE4) to "1".

The watchdog timer interrupt is non-maskable and does not depend upon the interrupt enable register or the master interrupt enable register (MIEF).

Setting the appropriate bits of an interrupt request register to "1" allows software interrupts to be generated.

When an interrupt request is received, the corresponding bits of IRQ0 to IRQ4 are cleared to "0".

At system reset, each bit of IRQ0 through IRQ4 is initialized to "0".



bit 2: QXI0 (reQuest eXternal Interrupt 0)

The external interrupt 0 request flag.

The external interrupt 0 is assigned as the secondary function of each bit of port B (PB.0 to PB.3). External interrupt 0 requests are generated by a 4-bit ORed input.

bit 1: QMD (reQuest Melody Driver)

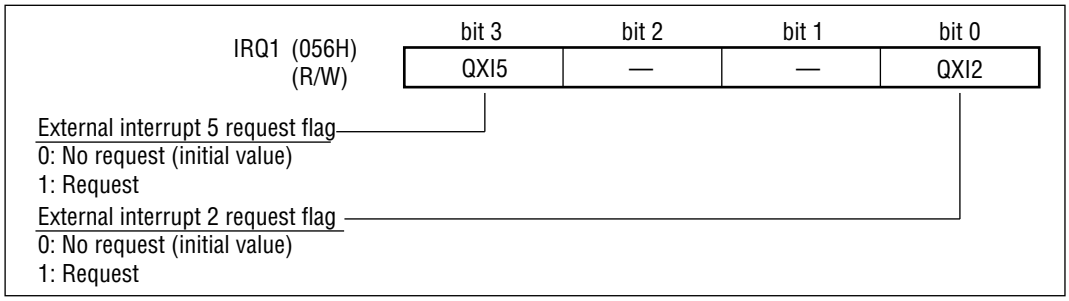
Melody end interrupt request flag.

Melody end interrupts are generated when the melody driver outputs the end note data (END bit = "1").

bit 0: QWDT (reQuest WatchDog Timer)

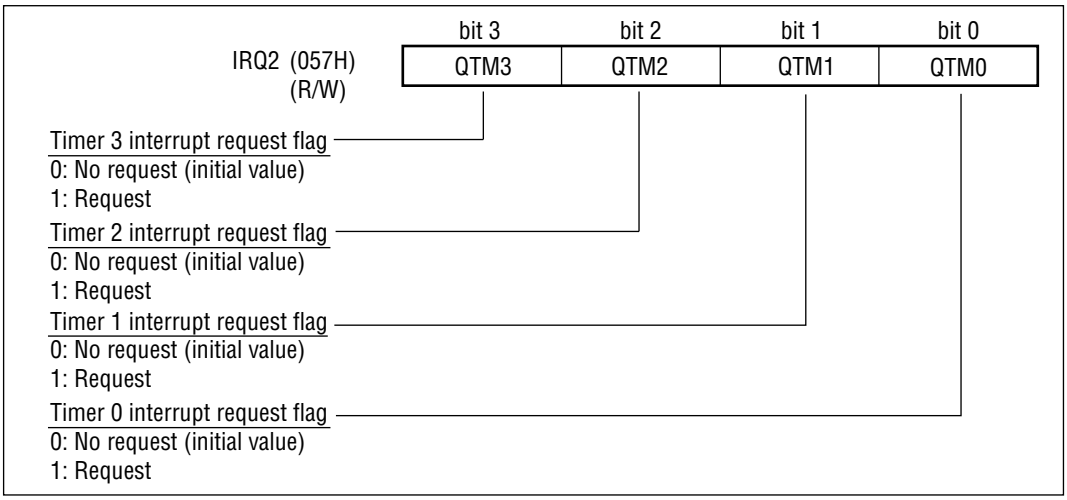
Watchdog timer interrupt request flag.

When the watchdog timer is started and then overflow occurs, an interrupt is requested. The watchdog timer interrupt is non-maskable and does not depend upon the interrupt enable registers or the master interrupt enable register (MIE).



bit 3: QXI5 (reQuest eXternal Interrupt 5)
External interrupt 5 request flag.
The external interrupt 5 is assigned as a secondary function to each bit (P0.0 to 0.3) of port 0.
An external interrupt request is generated through the 4-bit ORed input.

bit 0: QXI2 (reQuest eXternal Interrupt 2)
External interrupt 2 request flag.
The external interrupt 2 is assigned as a secondary function of port E.3 (PE.3).
Generation of the external interrupt 2 is triggered by the falling edge of the 128 Hz or 4 kHz output of the time base counter.

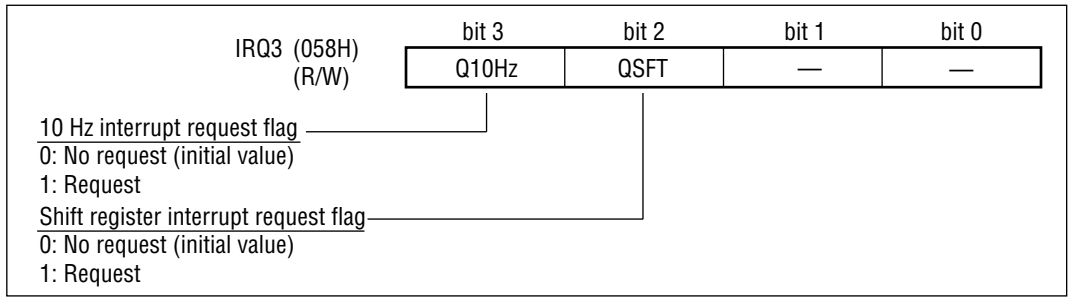


bit 3: QTM3 (reQuest TiMer 3)
Timer 3 interrupt request flag.
A timer 3 interrupt request is generated whenever timer 3 overflows.

bit 2: QTM2 (reQuest TiMer 2)
Timer 2 interrupt request flag.
A timer 2 interrupt request is generated whenever timer 2 overflows.

bit 1: QTM1 (reQuest TiMer 1)
Timer 1 interrupt request flag.
A timer 1 interrupt request is generated whenever timer 1 overflows.

bit 0: QTM0 (reQuest TiMer 0)
Timer 0 interrupt request flag.
A timer 0 interrupt request is generated whenever timer 0 overflows.



bit 3: Q10Hz (reQuest 10 Hz)

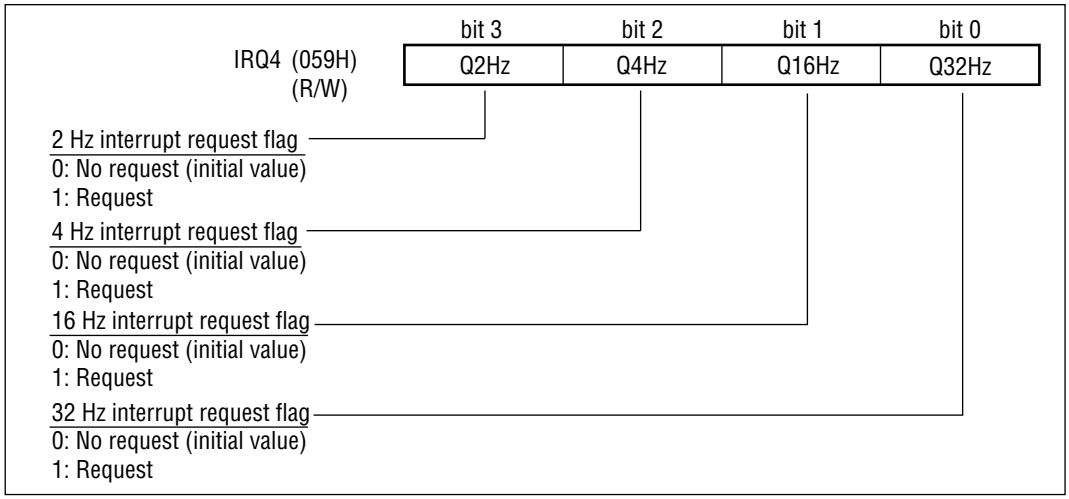
10 Hz interrupt request flag.

A 10 Hz interrupt request is generated whenever the 10 Hz carry generated by the 100 Hz timer counter is output.

bit 2: QSFT (reQuest ShiFT register)

Shift register interrupt request flag.

A shift register interrupt is generated when the 8-bit data transfer for the shift register is completed.



bit 3: Q2Hz (reQuest 2 Hz)

2 Hz interrupt request flag.

A 2 Hz interrupt request is generated at every falling edge of the 2 Hz output of the time base counter.

bit 2: Q4Hz (reQuest 4 Hz)

4 Hz interrupt request flag.

A 4 Hz interrupt request is generated at every falling edge of the 4 Hz output of the time base counter.

bit1: Q16Hz (reQuest 16 Hz)

16 Hz interrupt request flag.

A 16 Hz interrupt request is generated at every falling edge of the 16 Hz output of the time base counter.

bit 0: Q32Hz (reQuest 32 Hz)

32 Hz interrupt request flag.

A 32 Hz interrupt request is generated at every falling edge of the 32 Hz output of the time base counter.

5.3 Interrupt Sequence

5.3.1 Interrupt Processing

While MIE is "1", operation transfers to interrupt processing when individual interrupt factors are generated.

The watchdog timer interrupt is non-maskable and regardless of the MIE flag status, operation will shift to interrupt processing when the watchdog timer interrupt factor is generated.

The following processes are performed when an interrupt is generated.

(1) MIE and the corresponding interrupt request flag are cleared to "0".

(2) The program counter (PC) is saved on the call stack.

(3) The call stack pointer (SP) is incremented by 1. (SP←SP+1)

(4) The starting address of the interrupt routine is loaded into the program counter (PC).

Interrupt processing is performed in 0 machine cycles.

Figure 5-2 shows the stack contents after an interrupt is generated.

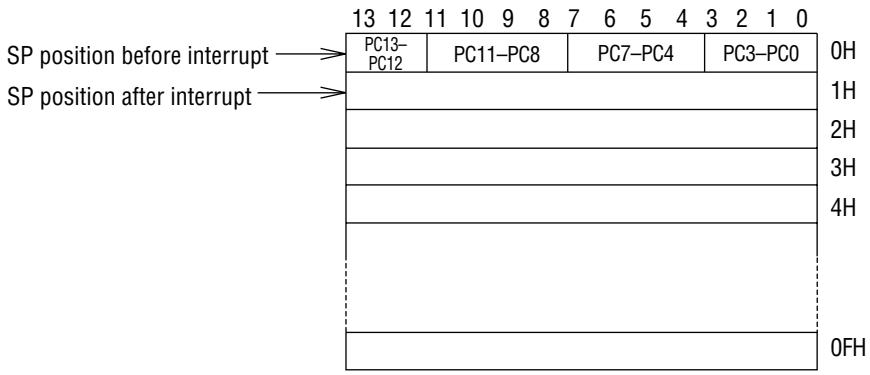


Figure 5-2 Call Stack Contents after Interrupt Generation

5.3.2 Return from an Interrupt Routine

Return from a watchdog timer interrupt routine is performed with an "RTNMI" instruction.

Return from all other interrupt routines is performed with an "RTI" instruction.

Execution of "RTI" and "RTNMI" instructions both require 1 machine cycle.

When returning from an interrupt routine, the CPU performs the following processes.

(1) The call stack pointer (SP) is decremented by 1. (SP←SP–1)

(2) MIE is set to "1" (when an "RTNMI" instruction is used, MIE is restored to its state prior to the interrupt).

(3) 1 is added to the call stack contents and that value is loaded into the program counter (PC).

Notes:

- While the MIE flag is "0" (interrupt disabled state), if a watchdog timer interrupt is processed and an "RTI" instruction is executed, the MIE flag will be set to "1" and interrupts enabled.
- Use "RTNMI" instructions to return from watchdog timer interrupts only. Use "RTI" instructions for normal interrupts.

5.3.3 Interrupt Hold Instructions

Interrupt requests are not received after execution of interrupt hold instruction.

The interrupt hold instructions follow.

- ROM table reference instructions
- Stack operation instructions
- Jump instructions
- Conditional branch instructions
- Call/return instructions
- "EI" (set MIE flag) instructions, "DI" (clear MIE flag) instructions and "MSA cadr15" (start melody output) instructions within control instructions

Note:

If interrupt hold instructions are used consecutively, even if an interrupt is generated, that interrupt may be put on hold for a considerable amount of time before the interrupt routine begins. Interrupt requests are received after execution of an instruction other than interrupt hold instructions.

Chapter 6

ML63193 Interrupt (INT193)

Chapter 6 ML63193 Interrupt (INT193)

6.1 Overview

The ML63193 supports 18 interrupt factors: 4 external interrupts and 14 internal interrupts.

With the exception of the watchdog timer interrupt, interrupt enable/disable is controlled by the master interrupt enable flag (MIE) and the individual interrupt enable registers (IE0 to IE4). Watchdog timer interrupt is a non-maskable interrupt.

When interrupt conditions are met, the interrupt routine is executed from the interrupt start address.

Table 6-1 indicates a list of interrupt factors, and Figure 6-1 shows the interrupt control equivalent circuit.

Table 6-1 ML63193 Interrupt Factors

Priority	Interrupt factor	Symbol	Interrupt start address
1	Watchdog timer interrupt	WDTINT	0010H
2	Melody end interrupt	MDINT	0012H
3	External interrupt 0 (PB 4-bit OR input)	XI0INT	0014H
4	External interrupt 1 (PC 4-bit OR input)	XI1INT	0016H
5	External interrupt 2 (PE.3)	XI2INT	0018H
6	External interrupt 5 (P0 4-bit OR input)	XI5INT	001EH
7	Timer 0 interrupt	TM0INT	0020H
8	Timer 1 interrupt	TM1INT	0022H
9	Timer 2 interrupt	TM2INT	0024H
10	Timer 3 interrupt	TM3INT	0026H
11	Serial port receive interrupt	SRINT	0028H
12	Serial port transmit interrupt	STINT	002AH
13	Shift register interrupt	SFTINT	002CH
14	T10 Hz interrupt	T10HzINT	002EH
15	32 Hz interrupt	32HzINT	0030H
16	16 Hz interrupt	16HzINT	0032H
17	4 Hz interrupt	4HzINT	0034H
18	2 Hz interrupt	2HzINT	0036H

If multiple interrupts are detected simultaneously, the lowest interrupt start address is given priority.

For details on interrupt operation, refer to Chapter 8 (Time Base Counter), Chapter 9 (Timers), Chapter 10 (100 Hz Timer Counter), Chapter 11 (Watchdog Timer), Chapter 12 (Ports), Chapter 13 (Melody Driver), Chapter 14 (Serial Port), and Chapter 15 (Shift Register).

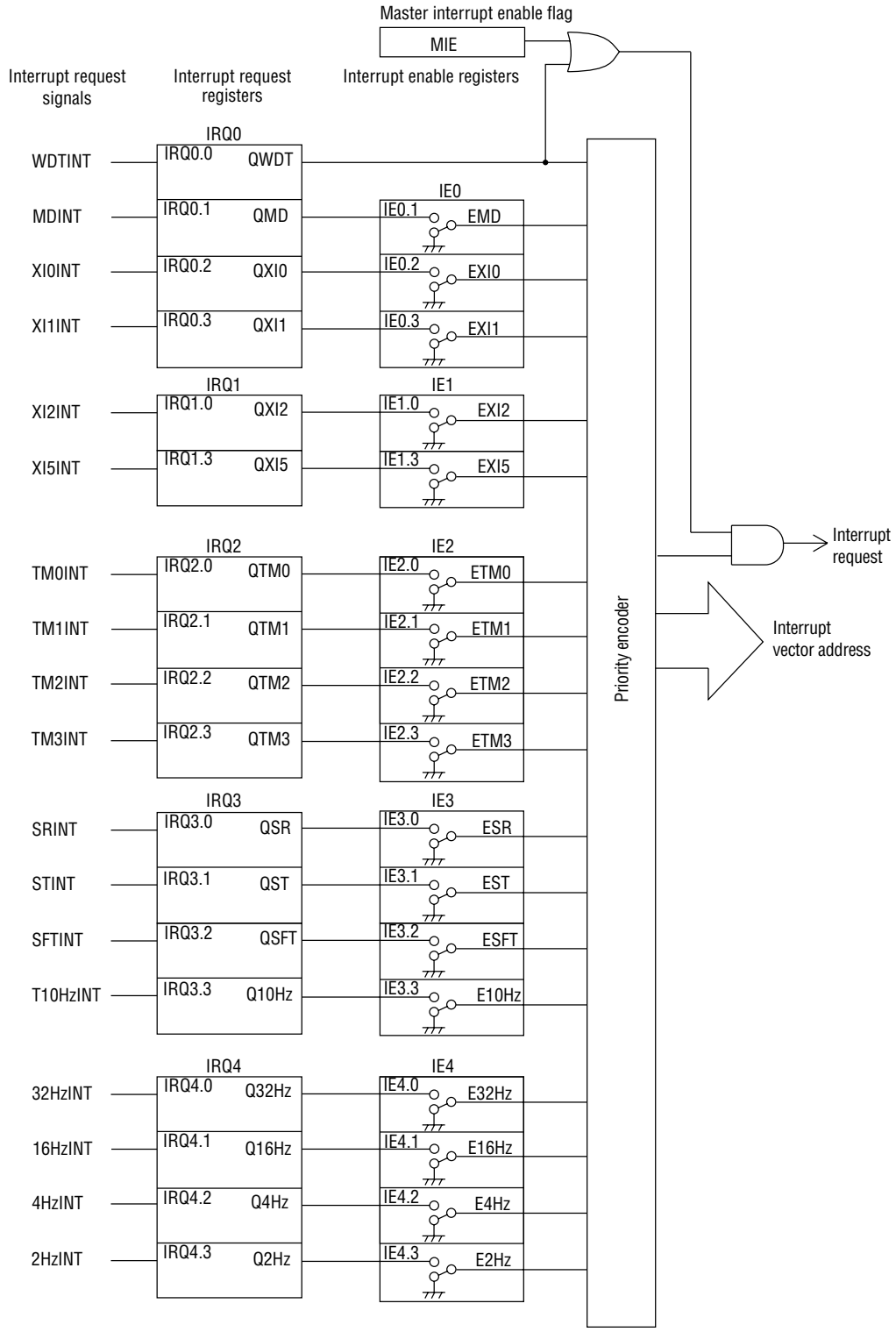


Figure 6-1 ML63193 Interrupt Control Equivalent Circuit

6.2 Interrupt Registers

The following three types of registers are used to control interrupts.

(1) Master interrupt enable register (MIEF)

(2) Interrupt enable registers (IE0 to IE4)

(3) Interrupt request registers (IRQ0 to IRQ4)

These registers are described below.

(1) Master interrupt enable register (MIEF)

MIEF is a 4-bit register in which bit 0 is the master interrupt enable flag (MIE).

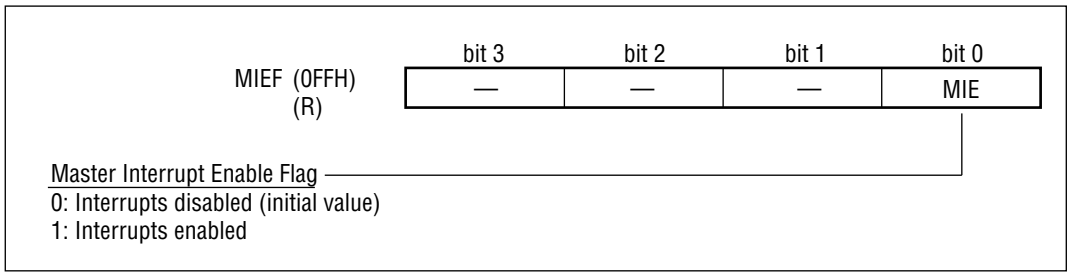
MIE (bit 0 of MIEF) is a flag that disables or enables all interrupts except for the watchdog timer interrupt.

If MIE is "0", all interrupts are disabled. If MIE is "1", all interrupts are enabled (with the exception of the watchdog timer).

When any interrupt is received, MIE is cleared to "0". MIE is set to "1" by execution of a return from interrupt instruction (RTI instruction).

If multi-level interrupt processing is to be performed, execute an RTI instruction (MIE←"1") during the interrupt processing routines.

At system reset, MIE is initialized to "0". MIEF only supports data reference (R) of data memory through addressing instructions.



Note:

When setting MIE, use "EI" instructions (MIE←"1") and "DI" instructions (MIE←"0").

(2) Interrupt enable registers (IE0 to IE4)

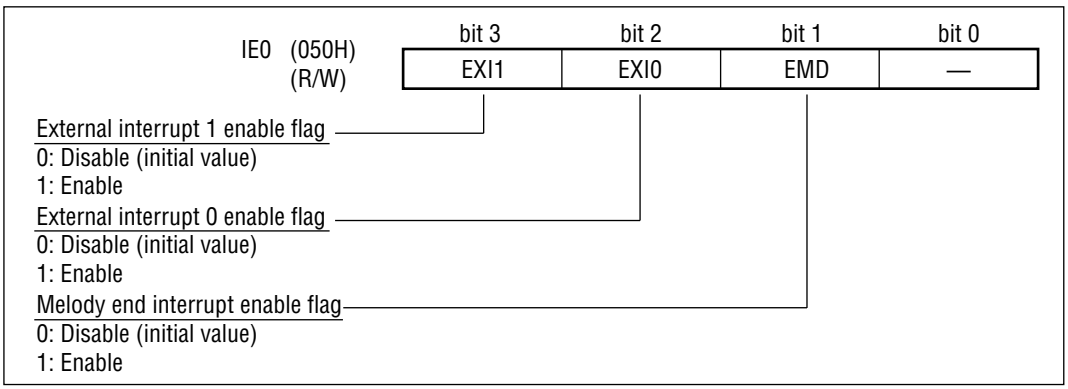
IE0, IE1, IE2, IE3, and IE4 are registers that consist of 4 bits each.

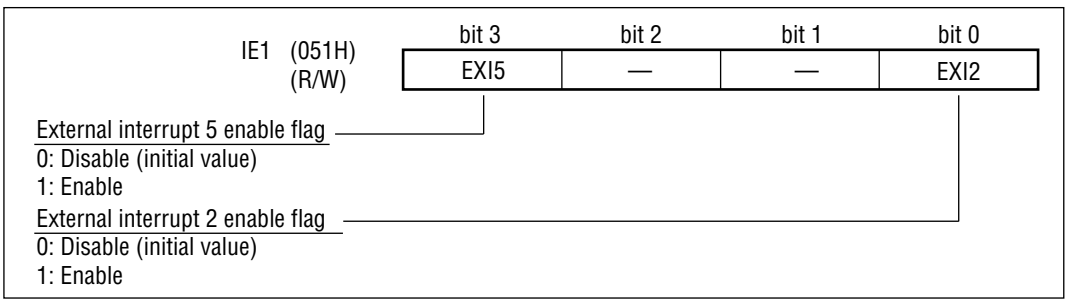
A logical AND of the corresponding bits of an interrupt enable register (IE0 to IE4) and an interrupt request register (IRQ0 to IRQ4) determines whether or not each interrupt request is issued to the CPU. The watchdog timer interrupt is non-maskable, and is therefore not dependent upon the interrupt enable registers (IE0 to IE4) and the master interrupt enable register (MIEF).

If multiple interrupts request the CPU at the same time, as shown in Table 6-1, the interrupts are accepted in order of highest priority and low priority interrupts are placed on hold.

When an interrupt is received, the master interrupt enable flag (MIE) is cleared to "0". The corresponding bits in the interrupt enable registers (IE0 to IE4) do not change.

At system reset, each bit of IE0 through IE4 is initialized to "0".





IE2 (052H) (R/W)

bit 3	bit 2	bit 1	bit 0
ETM3	ETM2	ETM1	ETM0

Timer 3 interrupt enable flag
0: Disable (initial value)
1: Enable

Timer 2 interrupt enable flag
0: Disable (initial value)
1: Enable

Timer 1 interrupt enable flag
0: Disable (initial value)
1: Enable

Timer 0 interrupt enable flag
0: Disable (initial value)
1: Enable

IE3 (053H) (R/W)

bit 3	bit 2	bit 1	bit 0
E10Hz	ESFT	EST	ESR

10 Hz interrupt enable flag
0: Disable (initial value)
1: Enable

Shift register interrupt enable flag
0: Disable (initial value)
1: Enable

Serial port transmit interrupt enable flag
0: Disable (initial value)
1: Enable

Serial port receive interrupt enable flag
0: Disable (initial value)
1: Enable

IE4 (054H) (R/W)

bit 3	bit 2	bit 1	bit 0
E2Hz	E4Hz	E16Hz	E32Hz

2 Hz interrupt enable flag
0: Disable (initial value)
1: Enable

4 Hz interrupt enable flag
0: Disable (initial value)
1: Enable

16 Hz interrupt enable flag
0: Disable (initial value)
1: Enable

32 Hz interrupt enable flag
0: Disable (initial value)
1: Enable

(3) Interrupt request registers (IRQ0 to IRQ4)

IRQ0, IRQ1, IRQ2, IRQ3 and IRQ4 are registers that consist of 4 bits each.

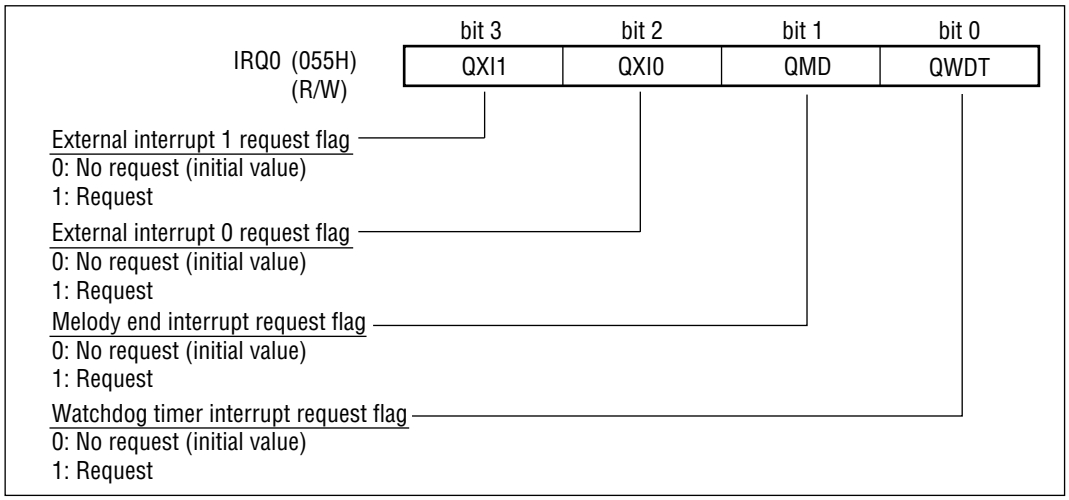
When an interrupt request is generated, the corresponding bit of the interrupt request register is set to "1" in the first half of the S1 state of the next instruction. So that the CPU can receive interrupt requests, set the master interrupt enable flag (MIE) to "1" and set the appropriate flag of the corresponding interrupt enable register (IE0 to IE4) to "1".

The watchdog timer interrupt is non-maskable and does not depend upon the interrupt enable register or the master interrupt enable register (MIEF).

Setting the appropriate bits of an interrupt request register to "1" allows software interrupts to be generated.

When an interrupt request is received, the corresponding bits of IRQ0 to IRQ4 are cleared to "0".

At system reset, each bit of IRQ0 through IRQ4 is initialized to "0".



bit 3: QXI1 (reQuest eXternal Interrupt 1)

The external interrupt 1 request flag.

The external interrupt 1 is assigned as the secondary function of each bit of port C (PC.0 to PC.3). External interrupt 1 requests are generated by a 4-bit ORed input.

bit 2: QXI0 (reQuest eXternal Interrupt 0)

The external interrupt 0 request flag.

The external interrupt 0 is assigned as the secondary function of each bit of port B (PB.0 to PB.3). External interrupt 0 requests are generated by a 4-bit ORed input.

bit 1: QMD (reQuest Melody Driver)

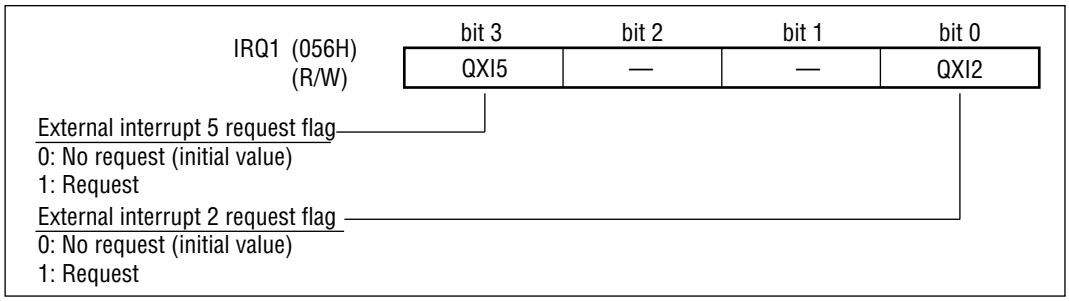
Melody end interrupt request flag.

Melody end interrupts are generated when the melody driver outputs the end note data (END bit = "1").

bit 0: QWDT (reQuest WatchDog Timer)

Watchdog timer interrupt request flag.

When the watchdog timer is started and then overflow occurs, an interrupt is requested. The watchdog timer interrupt is non-maskable and does not depend upon the interrupt enable registers or the master interrupt enable register (MIE).



bit 3: QXI5 (reQuest eXternal Interrupt 5)

External interrupt 5 request flag.

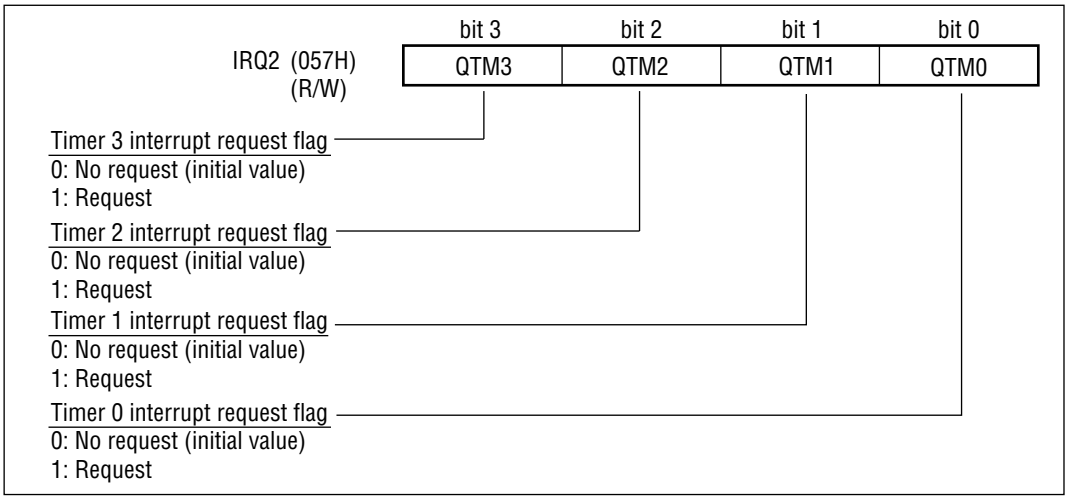
The external interrupt 5 is assigned as a secondary function to each bit (P0.0 to 0.3) of port 0.

An external interrupt request is generated through the 4-bit ORed input.

bit 0: QXI2 (reQuest eXternal Interrupt 2)

External interrupt 2 request flag.

The external interrupt 2 is assigned as a secondary function of port E.3 (PE.3). Generation of the external interrupt 2 is triggered by the falling edge of the 128 Hz or 4 kHz output of the time base counter.

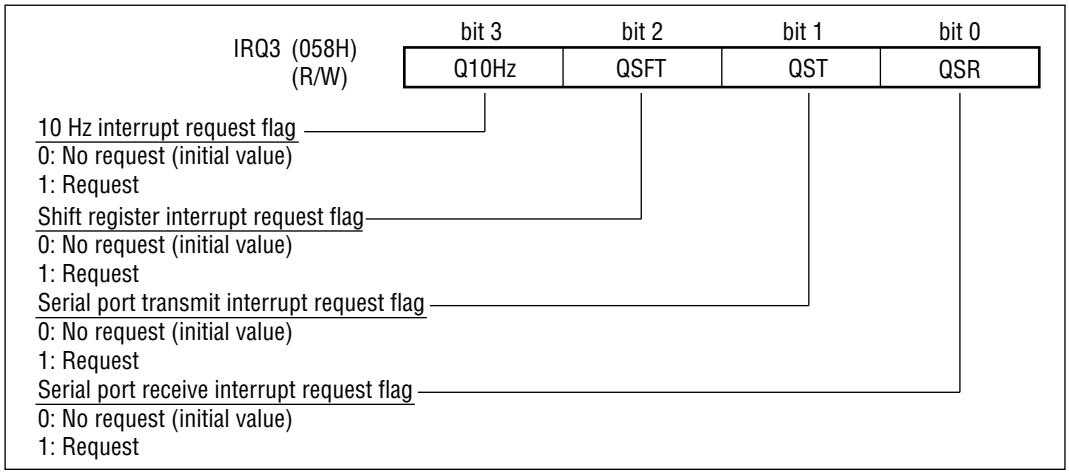


bit 3: QTM3 (reQuest TiMer 3)
Timer 3 interrupt request flag.
A timer 3 interrupt request is generated whenever timer 3 overflows.

bit 2: QTM2 (reQuest TiMer 2)
Timer 2 interrupt request flag.
A timer 2 interrupt request is generated whenever timer 2 overflows.

bit 1: QTM1 (reQuest TiMer 1)
Timer 1 interrupt request flag.
A timer 1 interrupt request is generated whenever timer 1 overflows.

bit 0: QTM0 (reQuest TiMer 0)
Timer 0 interrupt request flag.
A timer 0 interrupt request is generated whenever timer 0 overflows.



bit 3: Q10Hz (reQuest 10 Hz)

10 Hz interrupt request flag.

A 10 Hz interrupt request is generated whenever the 10 Hz carry generated by the 100 Hz timer counter is output.

bit 2: QSFT (reQuest ShiFT register)

Shift register interrupt request flag.

A shift register interrupt is generated when the 8-bit data transfer for the shift register is completed.

bit 1: QST

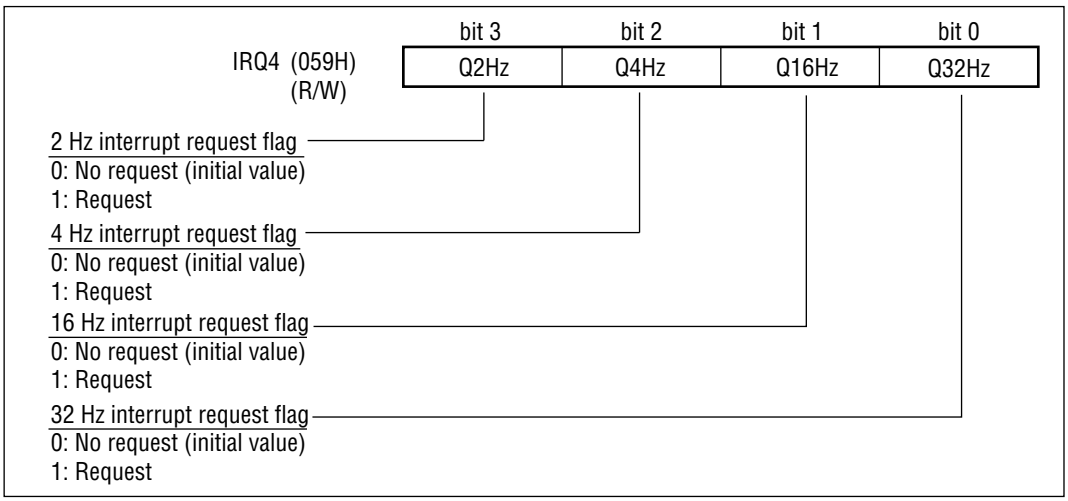
Serial port transmit interrupt request flag.

A serial port ransmit interrupt request is generated when a serial port transmit operation is completed.

bit 0: QSR

Serial port receive interrupt request flag.

A serial port receive interrupt is generated when a serial port receive operation is completed.



bit 3: Q2Hz (reQuest 2 Hz)

2 Hz interrupt request flag.

A 2 Hz interrupt request is generated at every falling edge of the 2 Hz output of the time base counter.

bit 2: Q4Hz (reQuest 4 Hz)

4 Hz interrupt request flag.

A 4 Hz interrupt request is generated at every falling edge of the 4 Hz output of the time base counter.

bit1: Q16Hz (reQuest 16 Hz)

16 Hz interrupt request flag.

A 16 Hz interrupt request is generated at every falling edge of the 16 Hz output of the time base counter.

bit 0: Q32Hz (reQuest 32 Hz)

32 Hz interrupt request flag.

A 32 Hz interrupt request is generated at every falling edge of the 32 Hz output of the time base counter.

6.3 Interrupt Sequence

6.3.1 Interrupt Processing

While MIE is "1", operation transfers to interrupt processing when individual interrupt factors are generated.

The watchdog timer interrupt is non-maskable and regardless of the MIE flag status, operation will shift to interrupt processing when the watchdog timer interrupt factor is generated.

The following processes are performed when an interrupt is generated.

(1) MIE and the corresponding interrupt request flag are cleared to "0".

(2) The program counter (PC) is saved on the call stack.

(3) The call stack pointer (SP) is incremented by 1. (SP←SP+1)

(4) The starting address of the interrupt routine is loaded into the program counter (PC).

Interrupt processing is performed in 0 machine cycles.

Figure 6-2 shows the stack contents after an interrupt is generated.

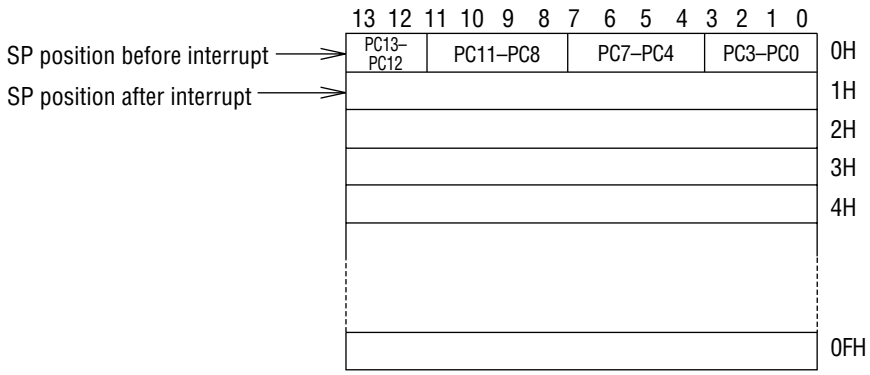


Figure 6-2 Call Stack Contents after Interrupt Generation

6.3.2 Return from an Interrupt Routine

Return from a watchdog timer interrupt routine is performed with an "RTNMI" instruction.

Return from all other interrupt routines is performed with an "RTI" instruction.

Execution of "RTI" and "RTNMI" instructions both require 1 machine cycle.

When returning from an interrupt routine, the CPU performs the following processes.

(1) The call stack pointer (SP) is decremented by 1. (SP←SP–1)

(2) MIE is set to "1" (when an "RTNMI" instruction is used, MIE is restored to its state prior to the interrupt).

(3) 1 is added to the call stack contents and that value is loaded into the program counter (PC).

Notes:

- While the MIE flag is "0" (interrupt disabled state), if a watchdog timer interrupt is processed and an "RTI" instruction is executed, the MIE flag will be set to "1" and interrupts enabled.
- Use "RTNMI" instructions to return from watchdog timer interrupts only. Use "RTI" instructions for normal interrupts.

6.3.3 Interrupt Hold Instructions

Interrupt requests are not received after execution of interrupt hold instruction.

The interrupt hold instructions follow.

- ROM table reference instructions
- Stack operation instructions
- Jump instructions
- Conditional branch instructions
- Call/return instructions
- "EI" (set MIE flag) instructions, "DI" (clear MIE flag) instructions and "MSA cadr15" (start melody output) instructions within control instructions

Note:

If interrupt hold instructions are used consecutively, even if an interrupt is generated, that interrupt may be put on hold for a considerable amount of time before the interrupt routine begins. Interrupt requests are received after execution of an instruction other than interrupt hold instructions.

Chapter 7

Clock Generator Circuit (OSC)

Chapter 7 Clock Generator Circuit (OSC)

7.1 Overview

The clock generator circuit (OSC) consists of a low-speed clock generator circuit, a high-speed clock generator circuit and a clock controller unit. The clock generator circuit generates the system clock (CLK), time base clock (TBCCLK) and the high-speed clock (HSCLK).

The following modes can be selected for the low-speed clock generator circuit and the high-speed clock generator circuit.

- Low-speed clock generator circuit: crystal oscillation mode or RC oscillation mode (mask option selection)
- High-speed clock generator circuit: ceramic oscillation mode or RC oscillation mode (software selection)

The system clock is the basic operation clock for the CPU. The time base clock is the basic operation clock for the time base counter.

Depending on the contents of the frequency control register (FCON), the system clock frequency is switched to either the output of the low-speed clock oscillation circuit (TBCCLK) or the output of the high-speed clock oscillation circuit (HSCLK).

The frequency control register (FCON) also controls modes of the high-speed clock oscillation circuit.

7.2 Clock Generator Circuit Configuration

Figure 7-1 shows a block diagram of the clock generator circuit.

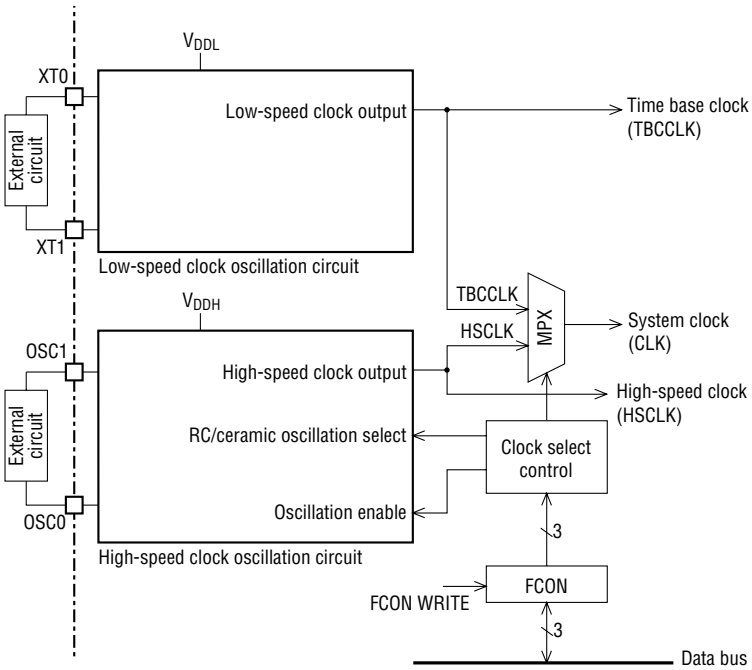


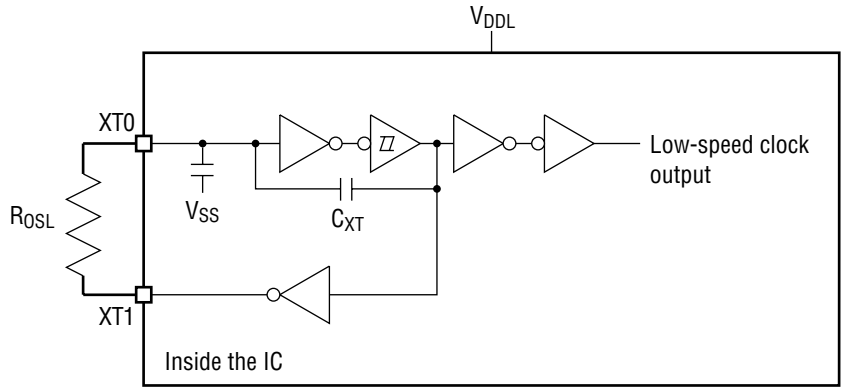
Figure 7-1 Clock Generator Circuit Configuration

7.3 Low-Speed Clock Generator Circuit

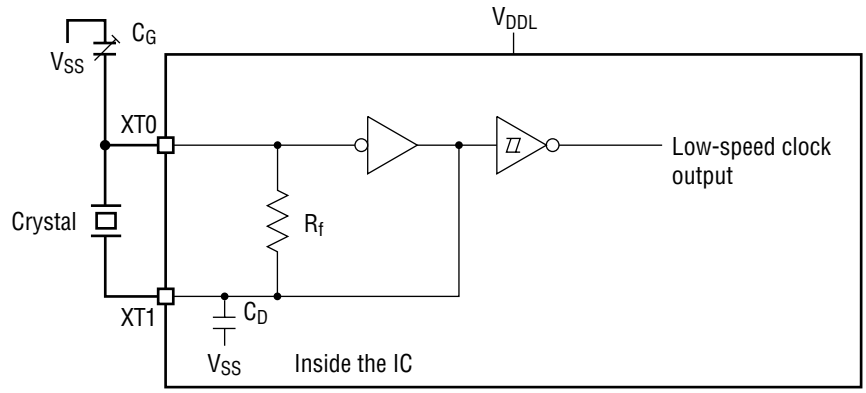
The low-speed clock generator circuit has two modes that are selected by the mask option, the RC oscillation mode and crystal oscillation mode. The oscillation frequency is 30 to 80 kHz.

For the RC oscillation mode, attach an external resistor, R_{OSL}, as shown in Figure 7-2(a).

For the crystal oscillation mode, attach an external crystal unit and capacitor, C_G, as shown in Figure 7-2(b).



(a) External Circuit for RC Oscillation Mode



(b) External Circuit for Crystal Oscillation Mode

Figure 7-2 External Circuits for Low-Speed Clock Oscillation

Note:

For convenience, the descriptions of this manual assume that a 32.768 kHz crystal unit is used in the low-speed clock oscillation circuit.

For the method of specifying mask options for the low-speed clock oscillation circuit, see "Appendix G: Mask Option."

Table 7-1 lists typical values of oscillation frequency when the low-speed side RC oscillation mode is selected. Table 7-2 shows an example external component to be attached when the low-speed side crystal oscillation mode is selected.

Table 7-1 Typical Oscillation Frequencies for the Low-Speed Side RC Oscillation Mode

R_{OSL}	f_{ROSL}
1.5 MΩ	32 kHz ±30%
700 kΩ	60 kHz ±30%
500 kΩ	80 kHz ±30%

Table 7-2 Example External Component for the Low-Speed Side Crystal Oscillation Mode

C_G	f_{XT}
12 pF	32.768 kHz

7.4 High-Speed Clock Generator Circuit

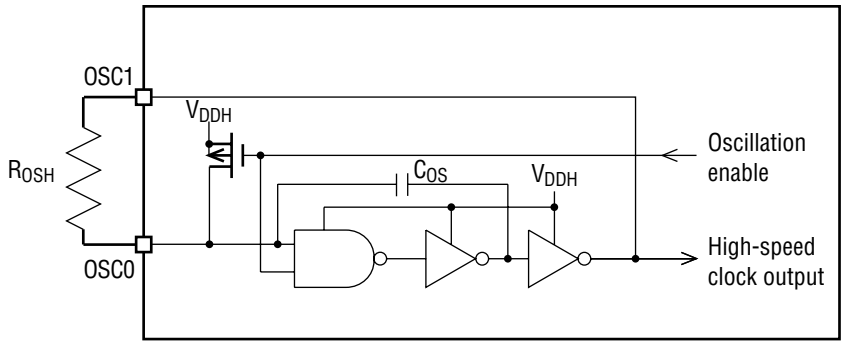
The high-speed clock generator circuit has two modes, the RC oscillation mode and ceramic oscillation mode. Oscillation modes are set by OSCSEL (bit 2 of FCON). The maximum oscillation frequency is 2 MHz.

- OSCSEL = "0" : RC oscillation mode
- OSCSEL = "1" : ceramic oscillation mode

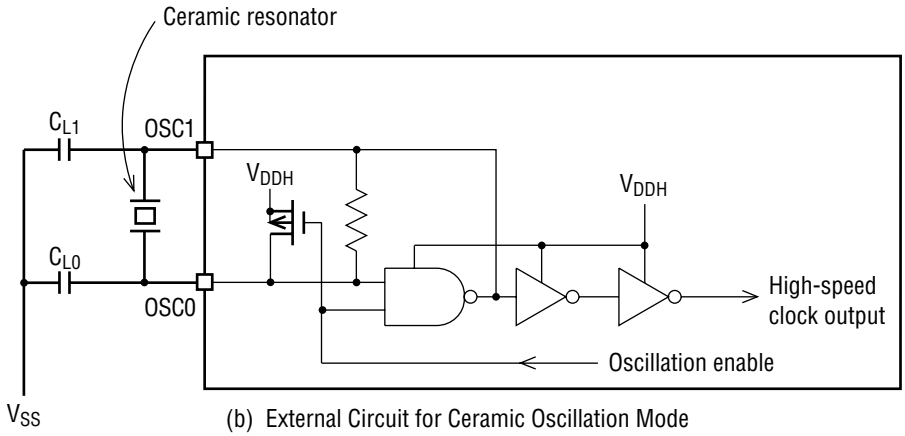
If the high-speed clock is not to be used, leave the OSC0 and OSC1 pins open (unconnected).

For the RC oscillation mode, attach an external resistor, R_{OSH}, as shown in Figure 7-3(a).

For the ceramic oscillation mode, attach an external ceramic unit and capacitors as shown in Figure 7-3(b).



(a) External Circuit for RC Oscillation Mode



(b) External Circuit for Ceramic Oscillation Mode

Figure 7-3 External Circuits for High-Speed Clock Oscillation

Table 7-3 lists typical values of oscillation frequency when the high-speed side RC oscillation mode is selected. Table 7-4 lists example external components to be attached when the high-speed side ceramic oscillation mode is selected.

Table 7-3 Typical Oscillation Frequencies for the High-Speed Side RC Oscillation Mode

R_{OSH} (kΩ)	V_{DD} (V)	Backup flag	f_{ROSH}
400	1.5	ON	200 kHz ±30%
100			700 kHz ±30%
75			1 MHz ±30%
100	3.0	OFF	700 kHz ±30%
75			1 MHz ±30%
51			1.35 MHz ±30%
30			2 MHz ±30%

Table 7-4 Example External Components for the High-Speed Side Ceramic Oscillation Mode

C_{L0} (pF)	C_{L1} (pF)	Ceramic unit
330	330	CSB200D (200 kHz)*
220	220	CSB300D (300 kHz)*
150	150	CSB500E (500 kHz)*
68	68	CSB1000J (1 MHz)*
30	30	CSA2.00MG (2 MHz)*

* Ceramic unit manufactured by Murata MFG. Co., Ltd.

7.5 System Clock Control

The system clock is the basic operation clock of the CPU.

The clock can be selected as follows with the CPUCLK (bit 0 of FCON) setting.

- CPUCLK = "0" (initial value)

  The output of the low-speed clock generator circuit (TBCCLK) is the system clock.

- CPUCLK = "1"

  The output of the high-speed clock generator circuit (HSCLK) is the system clock.

When HSCLK is selected as the system clock, the high-speed clock must be in the oscillating state (ENOSC = "1"). The crystal generator circuit will continue to oscillate even when the high-speed generator circuit is selected.

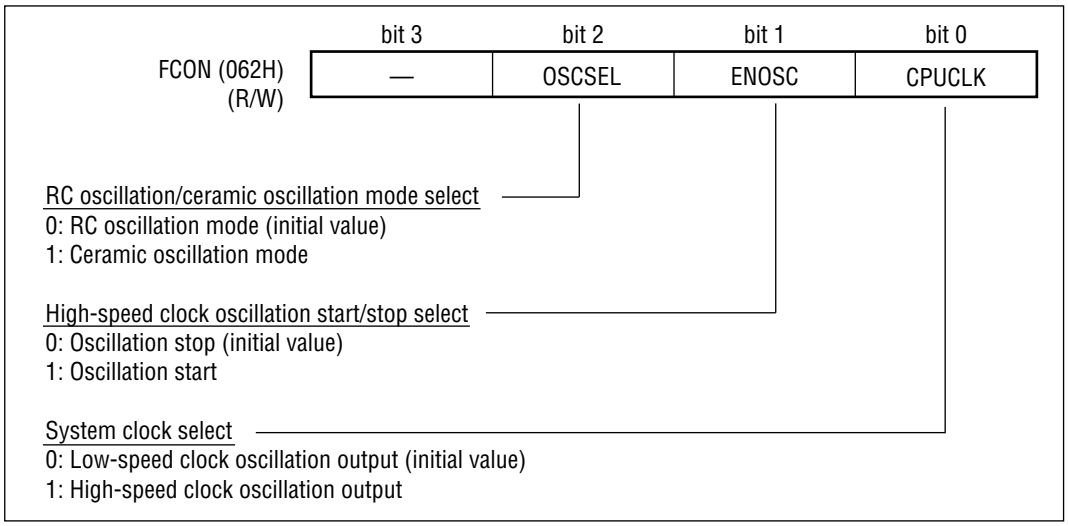
To reduce the total power consumption in applications that use the high-speed clock generator circuit, the following clock controls are generally implemented in software.

- During normal operation, the output of the low-speed clock generator circuit (CPUCLK = "0") should be the system clock.
- Only when high-speed operation is necessary should the high-speed clock oscillate (ENOSC = "1") and output of the high-speed clock generator circuit (CPUCLK = "1") should be selected.

For details of the system clock select timing, refer to section 7.7, "System Clock Select Timing."

7.6 Frequency Control Register (FCON)

FCON is a special function register (SFR) that selects the system clock.



bit 2: OSCSEL

This bit selects the RC oscillation mode or the ceramic oscillation mode of the high-speed clock generator circuit. At system reset, this bit is cleared to "0", selecting the RC oscillation mode.

bit 1: ENOSC

This bit starts and stops oscillation of the high-speed clock generator circuit. At system reset, this bit is cleared to "0", stopping oscillation of the high-speed clock generator circuit.

bit 0: CPUCLK

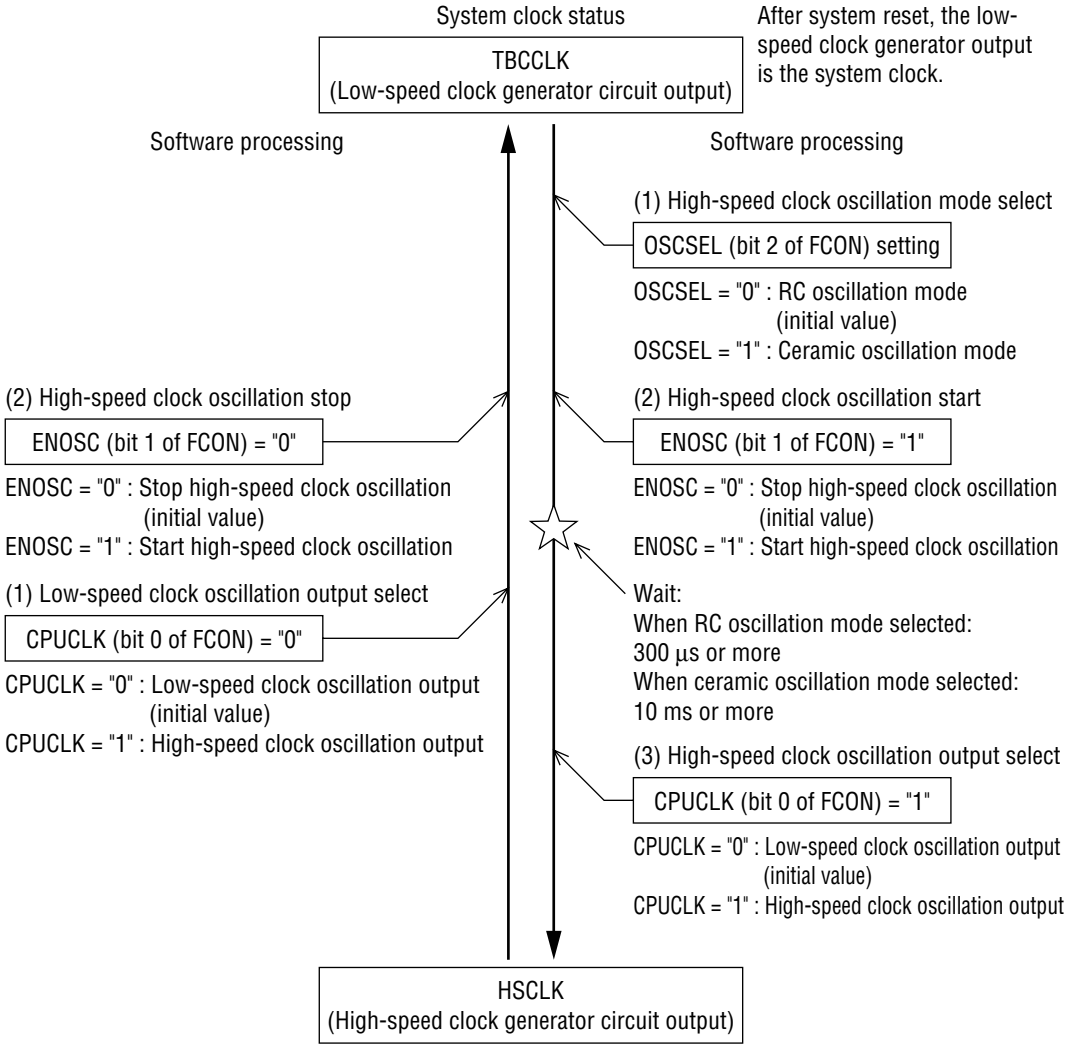
This bit selects the system clock, the basic operation clock of the CPU. At system reset, this bit is cleared to "0", selecting output of the low-speed clock generator circuit (TBCCLK).

7.7 System Clock Select Timing

After system reset, the system clock is TBCCLK.

When high-speed operation is necessary, switch the system clock to HSCLK.

A flowchart of system clock operation is shown below.



When ENOSC (bit 1 of FCON) is set to "1", oscillation starts in the mode selected by OSCSEL. At the same time, the internal logic power supply (V_{DDL}) switches from the constant voltage circuit output level (approx. 1.5 V) to the V_{DDH} level. Next, if CPUCLK is set to "1", the system clock switches from crystal oscillation output (TBCCLK) to high-speed clock output (HSCLK).

Figure 7-4 shows the system clock select timing and status of the internal logic power supply (V_{DDL}).

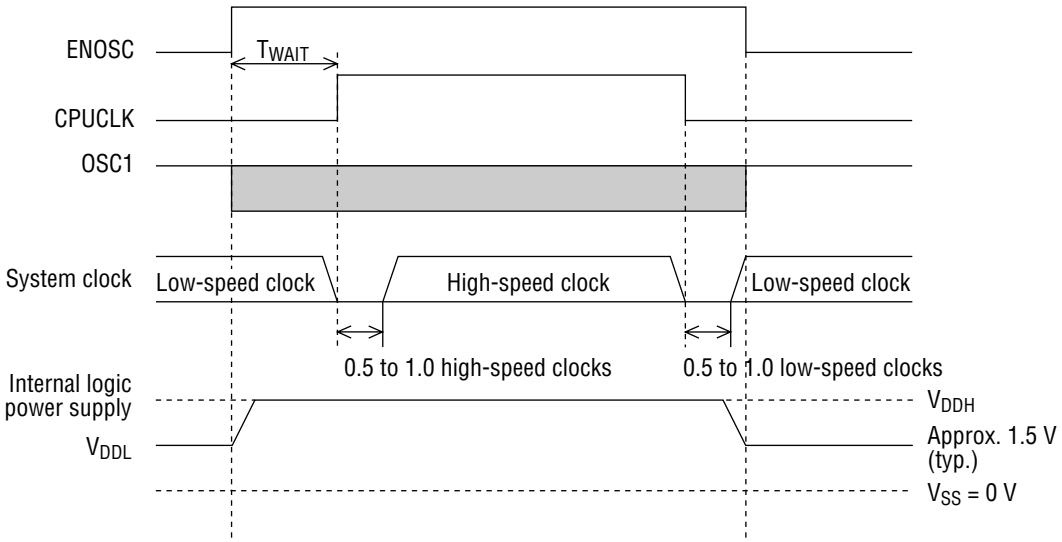


Figure 7-4 System Clock Select Timing

In the ceramic oscillation mode, 10 ms are required from the time when ENOSC is set to "1" until the high-speed clock generator circuit enters the oscillating state. Therefore, in this mode, when switching CPUCLK to a high-speed setting, wait for an interval of at least T_{WAIT} = 10 ms after the rising edge of ENOSC.

In the CR oscillation mode, oscillation begins soon after setting ENOSC to "1". When switching CPUCLK to a high-speed setting, wait for an interval of at least T_{WAIT} = 300 µs after the rising edge of ENOSC.

When switching from the high-speed mode to the low-speed mode, set the CPUCLK bit to "0", and sometime after the next instruction, set the ENOSC bit to "0".

For details regarding the constant voltage circuit for the internal logic power supply, refer to Chapter 19, "Backup Circuit."

Chapter 8

Time Base Counter (TBC)

Chapter 8 Time Base Counter (TBC)

8.1 Overview

The time base counter (TBC) is a 15-bit internal counter, which generates the clock supplied to internal peripheral functions.

The TBC clock is a time base clock (TBCCLK).

TBC outputs are used for functions such as time base interrupts and various other circuits. TBC8–11 and TBC12–15 can be read/reset by software.

The TBC generates an interrupt request at the falling edge of 32 Hz/16 Hz/4 Hz/2 Hz output.

The TBC is initialized to 0000H at system reset.

8.2 Time Base Counter Configuration

The configuration of the time base counter (TBC) is shown in Figure 8-1.

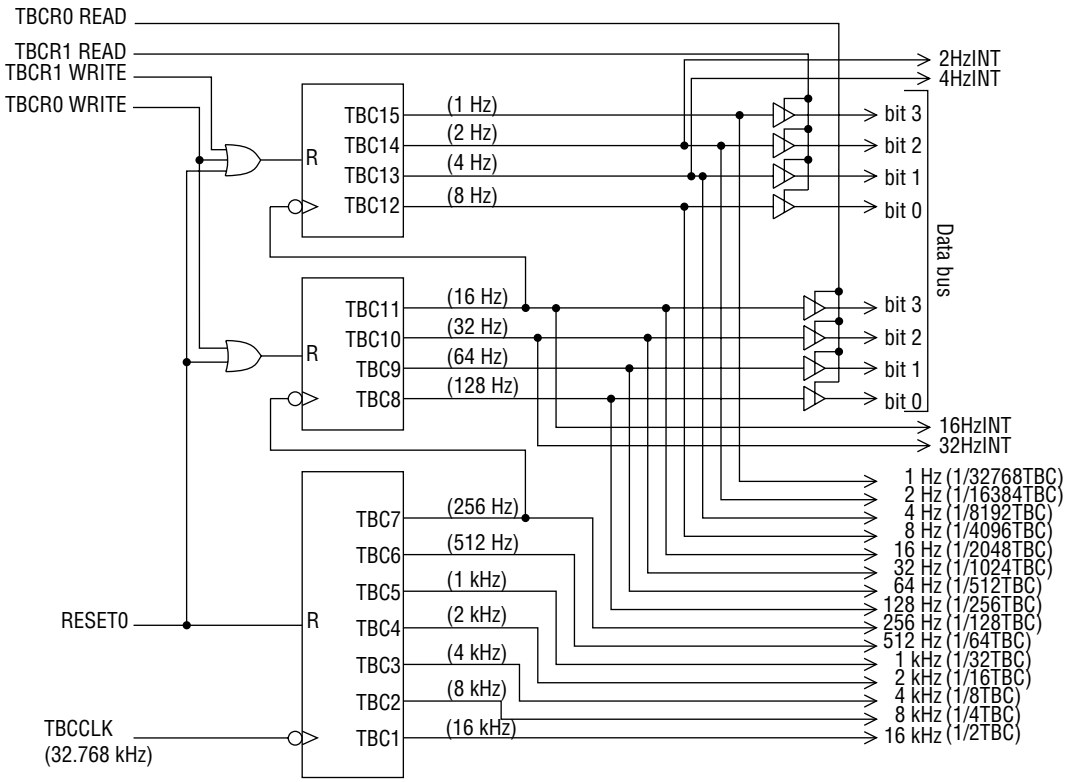


Figure 8-1 Time Base Counter (TBC) Configuration

(when a 32.768 kHz crystal is used for low-speed clock oscillation)

8.3 Time Base Counter Registers

Time base counter register 0 (TBCR0), time base counter register 1 (TBCR1)

These 4-bit special function registers (SFRs) are used to read the 1 to 8 Hz and 16 to 128 Hz outputs of the time base counter.

A write operation to TBCR0 sets both the 1 to 8 Hz and 16 to 128 Hz outputs to "0", and a write operation to TBCR1 sets the 1 to 8 Hz output to "0".

	bit 3	bit 2	bit 1	bit 0
TBCR0 (060H) (R/W)	16 Hz	32 Hz	64 Hz	128 Hz
TBCR1 (061H) (R/W)	1 Hz	2 Hz	4 Hz	8 Hz

8.4 Time Base Counter Operation

After system reset the time base counter (TBC) begins to count up from 0000H. The count is incremented at the falling edge of the TBCCLK.

TBC 32 Hz/16 Hz/4 Hz/2 Hz outputs are used as time base interrupts. At each output falling edge, four bits of interrupt request register 4 (IRQ4) are set to "1", namely bit 3 (Q32Hz), bit 2 (Q16Hz), bit 1 (Q4Hz) and bit 0 (Q2Hz), requesting an interrupt to the CPU. TBC outputs are also used as clocks for various circuits.

TBC 1 to 8 Hz output and 16 to 128 Hz output can be read through the time base counter register 0/1 (TBCR0/TBCR1).

A write operation to TBCR1 sets the 1 to 8 Hz output counter to "0", and a write operation to TBCR0 sets both the 1 to 8 Hz and 16 to 128 Hz output counters to "0". The write data in these write operations has no significance. For example, the "MOV TBCR0, A" instruction can be used to write, but is not dependent on accumulator content in any way. When write is executed to TBCR0 and TBCR1 and the 1 to 8 Hz and 16 to 128 Hz counters reset, interrupt requests are generated if 32 Hz/16 Hz/4 Hz/2 Hz outputs have been set to "1". To disable these interrupts, first set the master interrupt enable flag (MIE) or interrupt enable register 4 (IE4) to "0", execute the write operation to TBCR 0/1, and set the interrupt request flag 4 (IRQ4) to "0".

Figure 8-2 shows interrupt generation timing and time base counter output reset timing by writing "1" to TBCR0 and TBCR1.

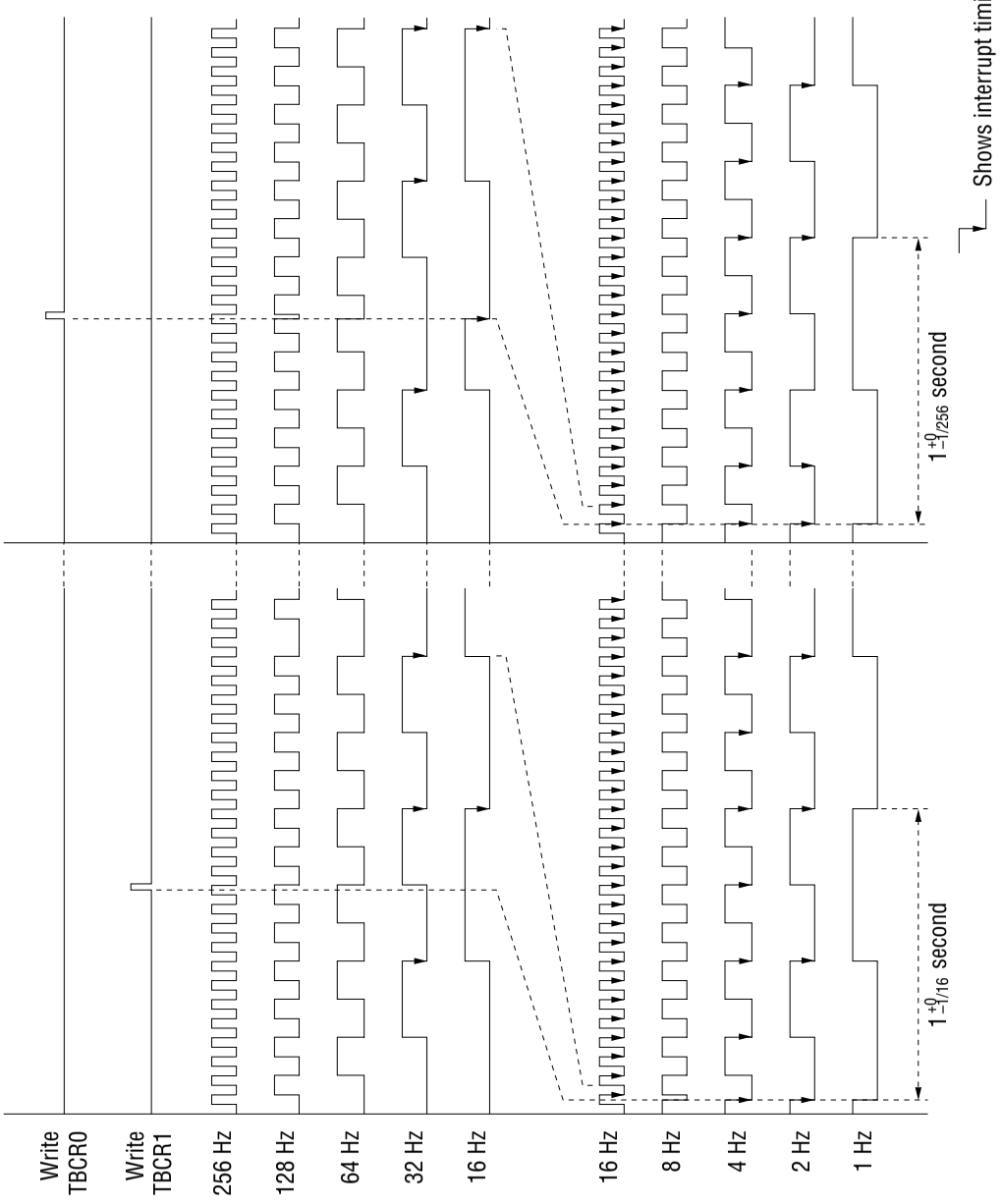


Figure 8-2 Interrupt Timing and Reset Timing by Writing "1" to TBCR0, TBCR1

Chapter 9

Timers (TIMER)

Chapter 9 Timers (TIMER)

9.1 Overview

The ML63187, ML63189B, and ML63193 have four internal 8-bit timers (0 to 3). Timers 0 and 1, or timers 2 and 3, can be used in tandem as a 16-bit timer.

Timers 0 and 1 have three operation modes: auto-reload mode, capture mode and frequency measurement mode. Timers 2 and 3 have two modes: auto-reload and frequency measurement. Timer clock may be set to the time base clock (TBCCLK: 32.768 kHz), the high-speed clock (HSCLK), or an external clock. When using the timers as a 16-bit timer, the overflow signals of timers 0 and 2 are used as the clocks for timers 1 and 3, respectively.

Timers can be used not only for pulse generation and time measurement, but as baud rate generators for serial communication in the ML63193.

	Timer 0	Timer 1	Timer 2	Timer 3
8-bit timer	●	●	●	●
16-bit timer	● (Timer 0 overflow signal is used as clock for timer 1)		● (Timer 2 overflow signal is used as clock for timer 3)	
Clock	TBCCLK / HSCLK / External clock (T02CK, T13CK)			
Auto-reload mode	●	●	●	●
Capture mode	●	●	—	—
Frequency measurement mode	●	●	●	●

9.2 Timer Configuration

Figures 9-1 through 9-4 show the configuration of timers 0 to 3.

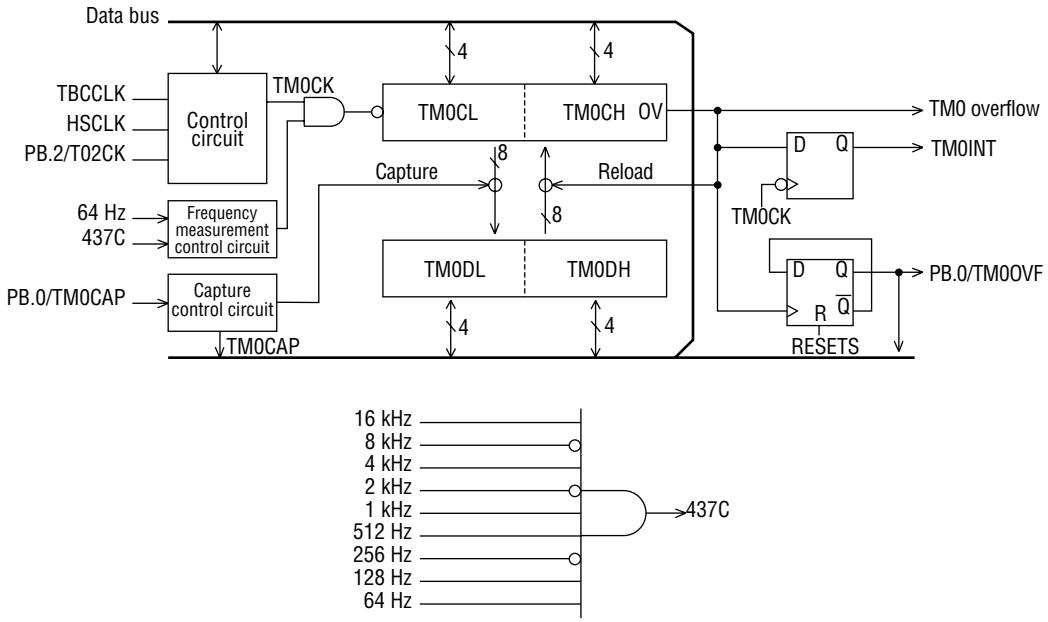


Figure 9-1 Timer 0 Configuration

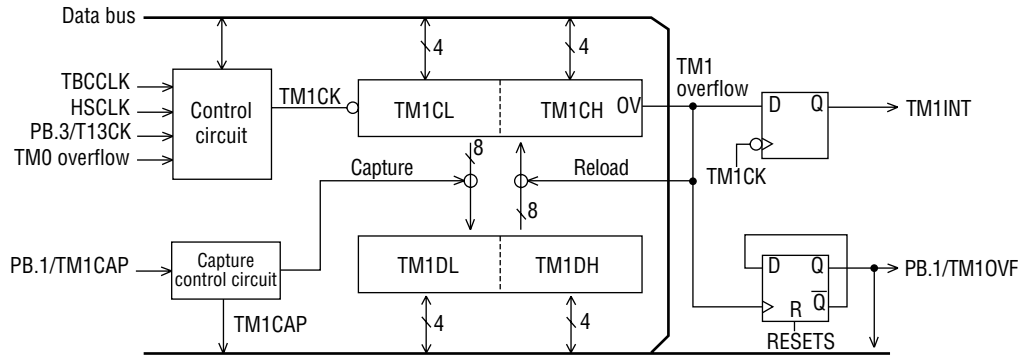


Figure 9-2 Timer 1 Configuration

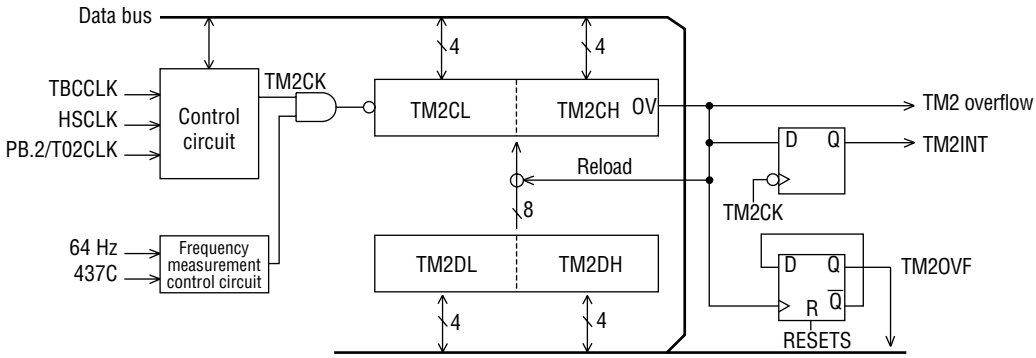


Figure 9-3 Timer 2 Configuration

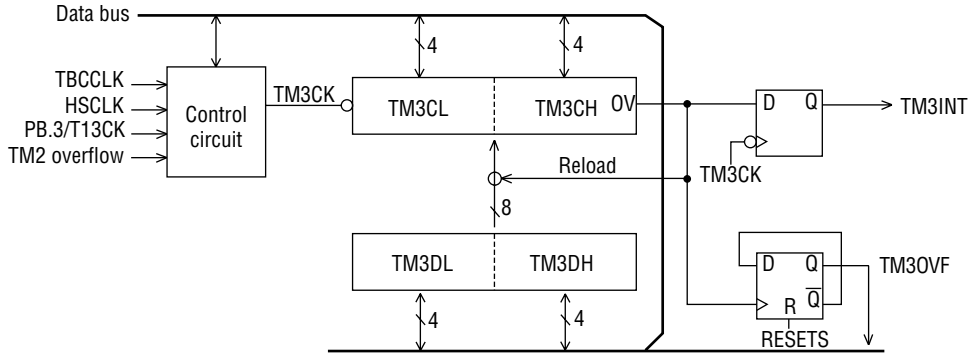


Figure 9-4 Timer 3 Configuration

9.3 Timer Registers

The following four registers are used for timer control.

(1) Timer data registers
(TM0DL, TM0DH, TM1DL, TM1DH, TM2DL, TM2DH, TM3DL, TM3DH)
(2) Timer counter registers
(TM0CL, TM0CH, TM1CL, TM1CH, TM2CL, TM2CH, TM3CL, TM3CH)
(3) Timer control registers
(TM0CON0, TM0CON1, TM1CON0, TM1CON1, TM2CON0, TM2CON1, TM3CON0, TM3CON1)
(4) Timer status registers
(TM0STAT, TM1STAT, TM2STAT, TM3STAT)

Each register is described below.

(1) Timer data registers

(TM0DL, TM0DH, TM1DL, TM1DH, TM2DL, TM2DH, TM3DL, TM3DH)

- During the auto-reload mode, timer data registers store the reload values.
- During the capture mode, timer data registers store the capture data.
  Writing to a timer data register causes the contents of the timer counter register to be transferred to the timer data register.
- At system reset, all valid bits are cleared to "0".
- Note regarding register values:
  Writing to the timer counter register causes the same value to also be written to the timer data register. However, when writing to the timer data register, the same value is not written to the timer counter register.

Timer 0 Registers

		bit 3	bit 2	bit 1	bit 0
TM0DL (Timer 0 lower)	(068H) (R/W)	T0D3	T0D2	T0D1	T0D0

		bit 3	bit 2	bit 1	bit 0
TM0DH (Timer 0 upper)	(069H) (R/W)	T0D7	T0D6	T0D5	T0D4

Timer 1 Registers

		bit 3	bit 2	bit 1	bit 0
TM1DL (Timer 1 lower)	(06AH) (R/W)	T1D3	T1D2	T1D1	T1D0

		bit 3	bit 2	bit 1	bit 0
TM1DH (Timer 1 upper)	(06BH) (R/W)	T1D7	T1D6	T1D5	T1D4

Timer 2 Registers

		bit 3	bit 2	bit 1	bit 0
TM2DL (Timer 2 lower)	(076H) (R/W)	T2D3	T2D2	T2D1	T2D0

		bit 3	bit 2	bit 1	bit 0
TM2DH (Timer 2 upper)	(077H) (R/W)	T2D7	T2D6	T2D5	T2D4

Timer 3 Registers

		bit 3	bit 2	bit 1	bit 0
TM3DL (Timer 3 lower)	(078H) (R/W)	T3D3	T3D2	T3D1	T3D0

		bit 3	bit 2	bit 1	bit 0
TM3DH (Timer 3 upper)	(079H) (R/W)	T3D7	T3D6	T3D5	T3D4

(2) Timer counter registers

(TM0CL, TM0CH, TM1CL, TM1CH, TM2CL, TM2CH, TM3CL, TM3CH)

- 8-bit binary counter operation
- At system reset, all valid bits are cleared to "0".
- Note regarding register values:

  Writing to the timer counter register causes the same value to also be written to the timer data register. However, when writing to the timer data register, the same value is not written to the timer counter register.

Timer 0 Registers

		bit 3	bit 2	bit 1	bit 0
TM0CL (Timer 0 lower)	(06CH) (R/W)	T0C3	T0C2	T0C1	T0C0

		bit 3	bit 2	bit 1	bit 0
TM0CH (Timer 0 upper)	(06DH) (R/W)	T0C7	T0C6	T0C5	T0C4

Timer 1 Registers

		bit 3	bit 2	bit 1	bit 0
TM1CL (Timer 1 lower)	(06EH) (R/W)	T1C3	T1C2	T1C1	T1C0

		bit 3	bit 2	bit 1	bit 0
TM1CH (Timer 1 upper)	(06FH) (R/W)	T1C7	T1C6	T1C5	T1C4

Timer 2 Registers

		bit 3	bit 2	bit 1	bit 0
TM2CL (Timer 2 lower)	(07AH) (R/W)	T2C3	T2C2	T2C1	T2C0

		bit 3	bit 2	bit 1	bit 0
TM2CH (Timer 2 upper)	(07BH) (R/W)	T2C7	T2C6	T2C5	T2C4

Timer 3 Registers

		bit 3	bit 2	bit 1	bit 0
TM3CL (Timer 3 lower)	(07CH) (R/W)	T3C3	T3C2	T3C1	T3C0

		bit 3	bit 2	bit 1	bit 0
TM3CH (Timer 3 upper)	(07DH) (R/W)	T3C7	T3C6	T3C5	T3C4

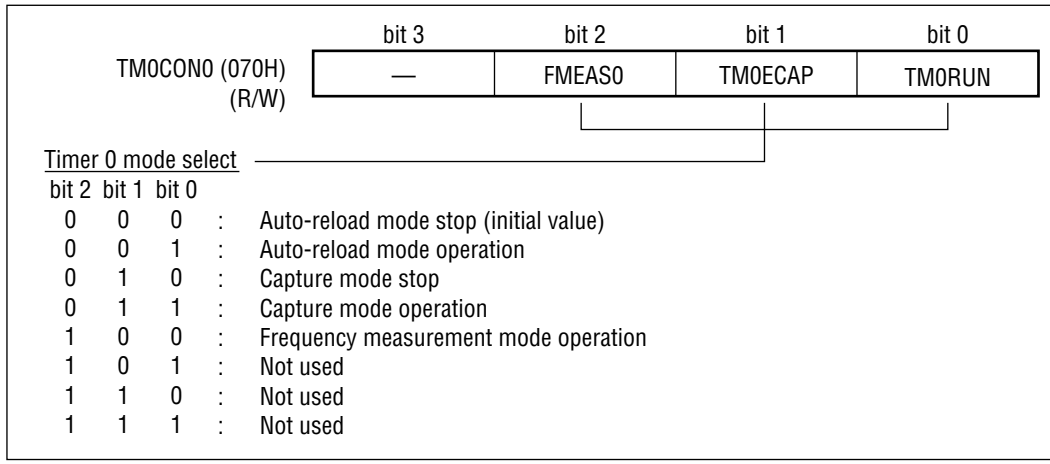
(3) Timer control registers

(TM0CON0, TM0CON1, TM1CON0, TM1CON1, TM2CON0, TM2CON1, TM3CON0, TM3CON1)

- Timer control registers select the operation mode and clock for each timer.
- At system reset, all valid bits are cleared to "0".
- Note regarding register values:
  Writing to the timer counter register causes the same value to also be written to the timer data register. However, when writing to the timer data register, the same value is not written to the timer counter register.

Timer 0 Registers

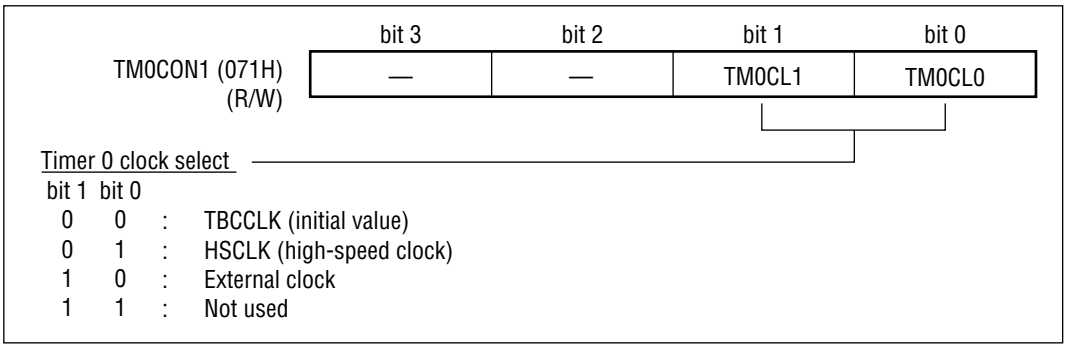
To use timer 1 in combination as a 16-bit timer, set timer 1 control registers TM1CON0 and TM1CON1.



bit 2, 1, 0: FMEAS0, TM0ECAP, TM0RUN

These bits select the timer 0 operation mode.

The timer 0 operation mode can be selected as auto-reload mode, capture mode, or frequency measurement mode.



bit 1, 0: TM0CL1, TM0CL0

These bits select the timer 0 clock.

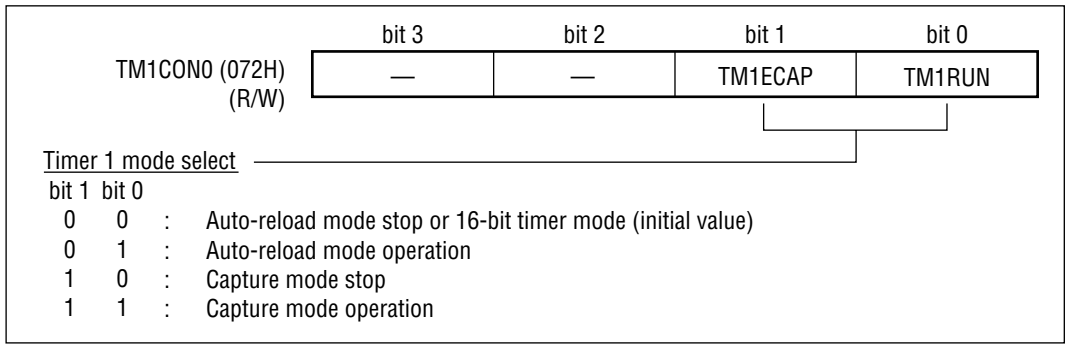
The timer 0 clock can be selected as TBCCLK (low-speed clock), HSCLK (high-speed clock), or external clock (T02CK: secondary function of PB.2).

Note:

If HSCLK is used as the clock, after ENOSC (bit 1 of FCON) is set to "1", wait for the following time interval before starting timer operation.

- Wait at least 10 ms when using ceramic oscillation.
- Wait at least 300 μs when using RC oscillation.

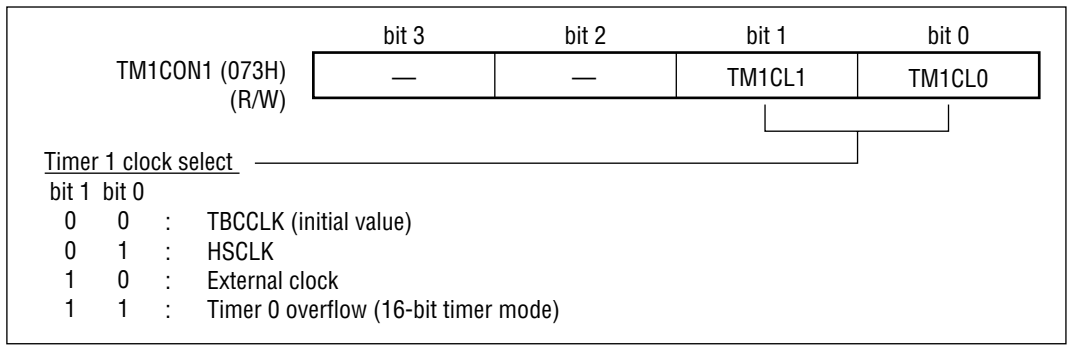
Timer 1 Registers



bit 1, 0: TM1ECAP, TM1RUN

These bits select the timer 1 operation mode.

The timer 1 operation mode can be selected as auto-reload mode, capture mode, or 16-bit timer mode.



bit 1, 0: TM1CL1, TM1CL0

These bits select the timer 1 clock.

The timer 1 clock can be selected as TBCCLK (low-speed clock), HSCLK (high-speed clock), external clock (T13CK: secondary function of PB.2), or the timer 0 overflow flag.

When using as a 16-bit timer, select timer 0 overflow for the clock.

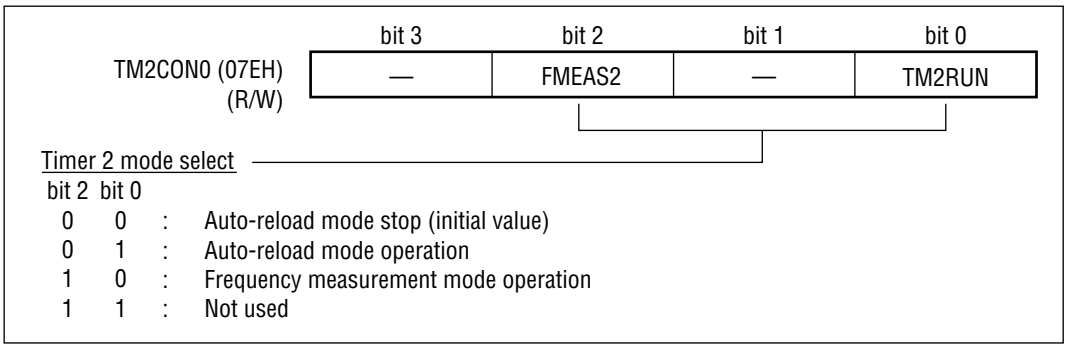
Note:

If HSCLK is used as the clock, after ENOSC (bit 1 of FCON) is set to "1", wait for the following time interval before starting timer operation.

- Wait at least 10 ms when using ceramic oscillation.
- Wait at least 300 μs when using RC oscillation.

Timer 2 Registers

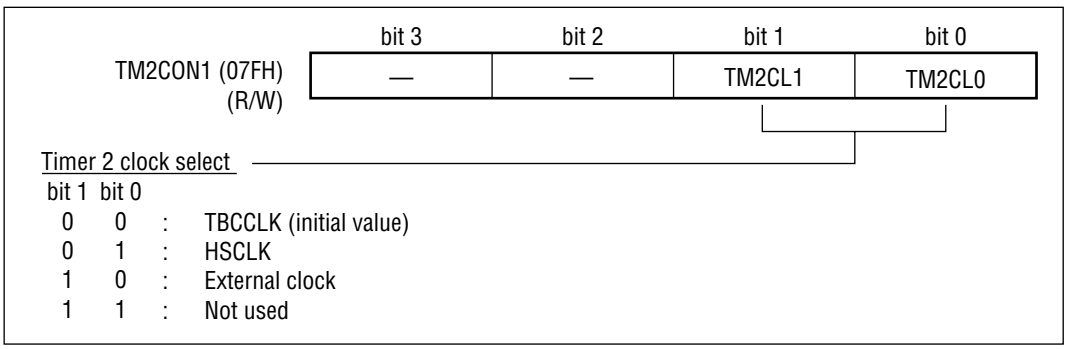
To use timer 3 in combination as a 16-bit timer, set timer 3 control registers TM3CON0 and TM3CON1.



bit 2, 0: FMEAS2, TM2RUN

These bits select the timer 2 operation mode.

The timer 2 operation mode can be selected as auto-reload mode or frequency measurement mode.



bit 1, 0: TM2CL1, TM2CL0

These bits select the timer 2 clock.

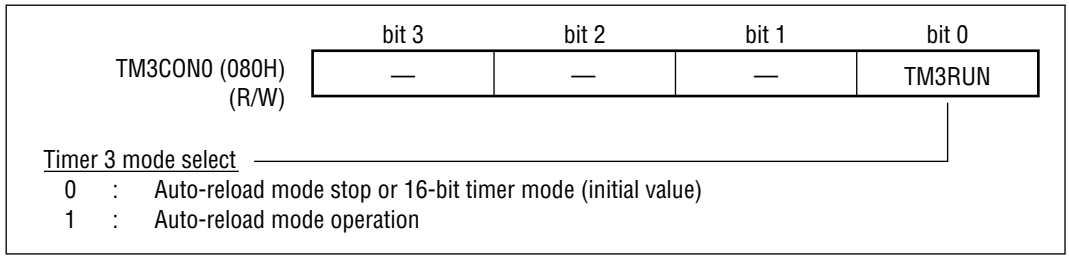
The timer 2 clock can be selected as TBCCLK (low-speed clock), HSCLK (high-speed clock), or external clock (T02CK: secondary function of PB.2).

Note:

If HSCLK is used as the clock, after ENOSC (bit 1 of FCON) is set to "1", wait for the following time interval before starting timer operation.

- Wait at least 10 ms when using ceramic oscillation.
- Wait at least 300 μs when using RC oscillation.

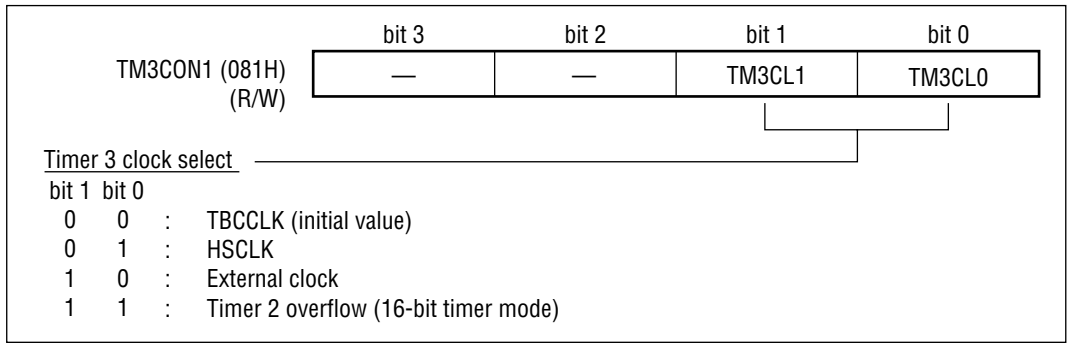
Timer 3 Registers



bit 0: TM3RUN

This bit selects the timer 3 operation mode.

The timer 3 operation mode can be selected as auto-reload mode or 16-bit timer mode.



bit 1, 0: TM3CL1, TM3CL0

These bits select the timer 3 clock.

The timer 3 clock can be selected as TBCCLK (low-speed clock), HSCLK (high-speed clock), external clock (T13CK: secondary function of PB.3), or the timer 2 overflow flag.

When using as a 16-bit timer, select timer 2 overflow for the clock.

Note:

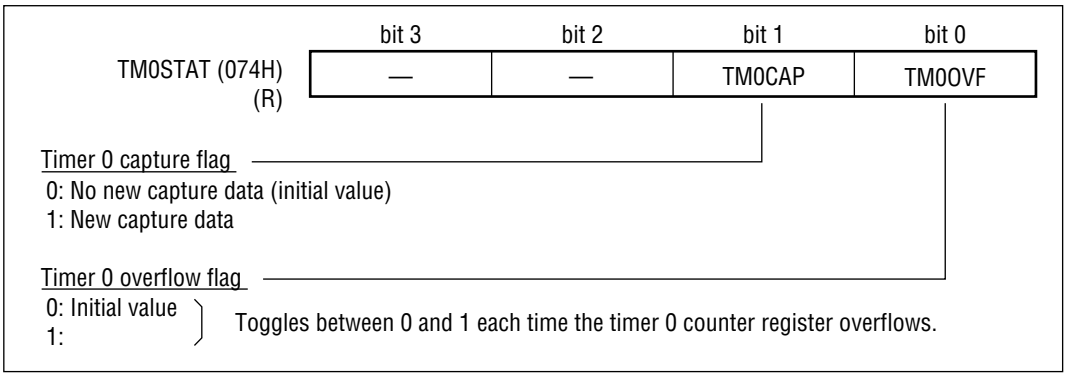
If HSCLK is used as the clock, after ENOSC (bit 1 of FCON) is set to "1", wait for the following time interval before starting timer operation.

- Wait at least 10 ms when using ceramic oscillation.
- Wait at least 300 µs when using RC oscillation.

(4) Timer status registers (TM0STAT, TM1STAT, TM2STAT, TM3STAT)

- Timer status registers read the status of each timer.
- At system reset, all valid bits are cleared to "0".

Timer 0 Registers



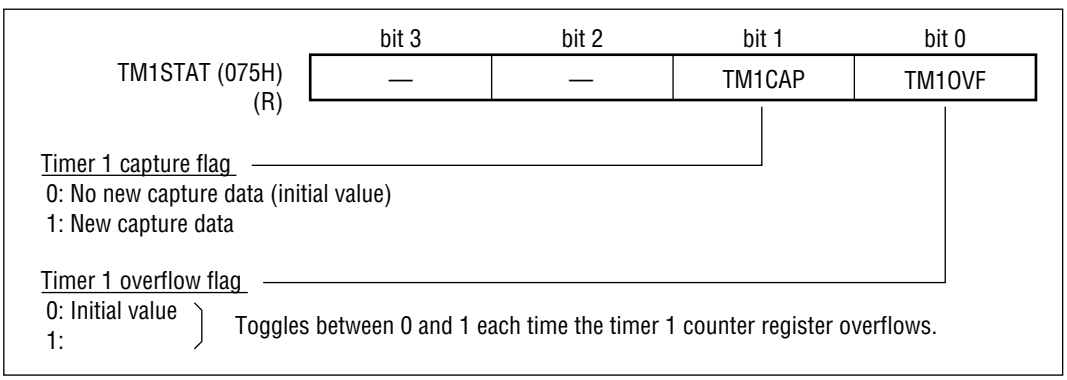
bit 1: TM0CAP (TiMer0 CAPture)

This bit indicates whether or not new capture data is present.
When TM0CAP = "0":
A value of "0" indicates that there has been no new capture data since system reset or since the last time TM0CAP was read.
When TM0CAP = "1":
A value of "1" indicates that there is new capture data since system reset or since the last time TM0CAP was read. Additional captures are disabled.
At system reset, TM0CAP is cleared to "0".
In the capture mode, if the level of the capture input pin (PB.0/TM0CAP) changes and a capture is generated, TM0CAP is automatically set to "1".
If TM0STAT is read, TM0CAP is automatically cleared to "0".

bit 0: TM0OVF (TiMer0 OVerFlow)

This bit indicates that the timer counter register has overflowed.
This bit toggles between "0" and "1" whenever overflow occurs.
At system reset, TM0OVF is cleared to "0".

Timer 1 Registers



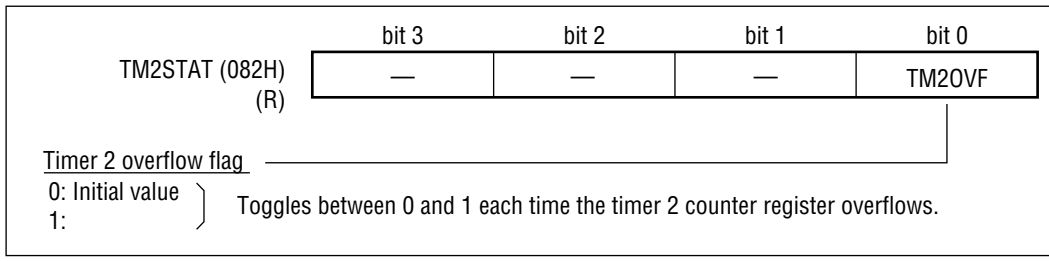
bit 1: TM1CAP (TiMer1 CAPture)

This bit indicates whether or not new capture data is present.
When TM1CAP = "0":
A value of "0" indicates that there has been no new capture data since system reset or since the last time TM1CAP was read.
When TM1CAP = "1":
A value of "1" indicates that there is new capture data since system reset or since the last time TM0CAP was read. Additional captures are disabled.
At system reset, TM1CAP is cleared to "0".
In the capture mode, if the level of the capture input pin (PB.1/TM1CAP) changes and a capture is generated, TM1CAP is automatically set to "1".
If TM1STAT is read, TM1CAP is automatically cleared to "0".

bit 0: TM1OVF (TiMer1 OVerFlow)

This bit indicates that the timer counter register has overflowed.
This bit toggles between "0" and "1" whenever overflow occurs.
At system reset, TM1OVF is cleared to "0".

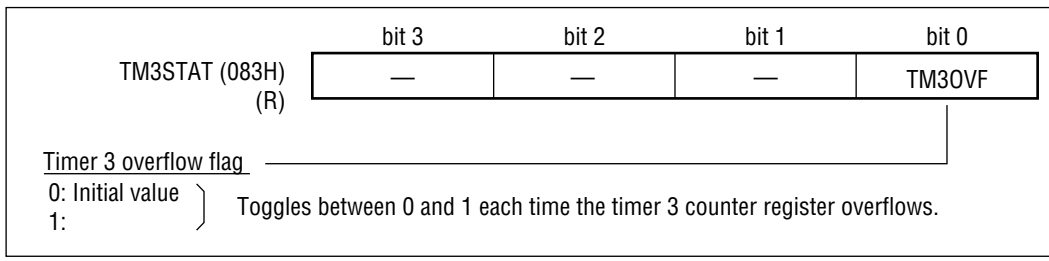
Timer 2 Register



bit 0: TM2OVF (TiMer2 OVerFlow)

This bit indicates that the timer counter register has overflowed.
This bit toggles between "0" and "1" whenever overflow occurs.
At system reset, TM2OVF is cleared to "0".

Timer 3 Register



bit 0: TM3OVF (TiMer3 OVerFlow)

This bit indicates that the timer counter register has overflowed.
This bit toggles between "0" and "1" whenever overflow occurs.
At system reset, TM3OVF is cleared to "0".

[Supplement] List of Timer Registers

Timer 0 Registers

Name	Symbol	Address	R/W	Initial value
Timer 0 data register L	TM0DL	068H	R/W	0H
Timer 0 data register H	TM0DH	069H		0H
Timer 0 counter register L	TM0CL	06CH	R/W	0H
Timer 0 counter register H	TM0CH	06DH		0H
Timer 0 control register 0	TM0CON0	070H	R/W	8H
Timer 0 control register 1	TM0CON1	071H		0CH
Timer 0 status register	TM0STAT	074H	R	0CH

Timer 1 Registers

Name	Symbol	Address	R/W	Initial value
Timer 1 data register L	TM1DL	06AH	R/W	0H
Timer 1 data register H	TM1DH	06BH		0H
Timer 1 counter register L	TM1CL	06EH	R/W	0H
Timer 1 counter register H	TM1CH	06FH		0H
Timer 1 control register 0	TM1CON0	072H	R/W	0CH
Timer 1 control register 1	TM1CON1	073H		0CH
Timer 1 status register	TM1STAT	075H	R	0CH

Timer 2 Registers

Name	Symbol	Address	R/W	Initial value
Timer 2 data register L	TM2DL	076H	R/W	0H
Timer 2 data register H	TM2DH	077H		0H
Timer 2 counter register L	TM2CL	07AH	R/W	0H
Timer 2 counter register H	TM2CH	07BH		0H
Timer 2 control register 0	TM2CON0	07EH	R/W	0AH
Timer 2 control register 1	TM2CON1	07FH		0CH
Timer 2 status register	TM2STAT	082H	R	0EH

Timer 3 Registers

Name	Symbol	Address	R/W	Initial value
Timer 3 data register L	TM3DL	078H	R/W	0H
Timer 3 data register H	TM3DH	079H		0H
Timer 3 counter register L	TM3CL	07CH	R/W	0H
Timer 3 counter register H	TM3CH	07DH		0H
Timer 3 control register 0	TM3CON0	080H	R/W	0EH
Timer 3 control register 1	TM3CON1	081H		0CH
Timer 3 status register	TM3STAT	083H	R	0EH

9.4 Timer Operation

9.4.1 Timer Clock

The timer clock can be selected as TBCCLK (low-speed clock: 32.768 kHz), HSCLK (high-speed clock), or an external clock. By using timer 0 and timer 2 overflow signals as clocks for timer 1 and timer 3, respectively, the timers can be used in pairs as 16-bit timers.

If the high-speed clock (HSCLK) is to be used, after setting ENOSC (bit 1 of FCON), wait at least 10 ms in the ceramic oscillation mode or 300 μs in the RC oscillation mode before operating the timer.

The external clock is input to a port assigned as a secondary function port. In the case of timers 0 and 2, PB.2/T02CK is used as the input pin for the external clock. In the case of timers 1 and 3, PB.3/T13CK is used as the input pin for the external clock. Since the external clock is sampled by the system clock (CLK), the high- and low-levels of the external clock should be longer than 1 cycle of the system clock (CLK).

9.4.2 Timer Data Registers

TM0DL, TM0DH, TM1DL, TM1DH, TM2DL, TM2DH, TM3DL and TM3DH are 4-bit registers.

In the auto-reload mode, the timer data registers save values that are reloaded into the timer counter registers when the timer counter registers overflow.

In the capture mode, the timer data registers save the value of the timer counter registers when a capture signal is input. Each timer data register can be read/written by software. Writing to timer data registers does not change the contents of the timer counter registers.

9.4.3 Timer Counter Registers

TM0CL and TM0CH, TM1CL and TM1CH, TM2CL and TM2CH, and TM3CL and TM3CH are 8-bit binary counters that are incremented at the falling edge of the timer clock.

Each timer counter register can be read/written by software. However, if the CPU clock and timer clock are different, values that are read or written during the count operation cannot be guaranteed. If an external clock is used as the timer clock, reading/writing is always possible.

When a value is written to any timer counter register, the same value is also written to the corresponding timer data register.

9.4.4 Timer Interrupt Requests and Overflow Flags

Timers generate timer interrupt requests when the timer counter register overflows. The overflow flag toggles between "1" and "0" at each overflow. The output of the overflow flag of timers 0 and 1 can be output to secondary port functions PB.0/TM0OVF and PB.1/TM1OVF pins.

Figure 9-5 indicates the operation timing for timer counter register overflow. Table 9-1 lists timer interrupts.

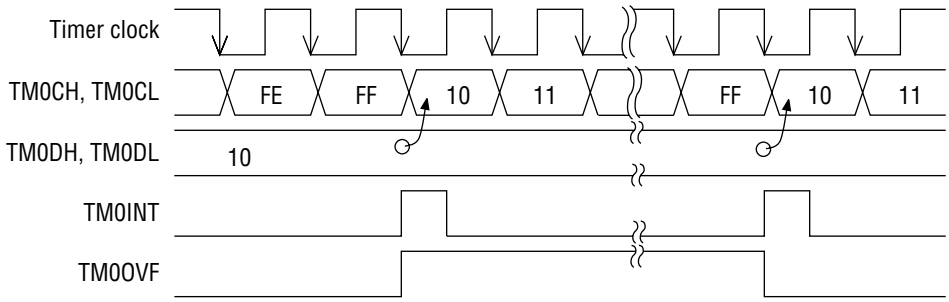


Figure 9-5 Timer Counter Register Overflow Timing (for Timer 0)

Table 9-1 List of Timer Interrupts

Interrupt factor	Symbol	IRQ flag (IRQ2)	IE flag (IE2)	Interrupt vector address
Timer 0 interrupt	TM0INT	QTM0	ETM0	0020H
Timer 1 interrupt	TM1INT	QTM1	ETM1	0022H
Timer 2 interrupt	TM2INT	QTM2	ETM2	0024H
Timer 3 interrupt	TM3INT	QTM3	ETM3	0026H

When the master interrupt enable flag (MIE) is set to "1" with the interrupt enable flags (ETM0–3) set to "1", and a timer overflow occurs, a CPU interrupt request is generated.

9.4.5 Auto-Reload Mode Operation

Timers 0 to 3 can be used as auto-reload mode timers. The setup method is as follows.

- Timer 0: Set FMEAS0 (bit 2 of TM0CON0) to "0", and set TM0ECAP (bit 1 of TM0CON0) to "0".
- Timer 1: Set TM1ECAP (bit 1 of TM1CON0) to "0".
- Timer 2: Set FMEAS2 (bit 2 of TM2CON0) to "0".
- Timer 3: No setup needed.

In the auto-reload mode, each time the timer counter register overflows, the timer data register value is reloaded into the timer counter register, and counting begins from the value. Setting the RUN bits (TM0RUN, TM1RUN, TM2RUN, TM3RUN) for each timer control register to "1" will restart the count, and resetting to "0" stops the count.

In the 16-bit timer mode for timers 0 and 1 the TM1RUN bit is disabled, and start/stop is controlled with the TM0RUN bit. In the 16-bit timer mode for timers 2 and 3 the TM3RUN bit is disabled, and start/stop is controlled with the TM2RUN bit.

Figure 9-6 shows auto-reload mode timing for pulse generation when timers 0 and 1 are used as a 16-bit timer.

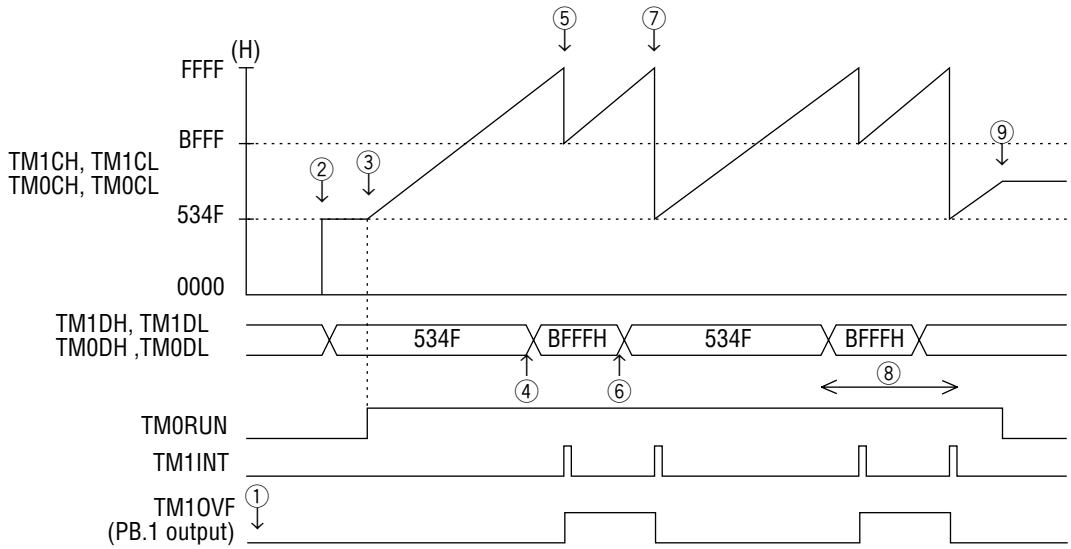


Figure 9-6 Auto-Reload Mode Timing

The operation procedures are as follows.

① Set PB.1 to the output mode (TM1OVF) secondary function.

② Write 534FH to the timer data and timer counter registers.
TM1DH = TM1CH = 5H (bits 15–12)
TM1DL = TM1CL = 3H (bits 11–8)
TM0DH = TM0CH = 4H (bits 7–4)
TM0DL = TM0CL = FH (bits 3–0)

③ If TM0CON and TM1CON are set to auto-reload mode and TM0RUN is set to "1", the timer counter register will start to count from 534FH.

④ Before the timer counter register overflows, write the next reload value BFFFH to the timer data register.

⑤ When the timer counter register overflows, BFFFH is set to the timer counter register, timer interrupt TM1INT is generated and timer 1 overflow flag TM1OVF toggles. The timer counter register continues to count up from BFFFH.

⑥ Before the timer counter register overflows, write the next reload value 534FH to the timer data register.

⑦ When the timer counter register overflows, 534FH is set to the timer counter register, timer interrupt TM1INT is generated and timer 1 overflow flag TM1OVF toggles. The timer counter register resumes counting from address 534FH.

⑧ Repeat steps 4 through 7. This allows a user-defined pulse to be output from PB.1/TM1OVF.

⑨ Halt the count by resetting TM0RUN to "0".

Figure 9-7 shows TM0RUN count start/halt timing.

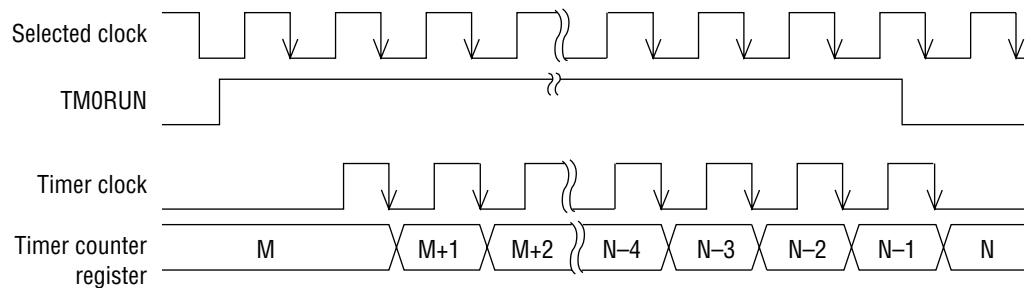


Figure 9-7 TM0RUN Count Start/Halt Timing

When TM0RUN is set to "1", the timer counter starts to count from the second falling edge of the selected clock. When TM0RUN is reset to "0", the counter stops counting at the falling edge of the selected clock which appears immediately after the TM0RUN falling edge.

9.4.6 Capture Mode Operation

Timer 0 and timer 1 can be used as capture mode timers.

In a capture mode, a change in the capture input (PB.0/TM0CAP, PB.1/TM1CAP) level during operation of the timer counter register triggers loading of the value of the timer counter register into the timer data register.

Methods to set the capture mode for each timer are listed below.

- Timer 0: Set TM0ECAP (bit 1 of TM0CON0) to "1", and set FMEAS0 (bit 2 of TM0CON0) to "0".
- Timer 1: Set TM1ECAP (bit 1 of TM1CON0) to "1".

In the capture mode, reloading the timer data register data into the timer counter register is inhibited, and when the timer counter register overflows, counting is restarted from 00H.

When a capture occurs, the capture flags (TM0CAP, TM1CAP) of the timer status registers (TM0STAT, TM1STAT) are set to "1". Additional captures are disabled while the capture flags are "1". The capture flags are assigned to bit 0 of the timer status registers, and are automatically cleared to "0" when the timer status registers are read.

If both the TM1CL1 and TM1CL0 bits of the timer 1 control register 1 (TM1CON1) are set to "1" and timer 0 overflow is selected as the clock, the 16-bit capture mode will be set. In this case, the PB.0/TM0CAP pin is the capture trigger input.

Figure 9-8 shows the timer 0 capture mode timing for pulse width measurement.

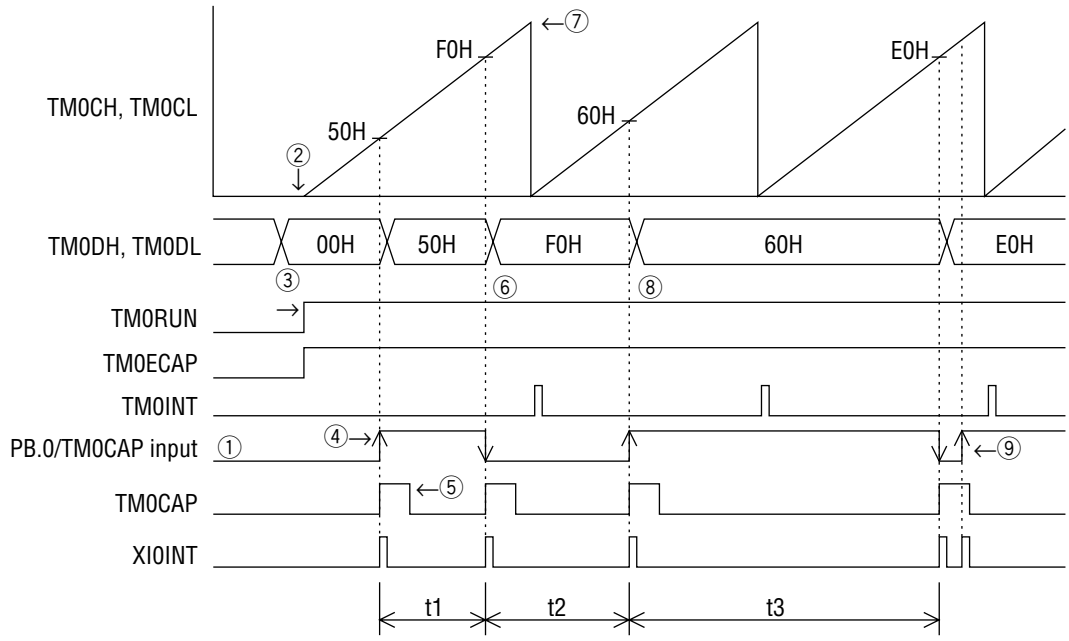


Figure 9-8 Capture Mode Timing

The operation procedure is listed below.

① Set PB.0/TM0CAP to input mode, and enable XI0INT and TM0INT.

② Clear all bits of the timer counter registers and timer data registers to zero.

③ Set TM0CON0 to the capture mode, and set TM0RUN to "1" to begin upward counting.

④ If the PB.0/TM0CAP input changes, the TM0CH/TM0CL value is captured by TM0DH/TM0DL and TM0CAP is set to "1" (first capture). The CPU detects this through XI0INT and reads the values of TM0DH/TM0DL.

⑤ After the TM0DH/TM0DL read is complete, TM0CAP is cleared to "0" to wait for the next capture.

⑥ If the PB.0/TM0CAP input changes, repeat operations ④ and ⑤ (second capture).

The high-level pulse width t1 of the PB.0 input can be determined as follows.

$$t1 = (F0H - 50H) \times t_{CLK} \qquad t_{CLK}: \text{TMCLK cycle}$$

⑦ TM0INT is generated when the timer counter register overflows. When overflow occurs, the timer counter register changes from FFH to 00H and continues upward counting.

⑧ If the PB.0/TM0CAP input changes, repeat operations ④ and ⑤ (third capture). Because the counter overflows once during the interval between the second capture and the third capture, the low-level pulse width t2 of the PB.0 input can be determined as follows.

$$t2 = (60H - F0H + 100H) \times t_{CLK}$$

⑨ While TM0CAP = "1", there is no capture even when PB.0/TM0CAP changes.

Figure 9-9 shows the capture timing and Figure 9-10 shows the capture signal (CAPT) generator circuit.

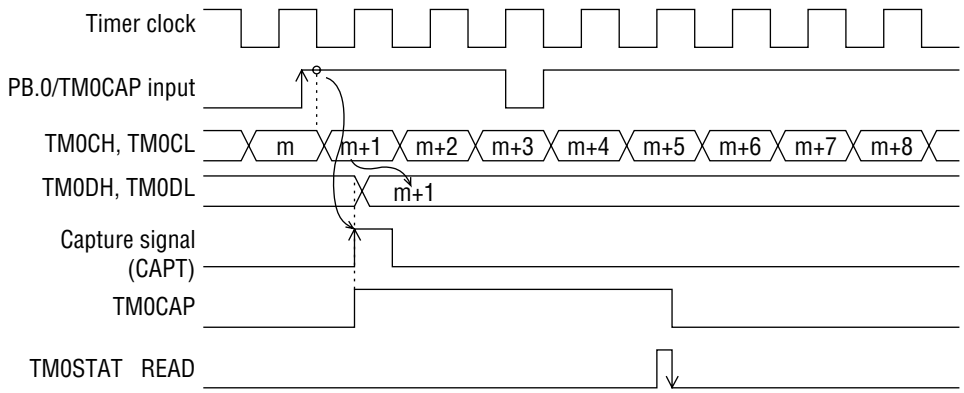


Figure 9-9 Capture Timing

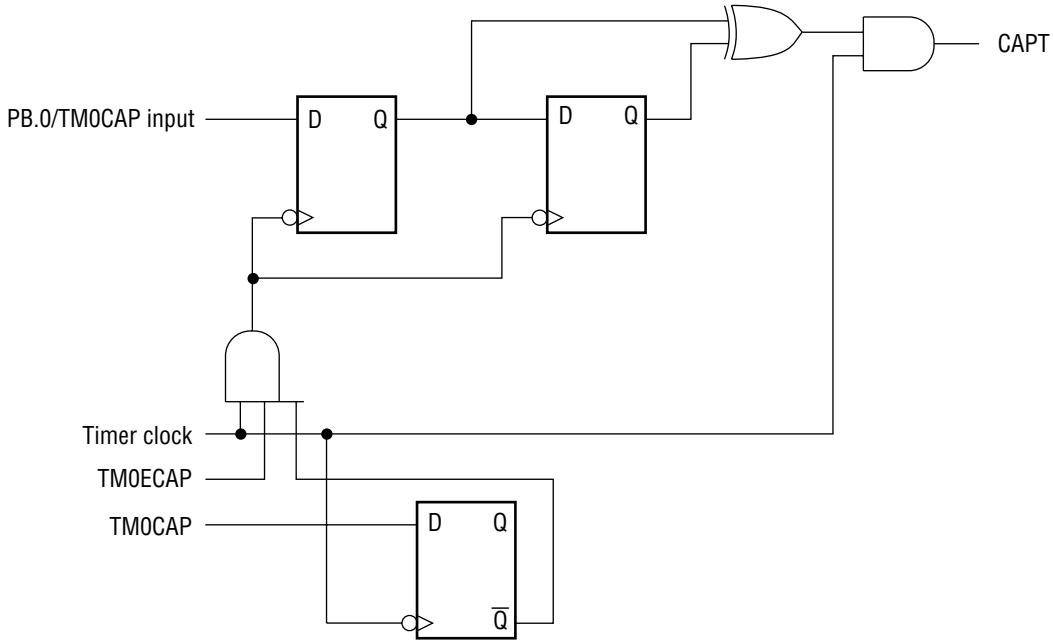


Figure 9-10 Capture Signal (CAPT) Generator Circuit

Note:

The maximum delay from a PB.0/TM0CAP input level change until capture is one cycle of the timer clock.

9.4.7 Frequency Measurement Mode Operation

The frequency measurement mode is used to measure the frequency of the RC oscillator clock, which has wide product variation.

Timers 0 and 1, and timers 2 and 3 can be used in the frequency measurement mode. These timers are set as follows for the frequency measurement mode:

- Timer 0: Set FMEAS0 (bit 2 of TM0CON0) to "1", and set TM0ECAP (bit 1 of TM0CON0) and TM0RUN (bit 0 of TM0CON0) to "0".
- Timer 1: Set TM1ECAP (bit 1 of TM1CON0) and TM1RUN (bit 0 of TM1CON0) to "0".
- Timer 2: Set FMEAS2 (bit 2 of TM2CON0) to "1", and set TM2RUN (bit 0 of TM2CON0) to "0".
- Timer 3: Set TM3RUN (bit 0 of TM3CON0) to "0".

The count obtained in the frequency measurement mode can be used to determine the auto-reload mode timer data register value, thereby making the timer overflow to generate various signals with required cycles. In the ML63193, the timer 3 interrupt signal (TM3INT) is used as the baud rate clock.

Figure 9-11 indicates frequency measurement mode timing when timers 2 and 3 are used as a 16-bit timer.

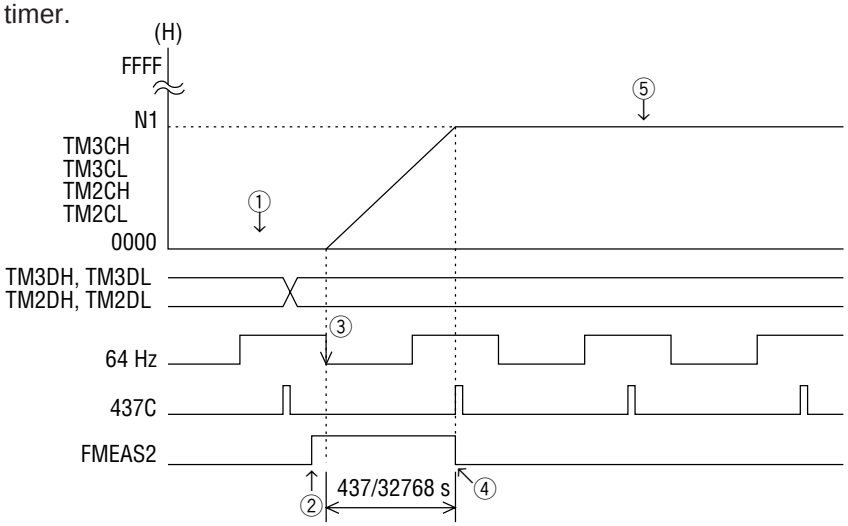


Figure 9-11 Frequency Measurement Mode Timing

The operation sequence for Figure 9-11 is as follows.

① Timer 3 control registers 0 and 1 (TM3CON0, TM3CON1) are set for 16-bit timer mode, and the timer counter and timer data register are cleared to "0". Enable the high-speed clock by the frequency control register (FCON) and the timer clock is set to HSCLK.

② Wait 10 ms or more in the ceramic oscillation mode or 300 μs or more in the RC oscillation mode after starting the high-speed clock and set FMEAS2 to "1" to enter the frequency measurement mode.

③ When FMEAS2 is "1", the counter starts at the 64 Hz falling edge.

④ When the 437C signal is "1", FMEAS2 is reset to "0", and the counter stops at the falling edge of the next clock. The 437C signal is a pulse signal which rises in 437/32768 seconds after the 64 Hz falling edge.

⑤ Timer counter register value N1 is read.

Assuming that the ceramic oscillation clock is exactly 2 MHz, value N1 read from the timer counter register is:

$$N1 = 2000000 \times 437/32768$$
$$= 26672 \text{ (decimal)}$$
$$= 6830 \text{ (hexadecimal)}$$
$$= 0110\ 1000\ 0011\ 0000 \text{ (binary)}$$
(truncated)

Because 437/32768 seconds are equivalent to 128 clocks at 9600 Hz (more precisely, 9598 Hz), a division of the count by 128 provides the frequency ratio (N2) between 2 MHz and 9600 Hz. Because $128 = 2^7$, that can be determined by merely truncating the righthand seven digits of N1 (binary), yielding.

$$N2 = 26672/128 = 011010000 \text{ (binary)}$$
$$= D0 \text{ (hexadecimal)}$$
$$= 208 \text{ (decimal)}$$

This indicates that 9600 Hz is about 208 times the cycle of 2 MHz, which means that the timer data register should be set to FF30H so that the counter overflows every 208 counts of the 2 MHz clock in auto-reload mode. As a result, overflow produces a TM3INT cycle t_{TM3INT} of

$$t_{TM3INT} = 1/2000000 \times 208 = 0.104 \text{ ms (9615 Hz)}$$

In the same way, assuming that RC oscillation clock is 600 kHz due to manufacturing variation, we get

$$N1 = 600000 \times 437/32768 = 8001 \text{ (decimal)}$$
$$= 1F41 \text{ (hexadecimal)}$$
$$= 0001\ 1111\ 0100\ 0001 \text{ (binary)}$$
(truncated)

Truncating the righthand seven digits of N1 (binary), we get

$$N2 = 8001/128 = 000111110 \text{ (binary)}$$
$$= 3E \text{ (hexadecimal)}$$
$$= 62 \text{ (decimal)}$$

Set the timer data register to FFC2H so that the counter overflows every 62 counts of the 600 kHz clock in auto-reload mode. As a result, overflow produces a TM3INT cycle t_{TM3INT} of

$$t_{TM3INT} = 1/600000 \times 62 = 0.10333 \text{ ms (9677 Hz)}$$

In this way the frequency measurement mode can be applied to generate TM3INT signals with precision cycles. These TM3INT signals can be supplied to the serial port as a baud rate clock.

Changing the value of N2 makes it possible to generate baud rates of 4800 Hz, 2400 Hz or user-defined rates. The precision of the generated baud rate clock is within ±2% for 9600 Hz, and within ±1% for 4800 Hz or lower.

Figure 9-12 illustrates the operation of timer 3 interrupt for an RC oscillator clock frequency of 600 kHz.

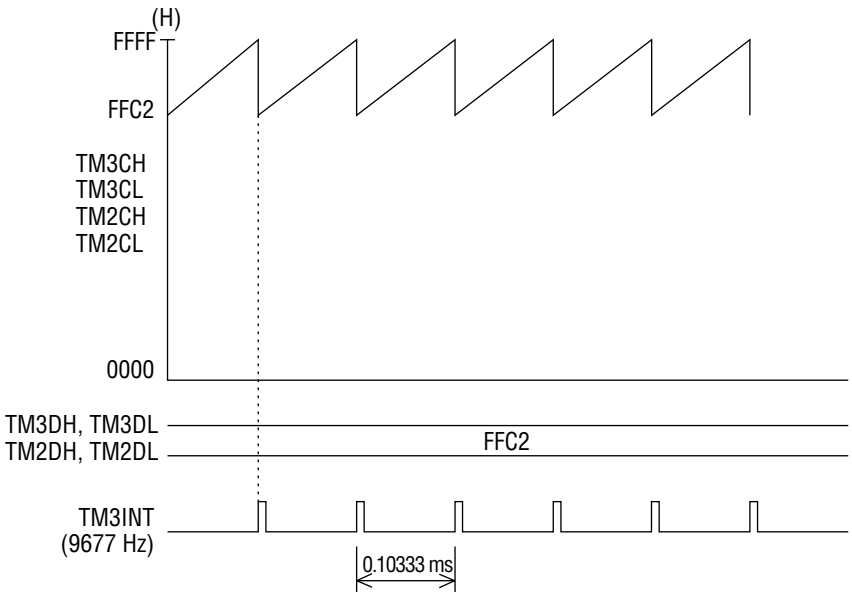


Figure 9-12 Timer 3 Interrupt (TM3INT) Generation

Chapter 10

100 Hz Timer Counter (100HzTC)

Chapter 10 100 Hz Timer Counter (100HzTC)

10.1 Overview

The 100 Hz timer counter has a circuit that divides the TBC6 output (512 Hz) of the time base counter to generate a 10 Hz interrupt. The 100 Hz timer consists of a 5/6-base counter and two decimal counters.

10.2 100 Hz Timer Counter Configuration

Figure 10-1 indicates the configuration of the 100 Hz timer counter.

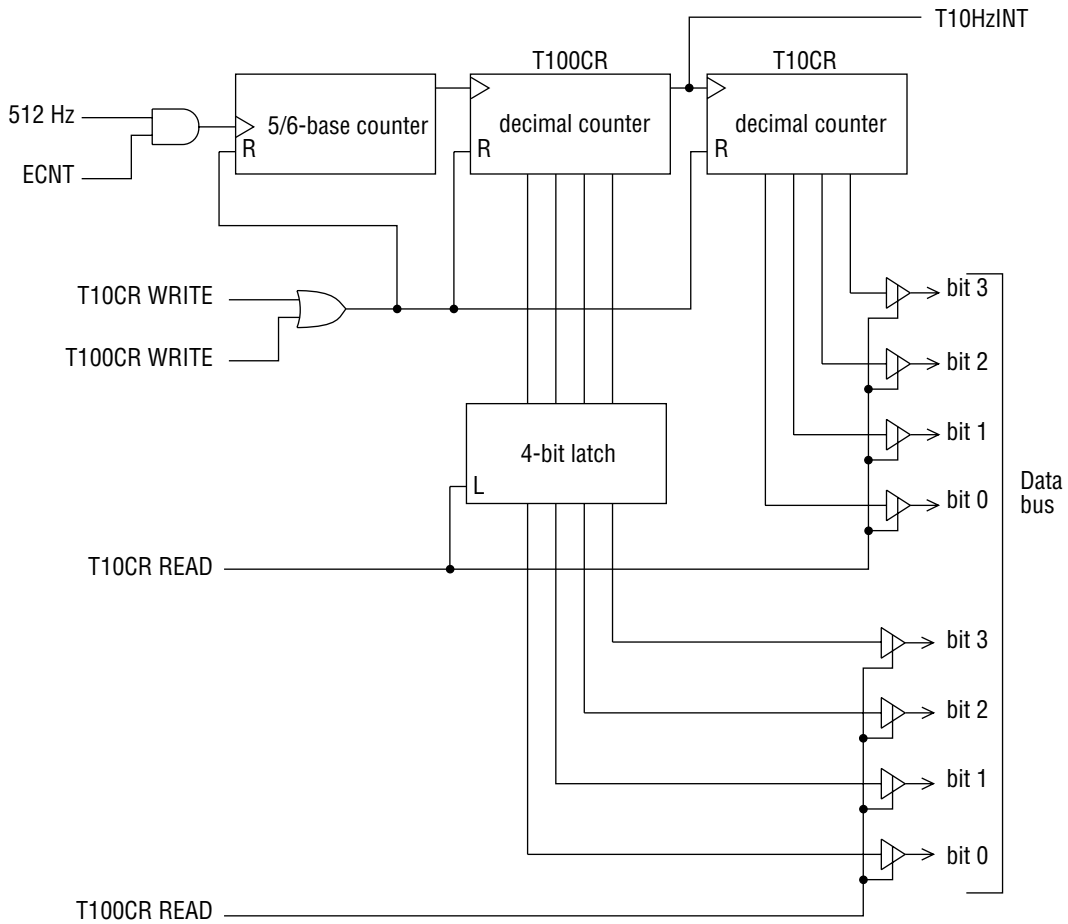
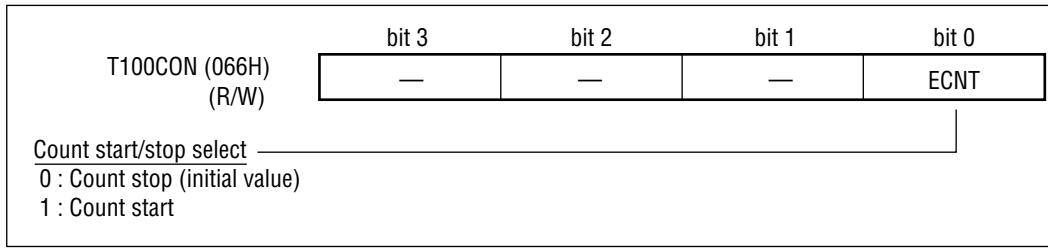


Figure 10-1 100 Hz Timer Counter Configuration

10.3 100 Hz Timer Counter Registers

(1) 100 Hz timer counter control register (T100CON)

This is a 4-bit special function register (SFR) controlling the 100 Hz timer counter.



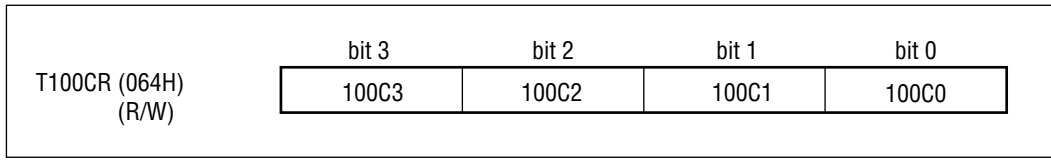
bit 0: ECNT

This bit controls count start/stop for the 100 Hz timer counter internal counter. Count starts when set to "1". At system reset the value is reset to "0" and counting is stopped.

(2) 100 Hz counter register (T100CR)

This is a 4-bit special function register (SFR) to read the 100 Hz counter of the 100 Hz timer counter. The content of the T100CR is latched by a 4-bit latch in T10CR read operation, so the value of the T100CR must always be read after reading T10CR.

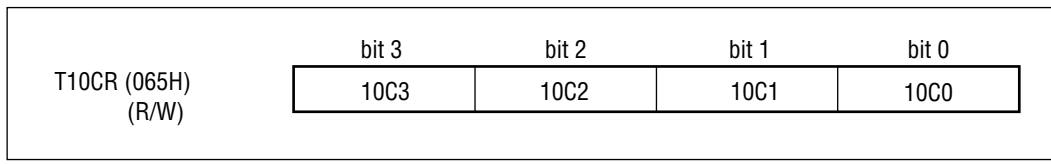
When data is written in T100CR, both T100CR and T10CR are reset to "0".



(3) 10 Hz counter register (T10CR)

A 4-bit special function register (SFR) to read the 10 Hz counter in the 100 Hz timer counter.

When data is written in T10CR, both T100CR and T10CR are reset to "0".



10.4 100 Hz Timer Counter Operation

The 100 Hz timer counter begins counting when bit 0 (ECNT) of the 100 Hz timer counter control register (T100CON) is set to "1". The 512 Hz output of the time base counter is divided into 100 Hz by the 5/6-base counter.

The 100 Hz signal is input to the 100 Hz counter (T100CR) and the carry output of that counter is input to the 10 Hz counter (T10CR). The 10HzINT signal, which is the carry output (10 Hz) of the T100CR 100 Hz counter also generates an interrupt request, setting bit 3 (Q10Hz) of interrupt request registers 3 (IRQ3) to "1".

If either T100CR or T10CR is written to, both are reset to "0". The write data used has no significance. For example, the "MOV T100CR, A" instruction is not dependent on the contents of the accumulator.

If T10CR is read, the contents of T100CR at that time are latched to the 4-bit latch. Therefore, the contents of T100CR at the time T10CR is read can be read correctly.

Chapter 11

Watchdog Timer (WDT)

Chapter 11 Watchdog Timer (WDT)

11.1 Overview

The watchdog timer is a circuit to detect CPU malfunction. The WDT consists of a 9-bit watchdog timer counter (WTDC) counting the 256 Hz output of the TBC7 of the time base counter (TBC), and a watchdog timer control register (WDTCON) to start and clear WDTC.

11.2 Watchdog Timer Configuration

Figure 11-1 shows the configuration of the watchdog timer.

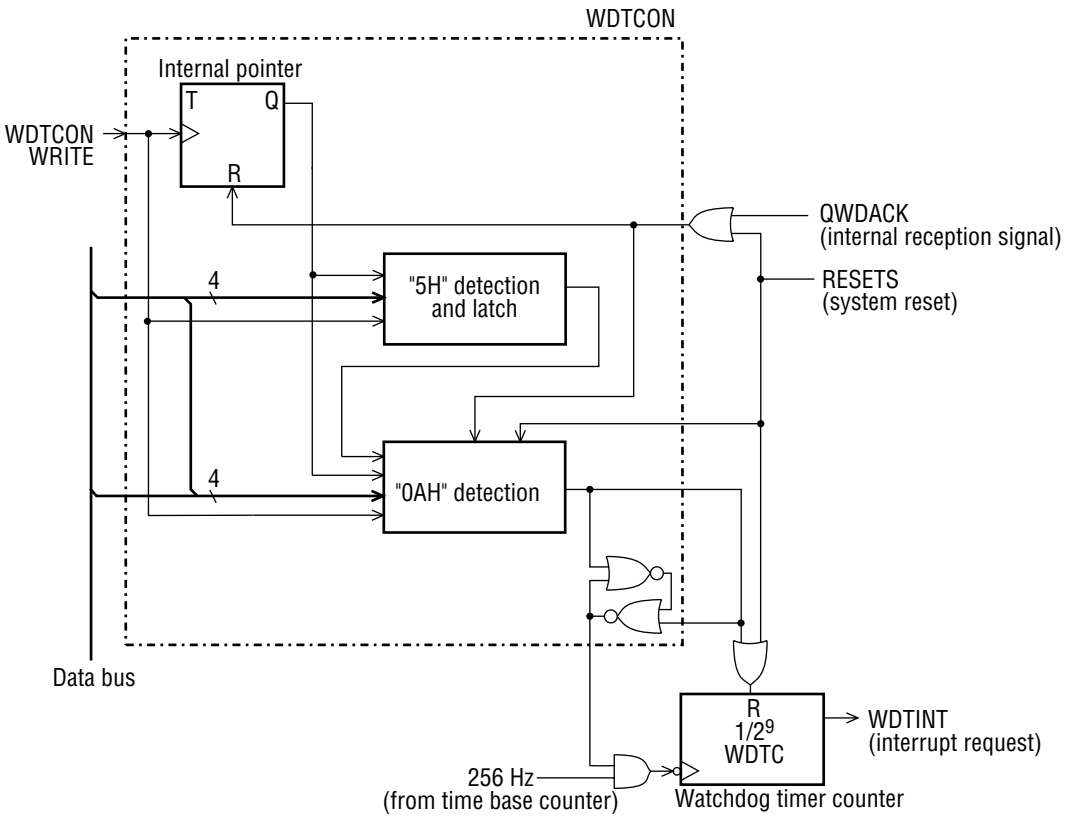


Figure 11-1 Watchdog Timer Configuration

11.3 Watchdog Timer Control Register (WDTCON)

The watchdog timer control register (WDTCON) is a 4-bit write only special function register (SFR) used to start/clear the watchdog timer counter (WDTC).

WDTCON (09FH) (W)

bit 3	bit 2	bit 1	bit 0
d3	d2	d1	d0

11.4 Watchdog Timer Operation

At system reset, WDTC (watchdog timer counter) stops counting.

WDTC begins counting by writing "5H" to WDTCON (watchdog timer control register) while the internal pointer is "0", and then writing "0AH" (while the internal pointer is "1").

The internal pointer is cleared to "0" at system reset or when WDTC overflows, and toggles every time a write operation to WDTCON is performed.

After WDTC is activated, WDTC is cleared by writing "5H" to WDTCON while the internal pointer is "0", and then writing "0AH" while the internal pointer is "1". When WDTC overflows (1FFH→000H), a watchdog timer interrupt request (WDTINT) is generated. WDTINT cannot be disabled by the software (non-maskable interrupt) and has the highest level of interrupt priority.

The WDTC overflow cycle (T) is given by:

$$T = \frac{128 \times 512}{32768\ (Hz)} = 2\ s$$

The minus deviation (t) of the WDTC overflow cycle is given by:

$$t = \frac{128}{32768\ (Hz)} = \text{approximately } 3.9\ ms$$

Therefore, the WDTC clear cycle (Ct) can be computed as follows.

$$Ct = T - t = 2\ s - 3.9\ ms = 1.9961\ s$$

If 32.768 kHz is to be used as the low-speed clock, the software must be programmed to clear WDTC within 1.9961 s.

If the CPU malfunctions due to a power failure or other factor and the WDTC cannot be cleared normally, WDTC will overflow and WDTINT will be generated. Program the watchdog timer interrupt routine to handle recovery operations by returning to the normal routine.

Note:

The watchdog timer cannot detect all operating faults. If the CPU malfunctions but WDTC can still be cleared, a fault will not be detected.

Figure 11-2 shows a flowchart of watchdog timer processing.

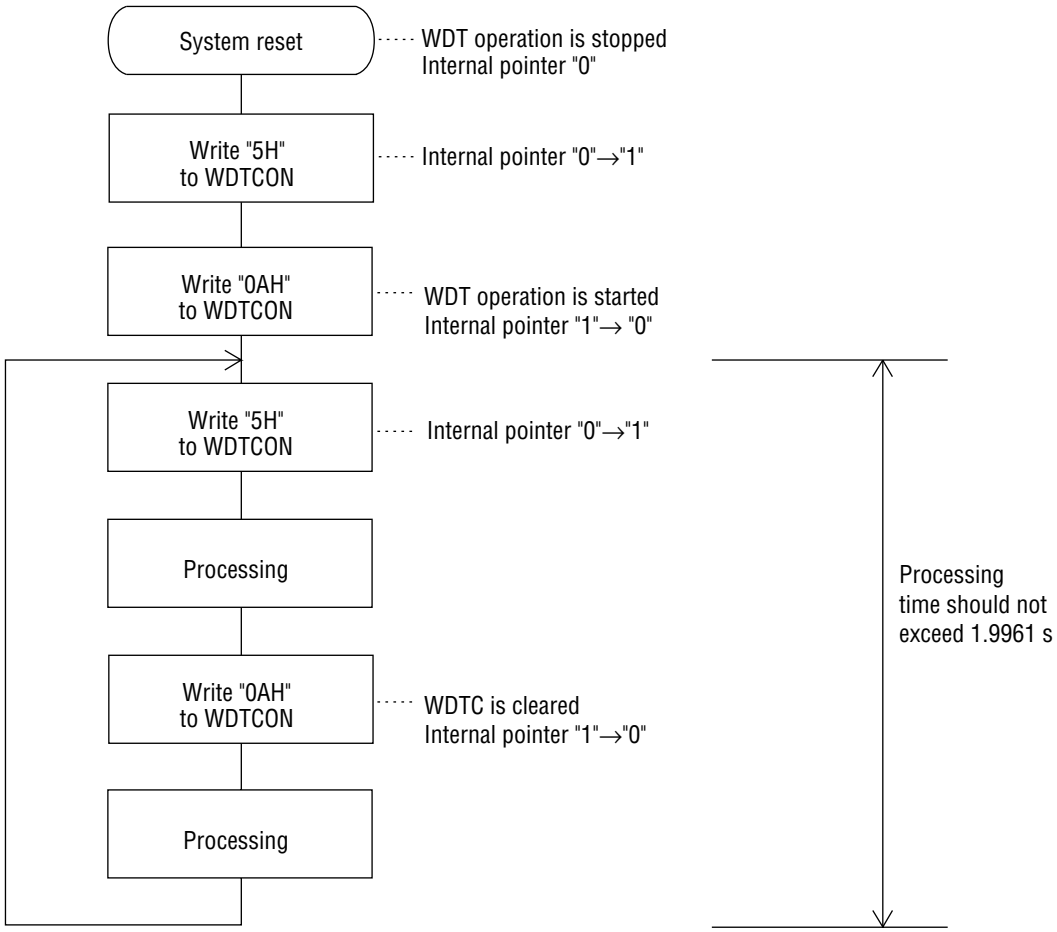


Figure 11-2 Watchdog Timer Processing Flowchart

Figure 11-3 shows the timing chart for watchdog timer operation.

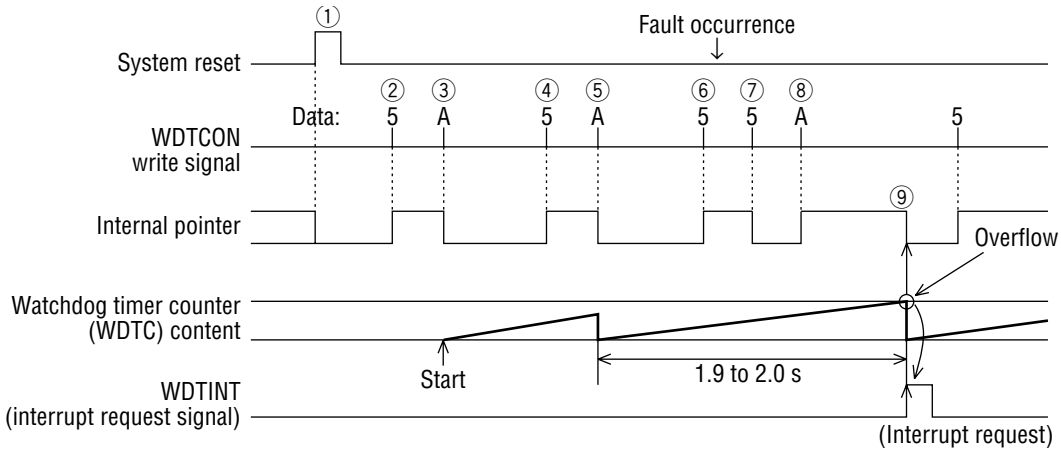


Figure 11-3 Watchdog Timer Operation Timing Chart

The watchdog timer operating sequence is listed below.

① System reset clears the internal pointer and WDTC.

② Write "5H" to WDTCON. (Internal pointer 0→1)

③ Write "0AH" to WDTCON to start WDTC. (Internal pointer 1→0)

④ Write "5H" to WDTCON. (Internal pointer 0→1)

⑤ Write "0AH" to WDTCON to clear WDTC. (Internal pointer 1→0)

⑥ Write "5H" to WDTCON. (Internal pointer 0→1)

⑦ After a fault occurs, "5H" is written to WDTCON but is not accepted since the internal pointer is "1". (Internal pointer 1→0)

⑧ "0AH" is written to WDTCON, but since the internal pointer is "0" and the write of "5H" in step ⑦ was not accepted, WDTC will not be cleared. (Internal pointer 0→1)

⑨ Because WDTC was not cleared, overflow of WDTC will generate the watchdog timer interrupt WDTINT. At this time, the internal pointer is cleared to "0".

Chapter 12

Ports (INPUT, I/O PORT)

Chapter 12 Ports (INPUT, I/O PORT)

12.1 Overview

The ML63187 has two 4-bit I/O ports.

The ML63189B has one 4-bit input port and four 4-bit I/O ports.

The ML63193 has one 4-bit input port and five 4-bit I/O ports.

The V_{DDI} (interface power supply) pin supplies power to the ports.

If a port is to be connected to an external device that operates on a different power supply, the power supply of the external device must be fed to the V_{DDI} pin.

Note:

Since V_{DDI} is separated from the positive power supply pin (V_{DD}), power must be supplied to the V_{DDI} pin.

12.2 Ports List

The ports of the ML63187, ML63189B, and ML63193 are shown in Table 12-1.

Table 12-1 Ports List

Port	I/O	Interrupt	Sedondary function	ML63187	ML63189B	ML63193	Page
Port 0	I	●	●	—	●	●	12-2
Port 9	I/O	—	●	—	●	●	12-7
Port A		—	●	—	●	●	12-7
Port B		●	●	●	●	●	12-12
Port C		●	●	—	—	●	12-18
Port E		●	●	●	●	●	12-25

12.3 Port 0 (P0.0–P0.3)

12.3.1 Port 0 Configuration

The ML63189B and ML63193 have Port 0, a 4-bit input-only port.

Figure 12-1 shows the configuration of port 0.

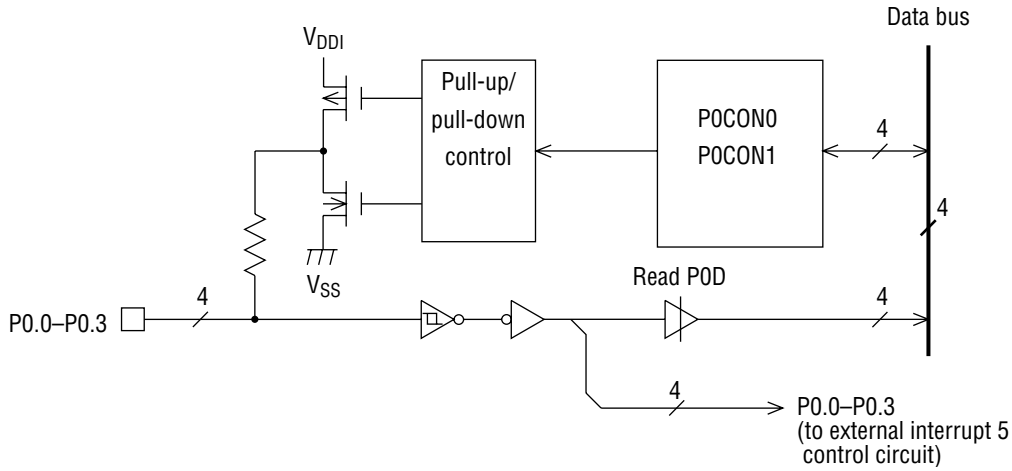
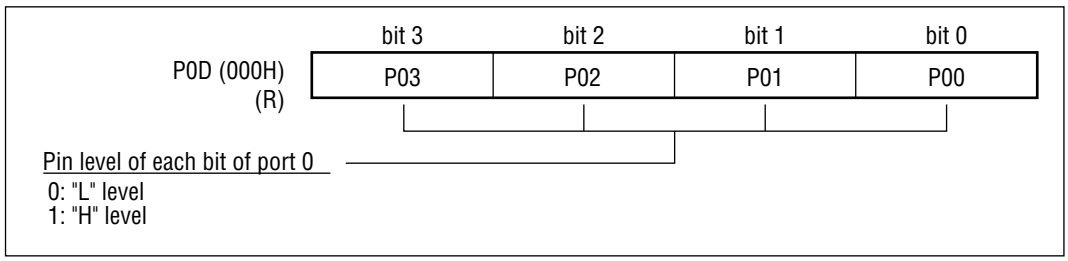


Figure 12-1 Input-Only Port (Port 0) Configuration

12.3.2 Port 0 Registers

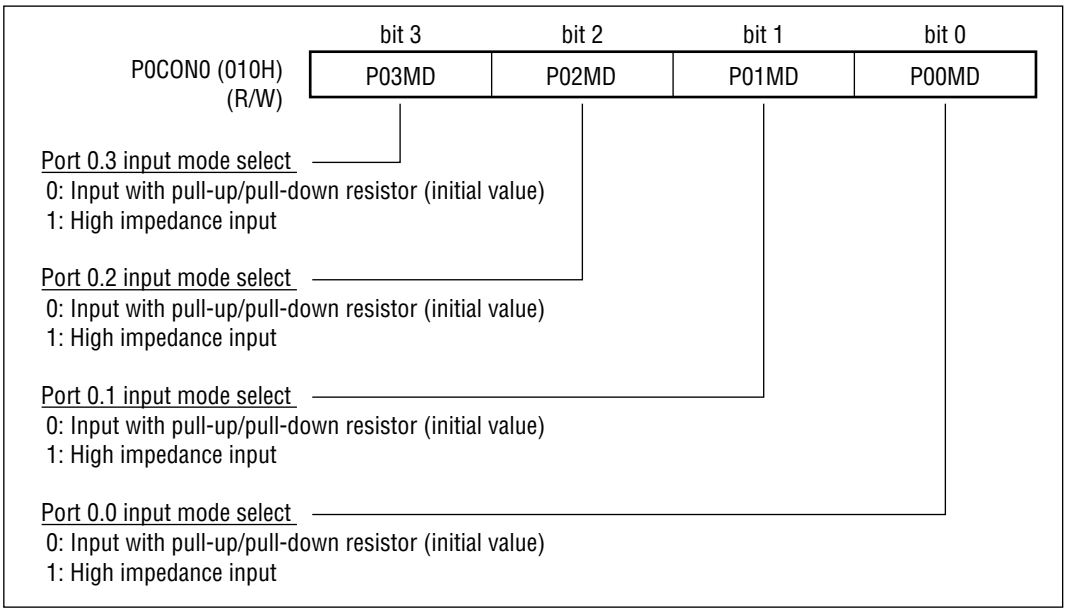
(1) Port 0 data register (P0D)

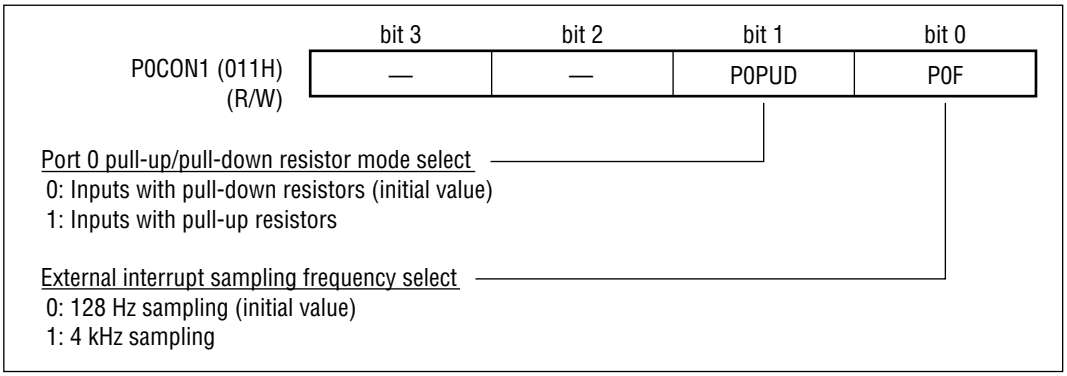
The port 0 data register (P0D) is a 4-bit read-only special function register (SFR) used to read the pin level of each bit of port 0.



(2) Port 0 control registers (P0CON0, P0CON1)

The port 0 control registers 0/1 (P0CON0, P0CON1) are 4-bit special function registers (SFRs) that select pull-up or pull-down resistors and select the external interrupt sampling frequency of Port 0 secondary function.





bit 1: P0PUD

This bit is used to select pull-up or pull-down resistors when any of the port 0 pins are selected by P0CON0 as an input with pull-up/pull-down resistor.

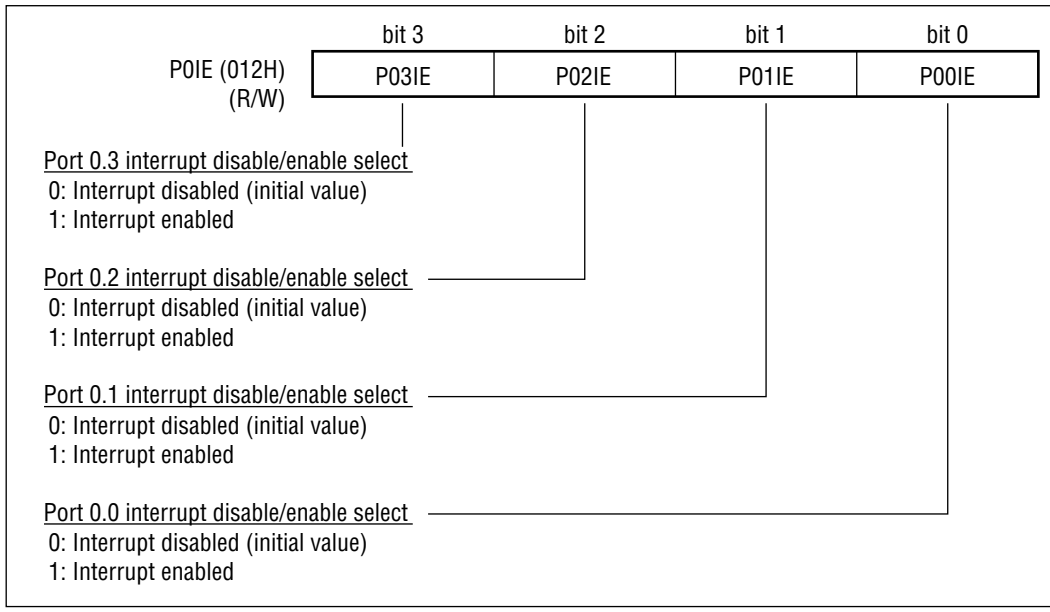
Setting P0PUD to "0" selects pull-down resistors, and setting to "1" selects pull-up resistors.

Individual specification of pull-down or pull-up resistors for the pins of port 0.0 to 0.3 is not possible.

(3) Port 0 interrupt enable register (P0IE)

The port 0 interrupt enable register (P0IE) is a 4-bit special function register (SFR) that enables/disables individual bits when port 0 is used as an external interrupt.

At system reset, all bits in the port interrupt enable register are cleared to "0" and port 0 is initialized to the interrupt disabled state.



12.3.3 Port 0 External Interrupt Function (External Interrupt 5)

An external interrupt (external interrupt 5) is assigned to port 0 as a secondary function. Individual bits can be enabled/disabled for external interrupt 5.

External interrupt generation for each input of port 0 is triggered by the falling edge of either the 128 Hz or 4 kHz sampling clock from the time base counter.

After the port level changes, interrupt request signal XI5INT is output and external interrupt 5 request flag (QXI5) is set. The maximum time delay from the change in port level until setting QXI5 is one cycle of the sampling clock (128 Hz or 4 kHZ).

Because the port 0 external interrupt 5 is set by a level change at any of the port 0 inputs, each bit of the port must be read to determine which bit of port 0 generated the interrupt.

External interrupt 5 is generated during the following states.

P0PUD = "0" (initial value: inputs with pull-down resistors) setting

With all P0.0 to P0.3 inputs at a "L" level, external interrupt 5 is generated when any port 0 input changes to a "H" level.

With any of P0.0 to P0.3 inputs at a "H" level, external interrupt 5 is generated when all the port 0 inputs change to a "L" level.

P0PUD = "1" (initial value: inputs with pull-up resistors) setting

With all P0.0 to P0.3 inputs at a "H" level, external interrupt 5 is generated when any port 0 input changes to a "L" level.

With any of P0.0 to P0.3 inputs at a "L" level, external interrupt 5 is generated when all the port 0 inputs change to a "H" level.

The interrupt vector address for external interrupt 5 is 001EH.

Figure 12-2 shows the timing for generation of external interrupt 5.

Figure 12-3 shows an equivalent circuit of external interrupt 5 control.

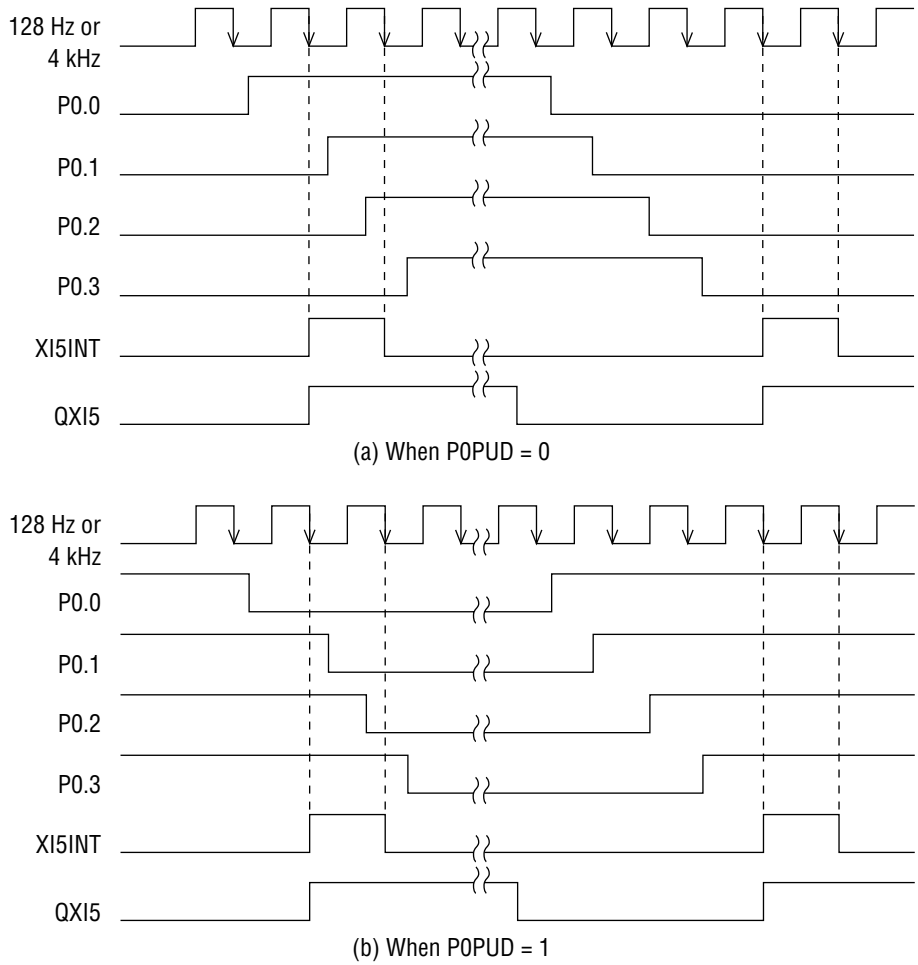


Figure 12-2 Interrupt Generation Timing of External Interrupt 5

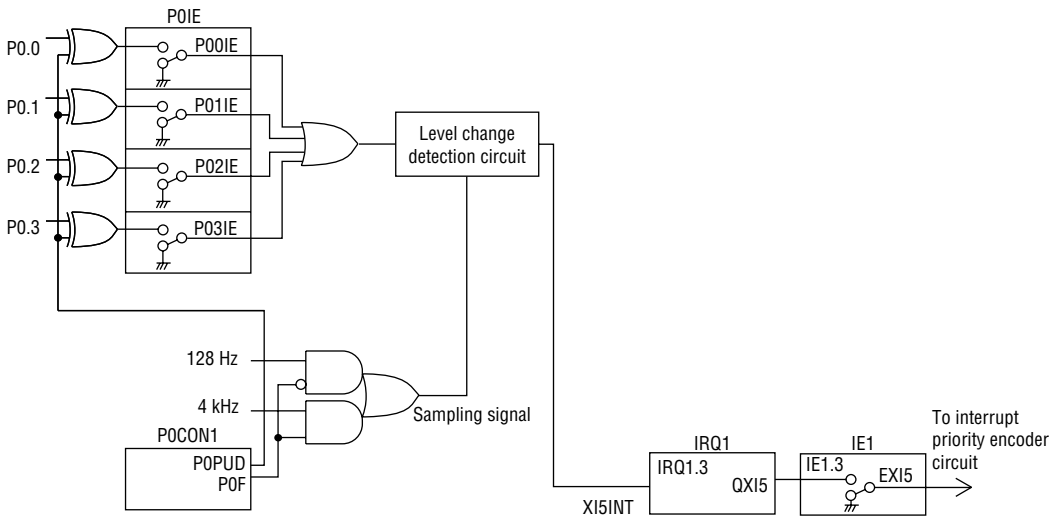


Figure 12-3 Equivalent Circuit of External Interrupt 5 Control

12.4 Port 9, Port A (P9.0–P9.3, PA.0–PA.3)

The ML63189B and ML63193 have Port 9 and Port A, 4-bit input/output ports.

12.4.1 Port 9, Port A Configuration

The circuit configurations for ports 9 and A are shown in Figure 12-4.

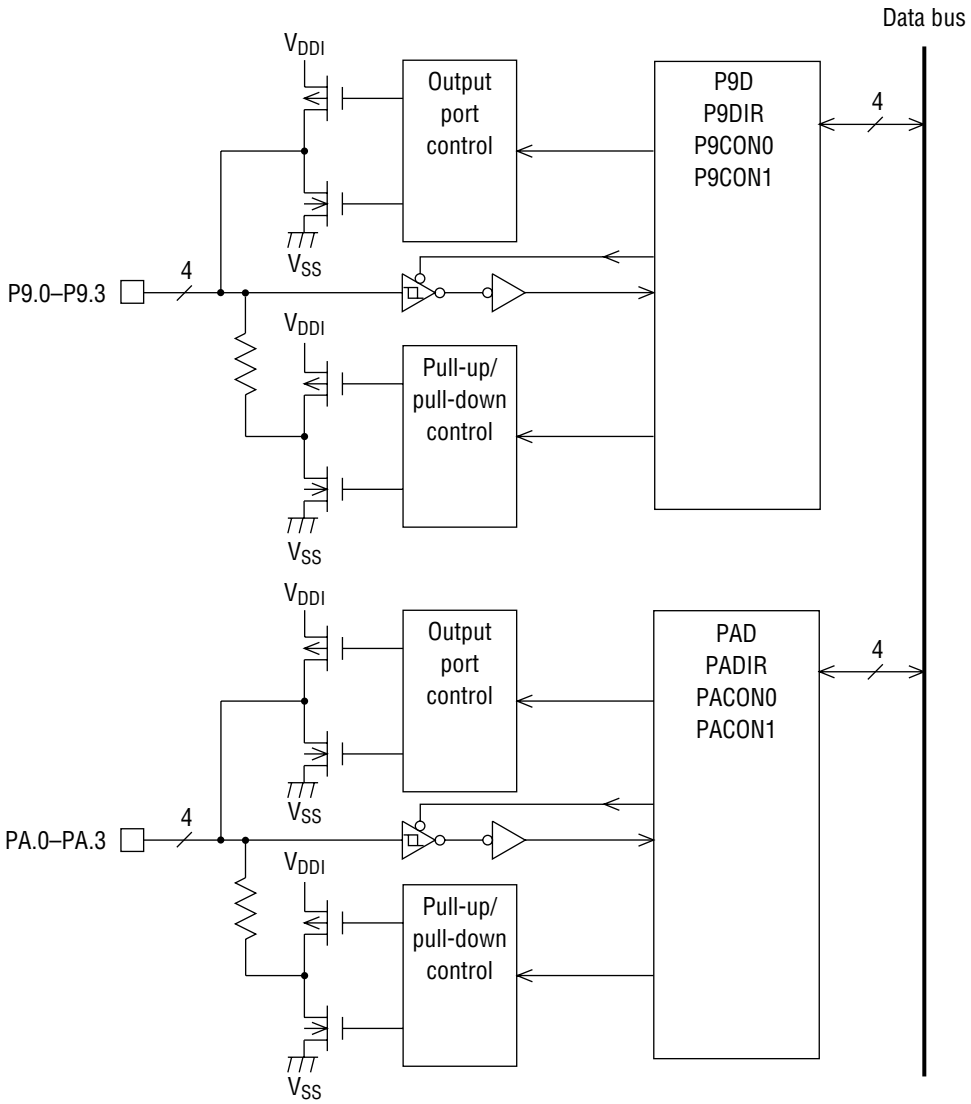


Figure 12-4 Input/Output Port (Ports 9 and A) Configuration

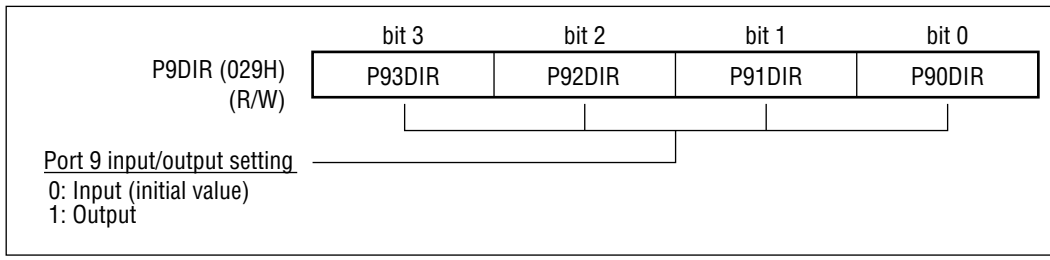
12.4.2 Port 9, Port A Registers

(1) Port 9, Port A direction registers (P9DIR, PADIR)

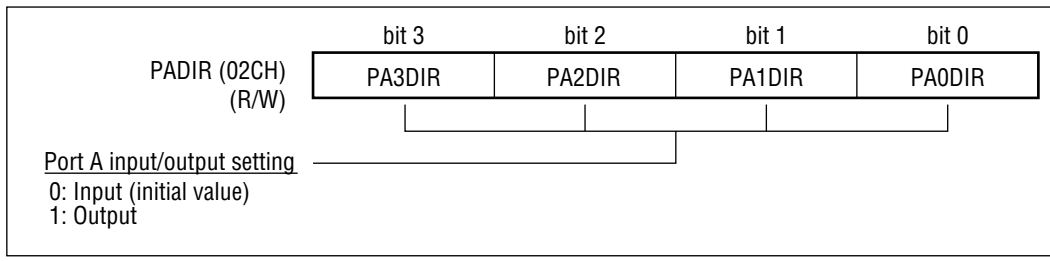
The port 9 direction register (P9DIR) and port A direction register (PADIR) are 4-bit special function registers (SFRs) which specify the port input/output direction for each bit. Pins corresponding to P9DIR and PADIR bits set to "0" are input, and those corresponding to bits set to "1" are output.

At system reset all bits in P9DIR and PADIR are set to "0", and ports 9 and A are initialized to input mode.

• Port 9



• Port A



(2) Port 9, Port A data registers (P9D, PAD)

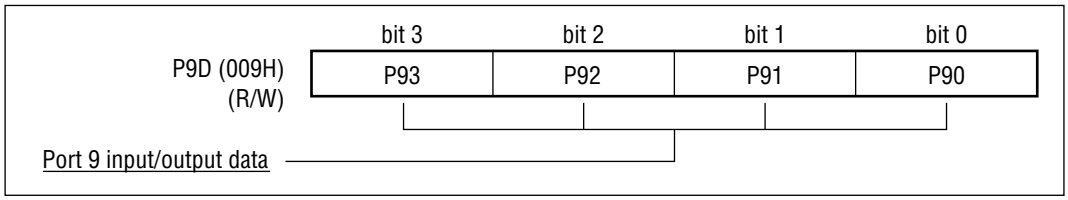
The port 9 data register (P9D) and port A data register (PAD) are 4-bit special function registers (SFRs) used to set the output values for the ports.

When a bit in the port direction register (P9DIR, PADIR) is set to "1" to select the output mode, the content of the corresponding bit in the port data register (P9D, PAD) is output to the port (port 9, port A).

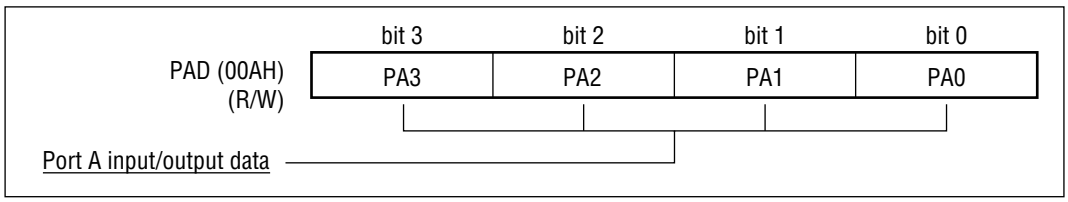
When a bit in the port data register (P9D, PAD) is read with the corresponding port direction register bit set to output, the value of the bit in the port data register is read.

When a bit in the port data register (P9D, PAD) is read with the corresponding port direction register bit set to "0" (input mode), the level of the corresponding pin is read.

• Port 9



• Port A



At system reset all bits in the port 9 and A data registers are set to "0". When data is written to a port data register, the actual pin change timing is at the rising edge of the system clock for state 2 of the write instruction.

Figure 12-5 shows port change timing.

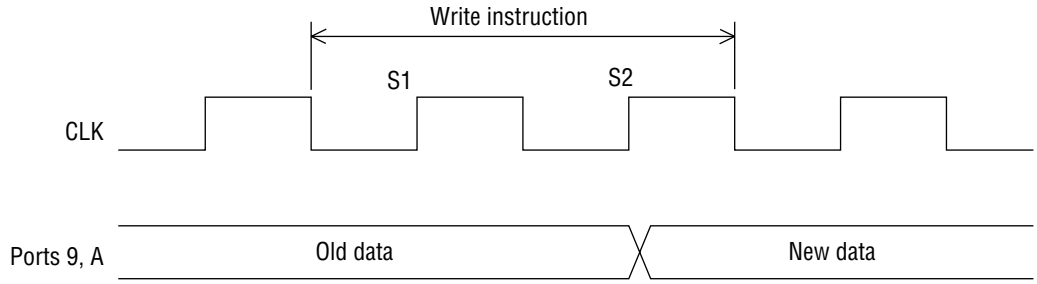


Figure 12-5 Port Change Timing

(3) Port 9, Port A control registers (P9CON0, P9CON1, PACON0, PACON1)

The port 9 control registers 0/1 (P9CON0, P9CON1) and port A control registers 0/1 (PACON0, PACON1) are 4-bit special function registers (SFRs) used to select port input/ output mode.

The input mode may be pull-down resistor input, pull-up resistor input or high-impedance input.

The output mode may be CMOS output, N-channel open drain output, P-channel open drain output or high-impedance output.

• Port 9

P9CON0 (027H) (R/W)

bit 3	bit 2	bit 1	bit 0
P91MD1	P91MD0	P90MD1	P90MD0

Port 9.1 input/output mode select

Input mode

bit 3	bit 2	
0	0	: Input with pull-down resistor (initial value)
1	0	: Input with pull-up resistor
×	1	: High-impedance input

Output mode

bit 3	bit 2	
0	0	: CMOS output (initial value)
0	1	: N-channel open drain output
1	0	: P-channel open drain output
1	1	: High-impedance output

Port 9.0 input/output mode select

Input mode

bit 1	bit 0	
0	0	: Input with pull-down resistor (initial value)
1	0	: Input with pull-up resistor
×	1	: High-impedance input

Output mode

bit 1	bit 0	
0	0	: CMOS output (initial value)
0	1	: N-channel open drain output
1	0	: P-channel open drain output
1	1	: High-impedance output

P9CON1 (028H) (R/W)

bit 3	bit 2	bit 1	bit 0
P93MD1	P93MD0	P92MD1	P92MD0

Port 9.3 input/output mode select

Input mode

bit 3	bit 2	
0	0	: Input with pull-down resistor (initial value)
1	0	: Input with pull-up resistor
×	1	: High-impedance input

Output mode

bit 3	bit 2	
0	0	: CMOS output (initial value)
0	1	: N-channel open drain output
1	0	: P-channel open drain output
1	1	: High-impedance output

Port 9.2 input/output mode select

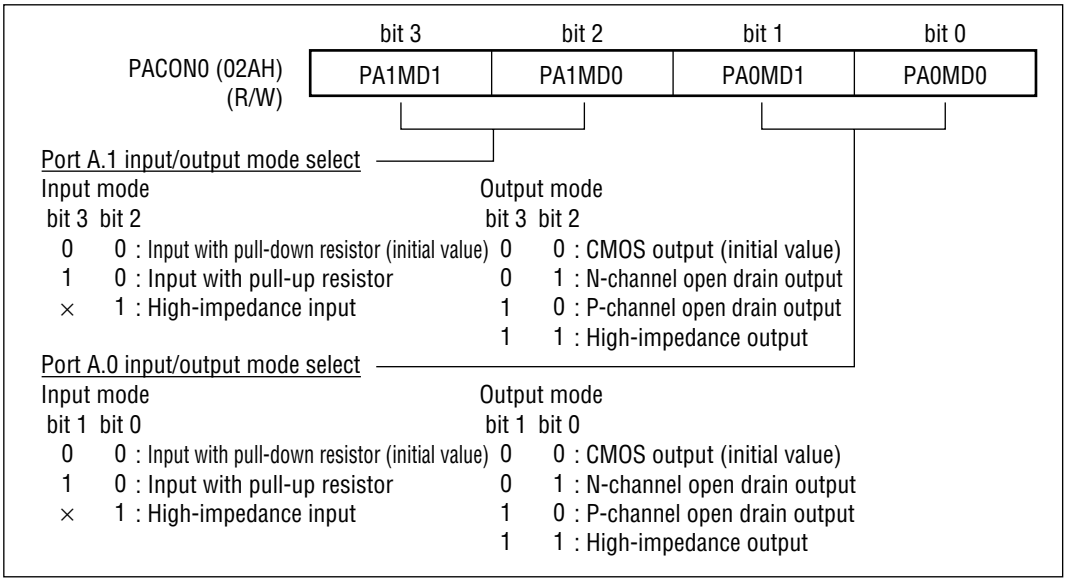
Input mode

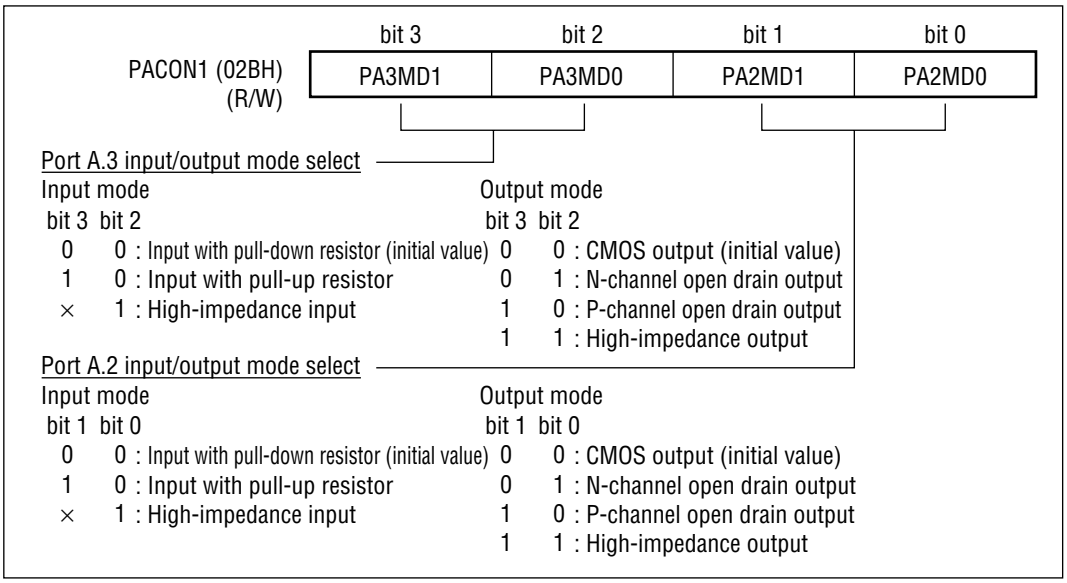
bit 1	bit 0	
0	0	: Input with pull-down resistor (initial value)
1	0	: Input with pull-up resistor
×	1	: High-impedance input

Output mode

bit 1	bit 0	
0	0	: CMOS output (initial value)
0	1	: N-channel open drain output
1	0	: P-channel open drain output
1	1	: High-impedance output

• Port A


bit 3
bit 2
bit 1
bit 0
PACON0 (02AH)
(R/W)
PA1MD1
PA1MD0
PA0MD1
PA0MD0
Port A.1 input/output mode select
Input mode
bit 3 bit 2
0 0 : Input with pull-down resistor (initial value)
1 0 : Input with pull-up resistor
× 1 : High-impedance input
Output mode
bit 3 bit 2
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output
Port A.0 input/output mode select
Input mode
bit 1 bit 0
0 0 : Input with pull-down resistor (initial value)
1 0 : Input with pull-up resistor
× 1 : High-impedance input
Output mode
bit 1 bit 0
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output


bit 3
bit 2
bit 1
bit 0
PACON1 (02BH)
(R/W)
PA3MD1
PA3MD0
PA2MD1
PA2MD0
Port A.3 input/output mode select
Input mode
bit 3 bit 2
0 0 : Input with pull-down resistor (initial value)
1 0 : Input with pull-up resistor
× 1 : High-impedance input
Output mode
bit 3 bit 2
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output
Port A.2 input/output mode select
Input mode
bit 1 bit 0
0 0 : Input with pull-down resistor (initial value)
1 0 : Input with pull-up resistor
× 1 : High-impedance input
Output mode
bit 1 bit 0
0 0 : CMOS output (initial value)
0 1 : N-channel open drain output
1 0 : P-channel open drain output
1 1 : High-impedance output

12.5 Port B (PB.0–PB.3)

The ML63187, ML63189B, and ML63193 have Port B, a 4-bit input/output port.

12.5.1 Port B Configuration

The circuit configuration for port B is shown in Figure 12-6.

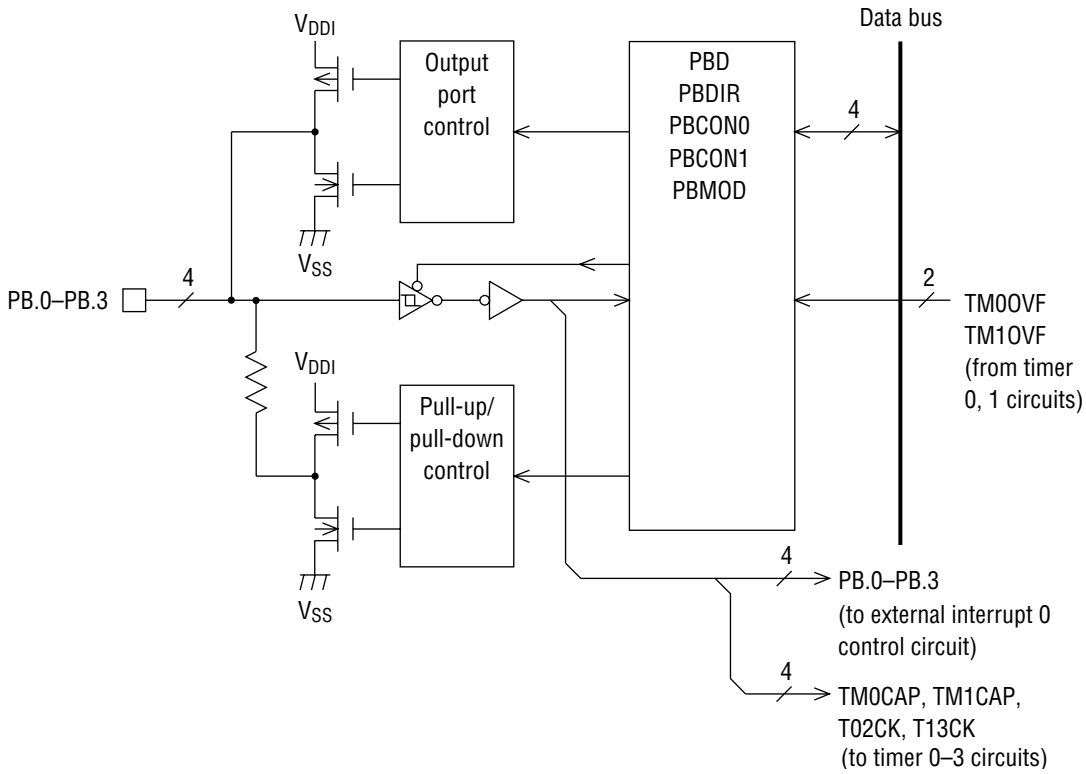


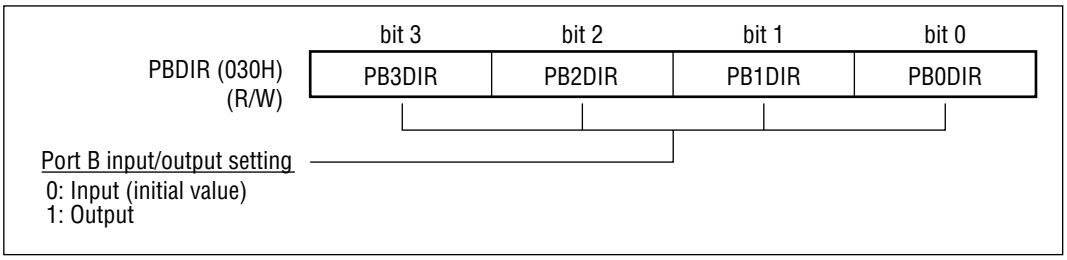
Figure 12-6 Input /Output Port (Port B) Configuration

12.5.2 Port B Registers

(1) Port B direction register (PBDIR)

PBDIR is a 4-bit special function register (SFR) which specifies the port input/output direction for each bit. Pins corresponding to PBDIR bits set to "0" are input, and those corresponding to bits set to "1" are output.

At system reset all bits in the port B direction register are reset to "0", and port B is initialized to input mode.



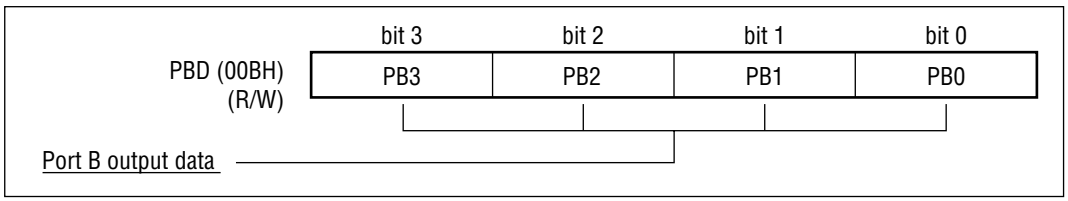
(2) Port B data register (PBD)

PBD is a 4-bit special function register used to set the output values for port B.

When a bit in the port B direction register (PBDIR) is set to "1" to select the output mode, the content of the corresponding bit in the port B data register is output to the port B.

When a bit in the port B data register is read with the corresponding PBDIR bit set to output, the value of the bit in the port B data register is read.

When a bit in the port B data register is read with the corresponding PBDIR bit set to "0" (input mode), the level of the corresponding pin of port B is read.



At system reset all bits in the port B data register (PBD) are set to "0". When data is written to the port B data register, the actual pin change timing is at the rising edge of the system clock for state 2 of the write instruction.

Figure 12-7 indicates port change timing.

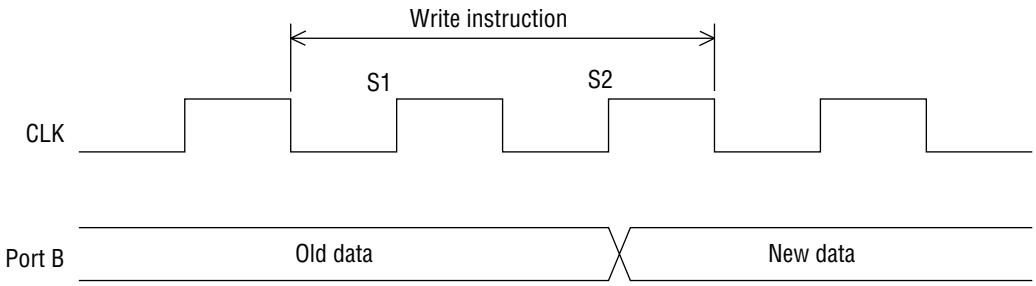


Figure 12-7 Port B Change Timing

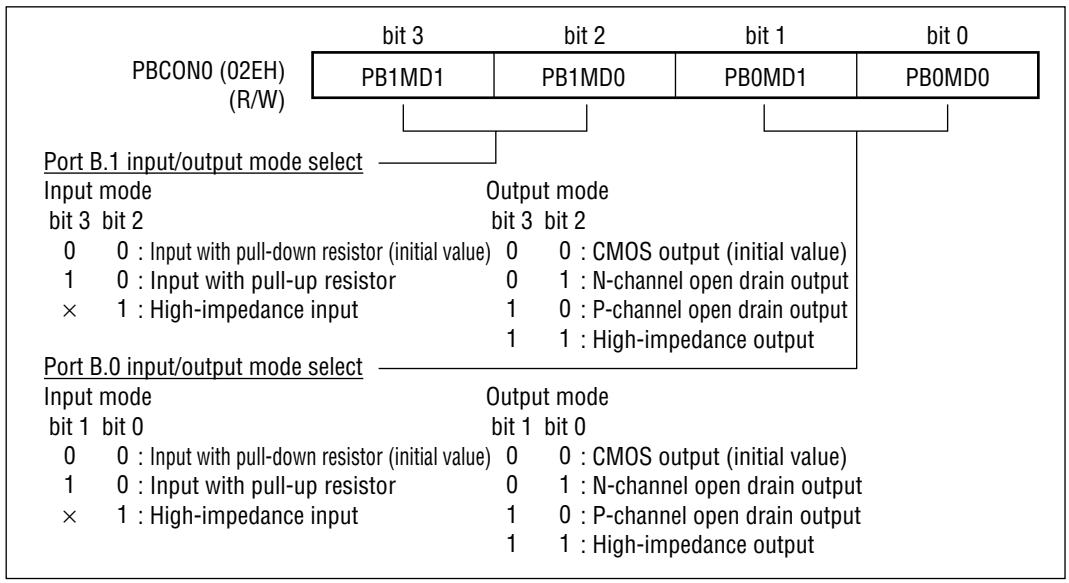
(3) Port B control registers (PBCON0, PBCON1)

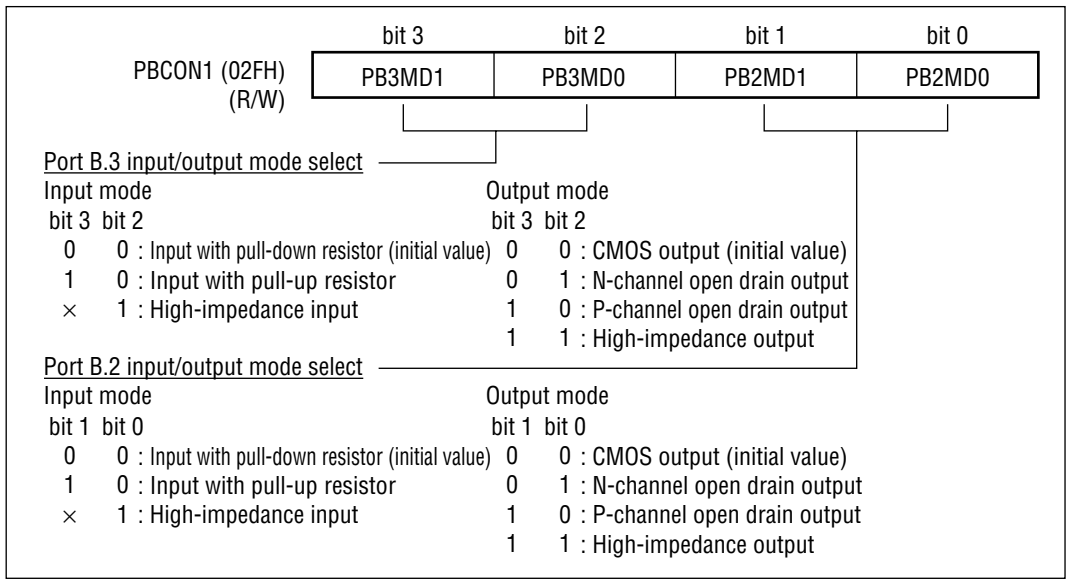
The port B control registers 0/1 (PBCON0, PBCON1) are 4-bit special function registers (SFRs) used to select port input/output mode.

The input mode can be pull-down resistor input, pull-up resistor input or high-impedance input.

The output mode can be CMOS output, N-channel open drain output, P-channel open drain output or high-impedance output.

At system reset all bits in PBCON0 and PBCON1 are set to "0", and port B is initialized to pull-down resistor input mode and CMOS output mode.





(4) Port B mode register (PBMOD)

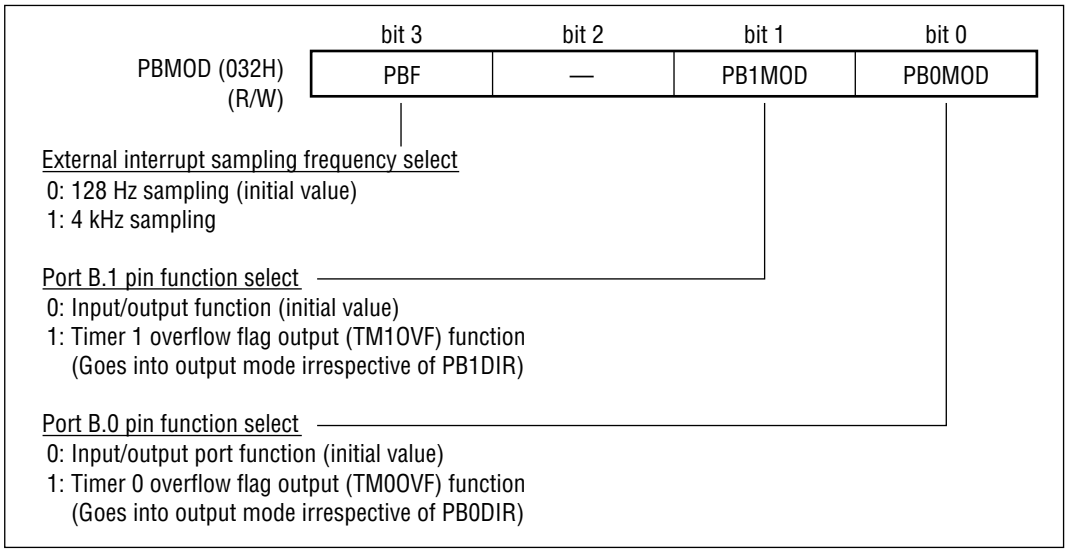
PBMOD is a 4-bit special function register (SFR) used to select the sampling frequency when port B is used as an external interrupt. It is also used to select port B secondary functions other than external interrupt.

The external interrupt sampling frequency can be selected as either 128 Hz or 4 kHz.

Port B secondary functions are indicated in Table 12-2.

Table 12-2 Port B Secondary Functions

Port	Secondary function	Description
PB.0	TM0CAP	Timer 0 capture input
PB.1	TM1CAP	Timer 1 capture input
PB.2	T02CK	Timer 0, timer 2 external clock input
PB.3	T13CK	Timer 1, timer 3 external clock input
PB.0	TM0OVF	Timer 0 overflow flag output
PB.1	TM1OVF	Timer 1 overflow flag output
PB.0	INT0	External interrupt 0
PB.1		
PB.2		
PB.3		

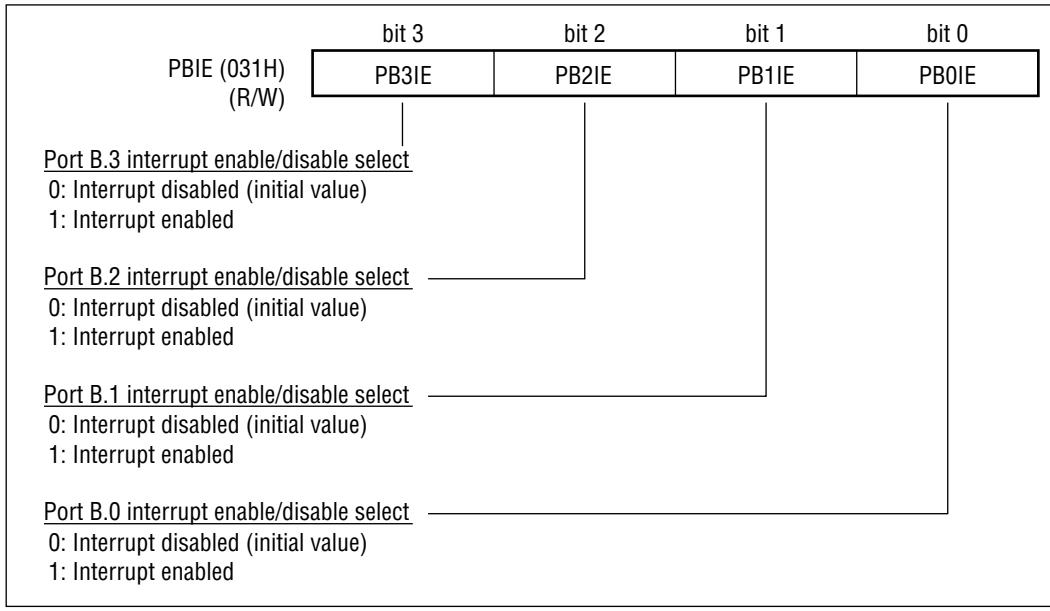


At system reset all the valid bits in PBMOD are initialized to "0".

(5) Port B interrupt enable register (PBIE)

PBIE is a 4-bit special function register (SFR) that enables/disables individual bits when port B is used as an external interrupt input.

At system reset, all bits in PBIE are cleared to "0" and port B is initialized to the interrupt disabled state.



12.5.3 Port B External Interrupt Function (External Interrupt 0)

Port B has external interrupt 0 allocated as secondary function. Individual bits of port B can be enabled/disabled.

External interrupt generation for port B is triggered by the falling edge of the 128 Hz or 4 kHz time base counter, which is the sampling clock.

After the port level changes, the interrupt request signal (XI0INT) is output, and the interrupt request flag (QXI0) is set. The maximum delay for this sequence is one cycle of the sampling clock (128 Hz or 4 kHz).

Because the port B external interrupt is set by a level change at any of the port B inputs, each bit of the port must be read to determine which bit of port B generated the interrupt.

The interrupt start address for external interrupt 0 is 0014H.

Figure 12-8 shows the external interrupt 0 generation timing.

Figure 12-9 shows the equivalent circuit for external interrupt 0 control.

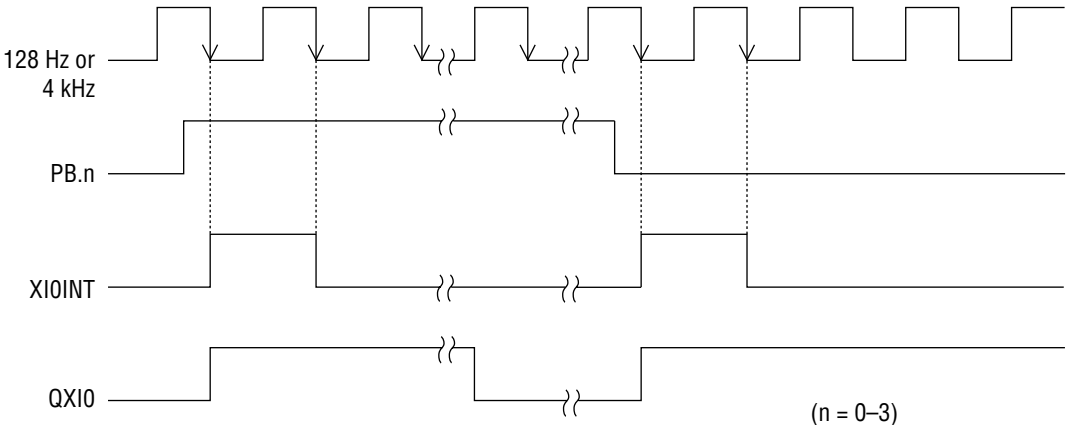


Figure 12-8 External Interrupt 0 Generation Timing

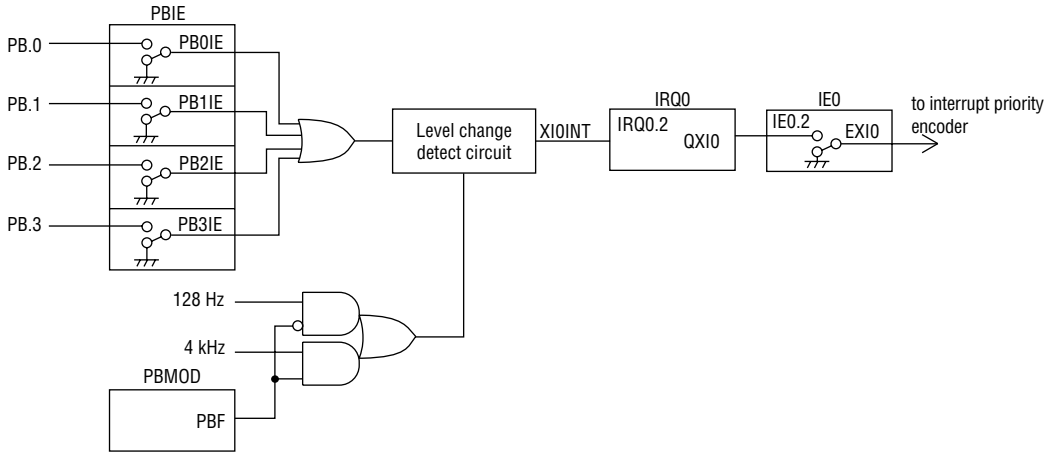


Figure 12-9 External Interrupt 0 Control Equivalent Circuit

12.6 Port C (PC.0–PC.3)

The ML63193 has Port C, a 4-bit input/output port.

12.6.1 Port C Configuration

The circuit configuration for port C is shown in Figure 12-10.

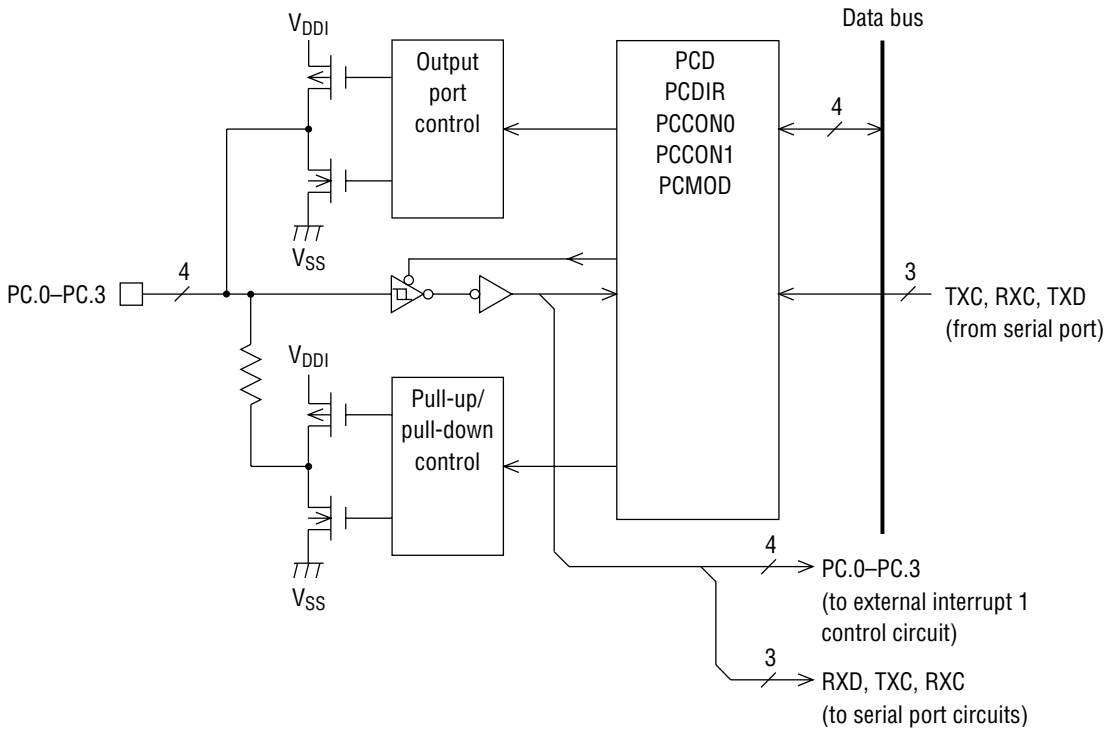


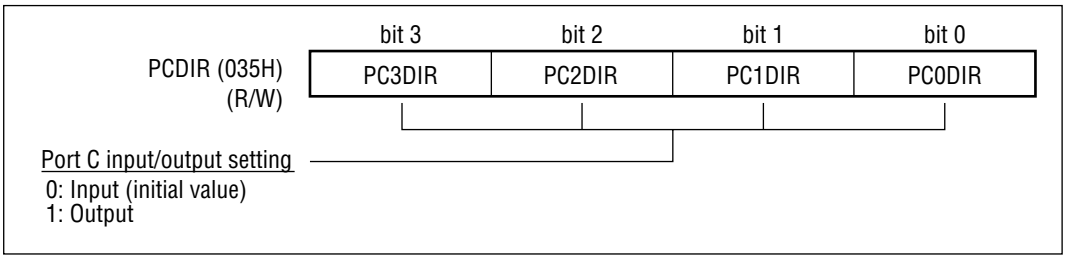
Figure 12-10 Input /Output Port (Port C) Configuration

12.6.2 Port C Registers

(1) Port C direction register (PCDIR)

PCDIR is a 4-bit special function register (SFR) which specifies the port input/output direction for each bit. Pins corresponding to PCDIR bits set to "0" are input, and those corresponding to bits set to "1" are output.

At system reset all bits in the port C direction register are reset to "0", and port C is initialized to input mode.



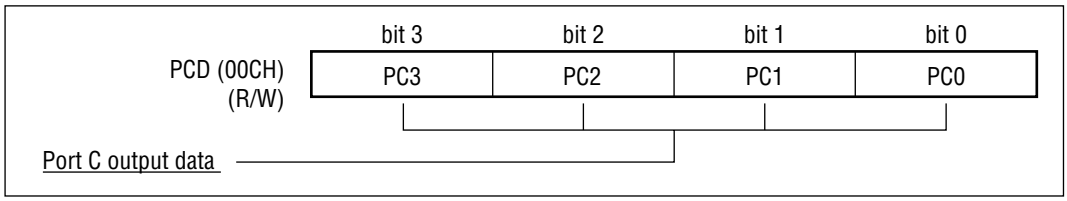
(2) Port C data register (PCD)

PCD is a 4-bit special function register used to set the output values for port C.

When a bit in the port C direction register (PCDIR) is set to "1" to select the output mode, the content of the corresponding bit in the port C data register is output to the port C.

When a bit in the port C data register is read with the corresponding PCDIR bit set to output, the value of the bit in the port C data register is read.

When a bit in the port C data register is read with the corresponding PCDIR bit set to "0" (input mode), the level of the corresponding pin of port C is read.



At system reset all bits in the port C data register (PCD) are set to "0". When data is written to the port C data register, the actual pin change timing is at the rising edge of the system clock for state 2 of the write instruction.

Figure 12-11 indicates port change timing.

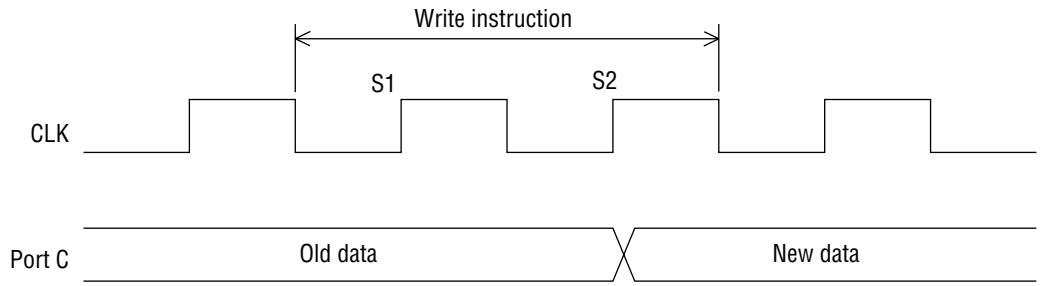


Figure 12-11 Port C Change Timing

(3) Port C control registers (PCCON0, PCCON1)

The port C control registers 0/1 (PCCON0, PCCON1) are 4-bit special function registers (SFRs) used to select port input/output mode.

The input mode can be pull-down resistor input, pull-up resistor input or high-impedance input.

The output mode can be CMOS output, N-channel open drain output, P-channel open drain output or high-impedance output.

At system reset all bits in PCCON0 and PCCON1 are set to "0", and port C is initialized to pull-down resistor input mode and CMOS output mode.

PCCON0 (033H) (R/W)

bit 3	bit 2	bit 1	bit 0
PC1MD1	PC1MD0	PC0MD1	PC0MD0

Port C.1 input/output mode select

Input mode

bit 3	bit 2	
0	0	: Input with pull-down resistor (initial value)
1	0	: Input with pull-up resistor
×	1	: High-impedance input

Output mode

bit 3	bit 2	
0	0	: CMOS output (initial value)
0	1	: N-channel open drain output
1	0	: P-channel open drain output
1	1	: High-impedance output

Port C.0 input/output mode select

Input mode

bit 1	bit 0	
0	0	: Input with pull-down resistor (initial value)
1	0	: Input with pull-up resistor
×	1	: High-impedance input

Output mode

bit 1	bit 0	
0	0	: CMOS output (initial value)
0	1	: N-channel open drain output
1	0	: P-channel open drain output
1	1	: High-impedance output

PCCON1 (034H) (R/W)

bit 3	bit 2	bit 1	bit 0
PC3MD1	PC3MD0	PC2MD1	PC2MD0

Port C.3 input/output mode select

Input mode

bit 3	bit 2	
0	0	: Input with pull-down resistor (initial value)
1	0	: Input with pull-up resistor
×	1	: High-impedance input

Output mode

bit 3	bit 2	
0	0	: CMOS output (initial value)
0	1	: N-channel open drain output
1	0	: P-channel open drain output
1	1	: High-impedance output

Port C.2 input/output mode select

Input mode

bit 1	bit 0	
0	0	: Input with pull-down resistor (initial value)
1	0	: Input with pull-up resistor
×	1	: High-impedance input

Output mode

bit 1	bit 0	
0	0	: CMOS output (initial value)
0	1	: N-channel open drain output
1	0	: P-channel open drain output
1	1	: High-impedance output

(4) Port C mode registers (PCMOD0, PCMOD1)

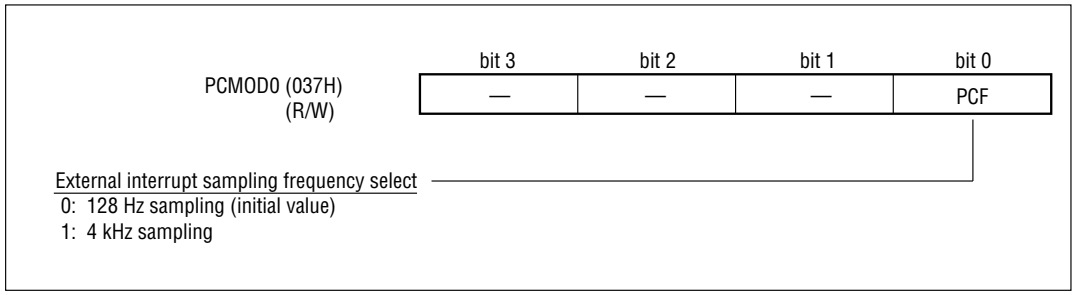
The port C mode registers 0/1 (PCMOD0, PCMOD1) are 4-bit special function registers (SFRs) used to select the sampling frequency when ports are used for external interrupt, and to select secondary functions other than external interrupt.

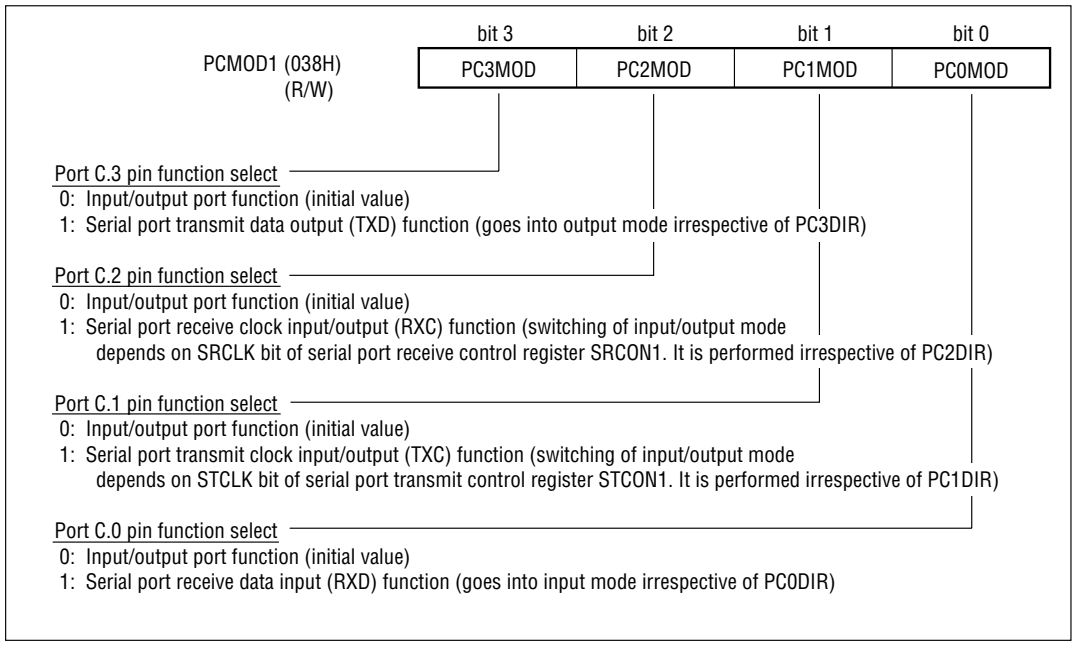
The external interrupt sampling frequency is either 128 Hz or 4 kHz.

Port C secondary functions are indicated in Table 12-3.

Table 12-3 Port C Secondary Functions

Port	Secondary function	Description
PC.0	RXD	Serial port receive data input
PC.1	TXC	Serial port transmit clock I/O
PC.2	RXC	Serial port receive clock I/O
PC.3	TXD	Serial port transmit data output
PC.0	INT1	External interrupt 1
PC.1		
PC.2		
PC.3		



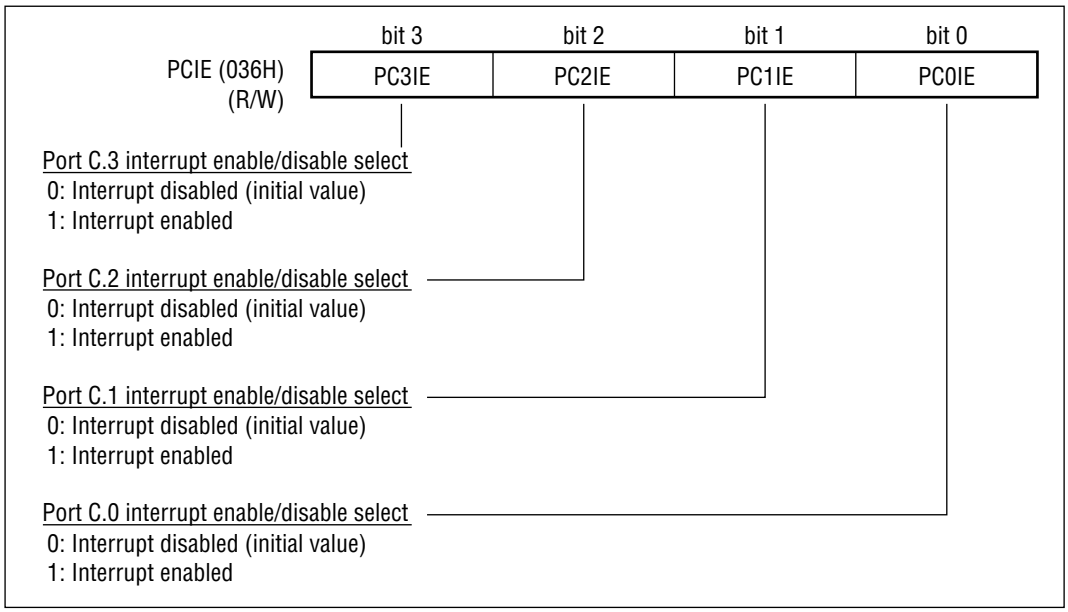


At system reset all the valid bits in the port C mode registers are initialized to "0".

(5) Port C interrupt enable register (PCIE)

PCIE is a 4-bit special function register (SFR) that enables/disables individual bits when port C is used as an external interrupt input.

At system reset, all bits in PCIE are cleared to "0" and port C is initialized to the interrupt disabled state.



12.6.3 Port C External Interrupt Function (External Interrupt 1)

Port C has external interrupt 1 allocated as secondary function. Individual bits of port C can be enabled/disabled.

External interrupt generation for port C is triggered by the falling edge of the 128 Hz or 4 kHz time base counter, which is the sampling clock.

After the port level changes, the interrupt request signal (XI1INT) is output, and the interrupt request flag (QXI1) is set. The maximum delay for this sequence is one cycle of the sampling clock (128 Hz or 4 kHz).

Because the port C external interrupt is set by a level change at any of the port C inputs, each bit of the port must be read to determine which bit of port C generated the interrupt.

The interrupt start address for external interrupt 1 is 0016H.

Figure 12-12 shows the external interrupt 1 generation timing.

Figure 12-13 shows the equivalent circuit for external interrupt 1 control.

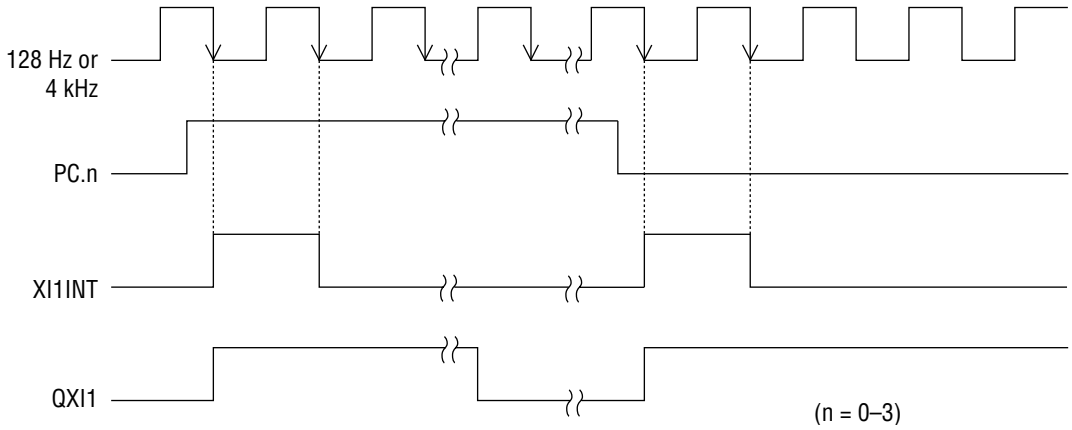


Figure 12-12 External Interrupt 1 Generation Timing

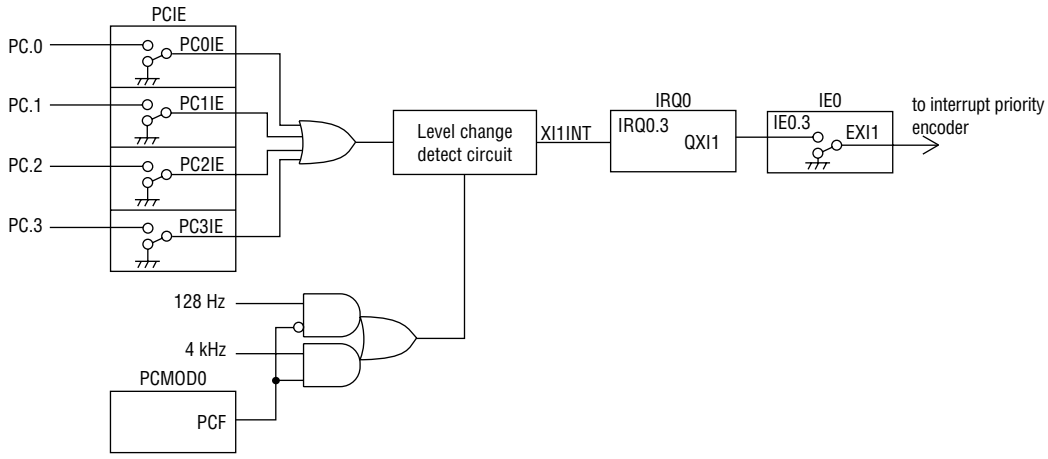


Figure 12-13 External Interrupt 1 Control Equivalent Circuit

12.7 Port E (PE.0–PE.3)

The ML63187, ML63189B, and ML63193 have Port E, a 4-bit input/output port.

12.7.1 Port E Configuration

The circuit configuration for port E is shown in Figure 12-14.

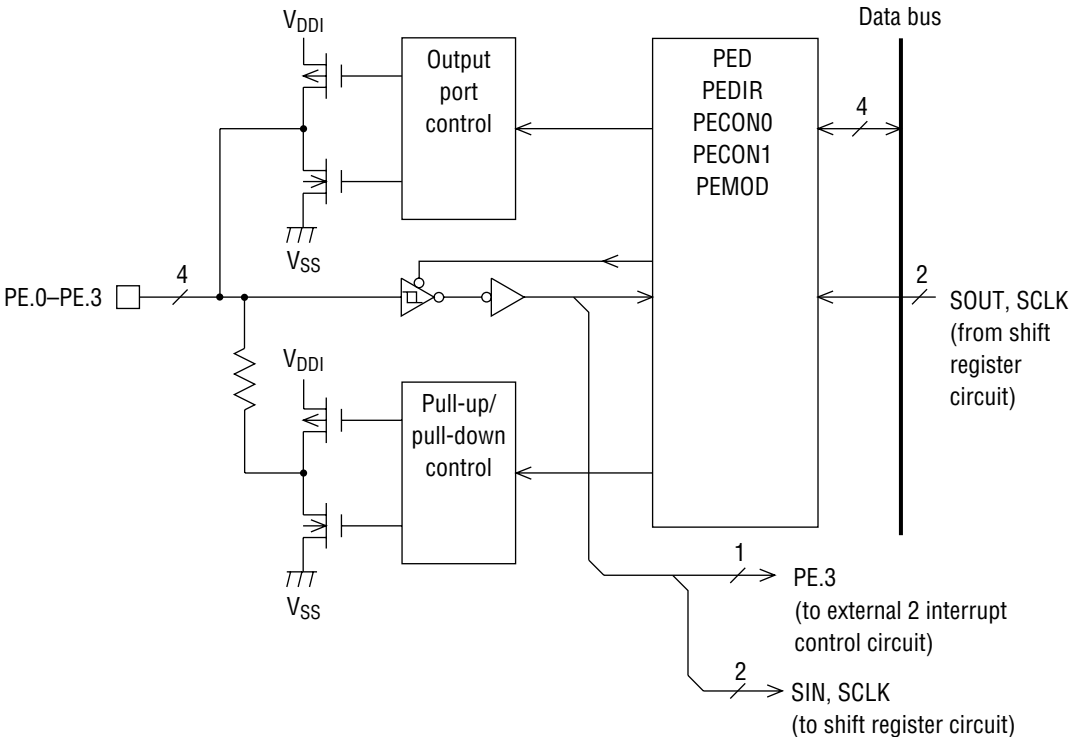


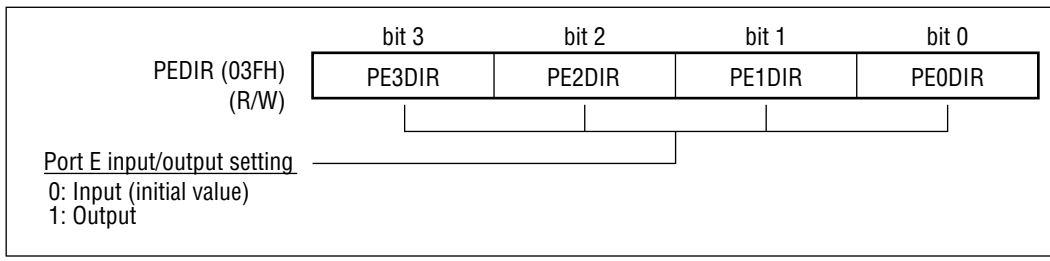
Figure 12-14 Input/Output Port (Port E) Configuration

12.7.2 Port E Registers

(1) Port E direction register (PEDIR)

PEDIR is a 4-bit special function register (SFR) which specifies the port input/output direction for each bit. Pins corresponding to PEDIR bits set to "0" are input, and those corresponding to bits set to "1" are output.

At system reset all bits in the port E direction register are set to "0", and port E is initialized to input mode.



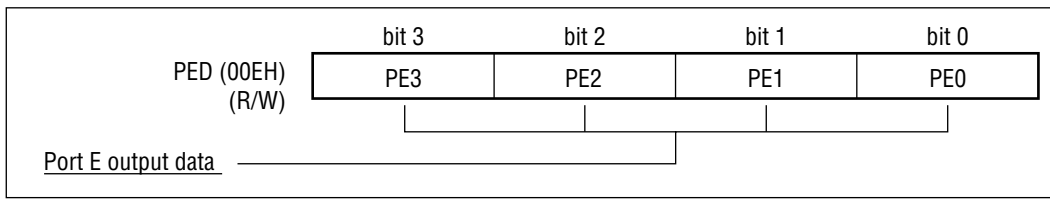
(2) Port E data register (PED)

PED is a 4-bit special function register used to set the output values for port E.

When a bit in the port E direction register (PEDIR) is set to "1" to select the output mode, the content of the corresponding bit in the port E data register is output to the port E.

When a bit in the port E data register is read with the corresponding PEDIR bit set to output, the value of the bit in the port E data register is read.

When a bit in the port E data register is read with the corresponding PEDIR bit set to "0" (input mode), the level of the corresponding pin of port E is read.



At system reset all bits in the port E data register (PED) are reset to "0". When data is written to the port E data register, the pin change timing is at the rising edge of the system clock for state 2 of the write instruction.

Figure 12-15 indicates port change timing.

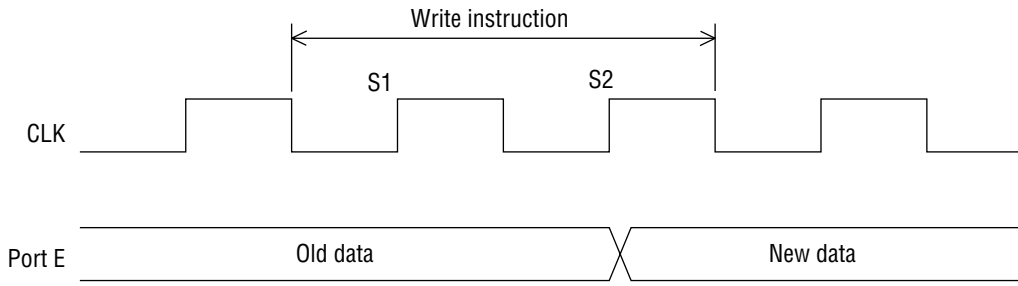


Figure 12-15 Port E Change Timing

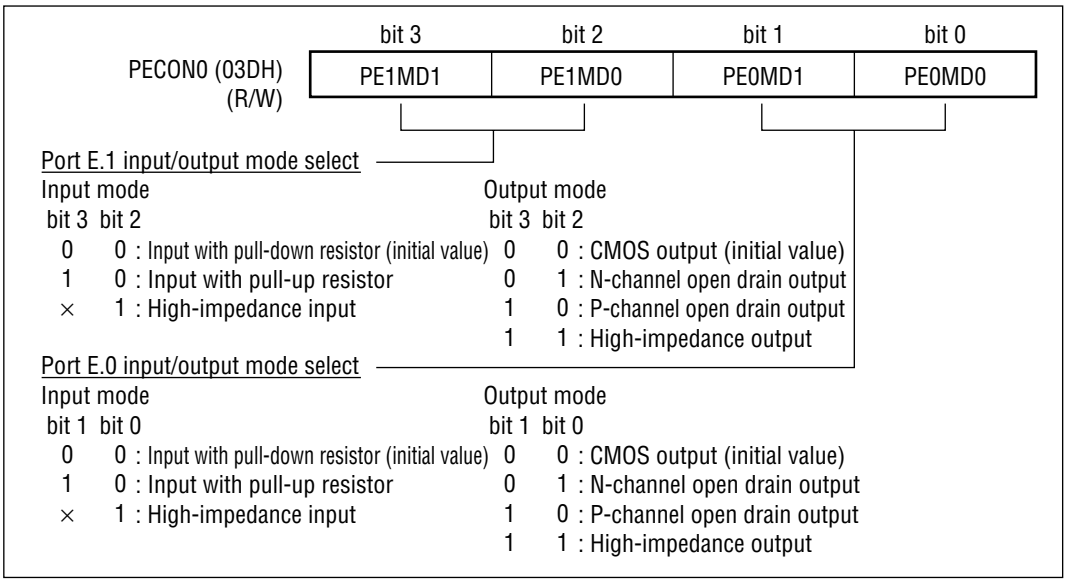
(3) Port E control registers (PECON0, PECON1)

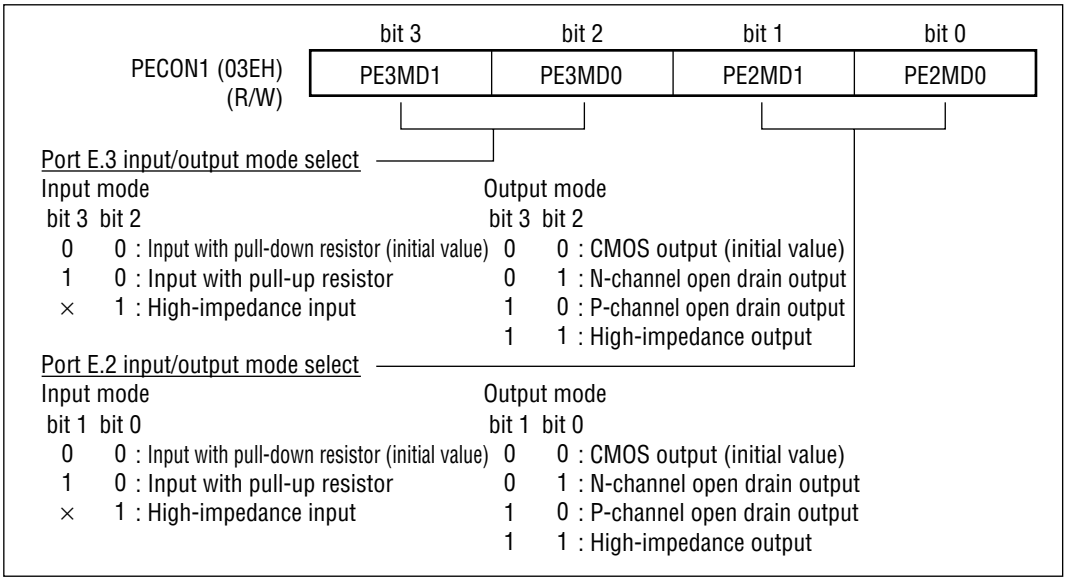
The port E control registers 0/1 (PECON0, PECON1) are 4-bit special function registers (SFRs) used to select port input/output mode.

The input mode can be pull-down resistor input, pull-up resistor input or high-impedance input.

The output mode can be CMOS output, N-channel open drain output, P-channel open drain output or high-impedance output.

At system reset all bits in PECON0 and PECON1 are set to "0", and port E is initialized to pull-down resistor input mode and CMOS output mode.





(4) Port E mode register (PEMOD)

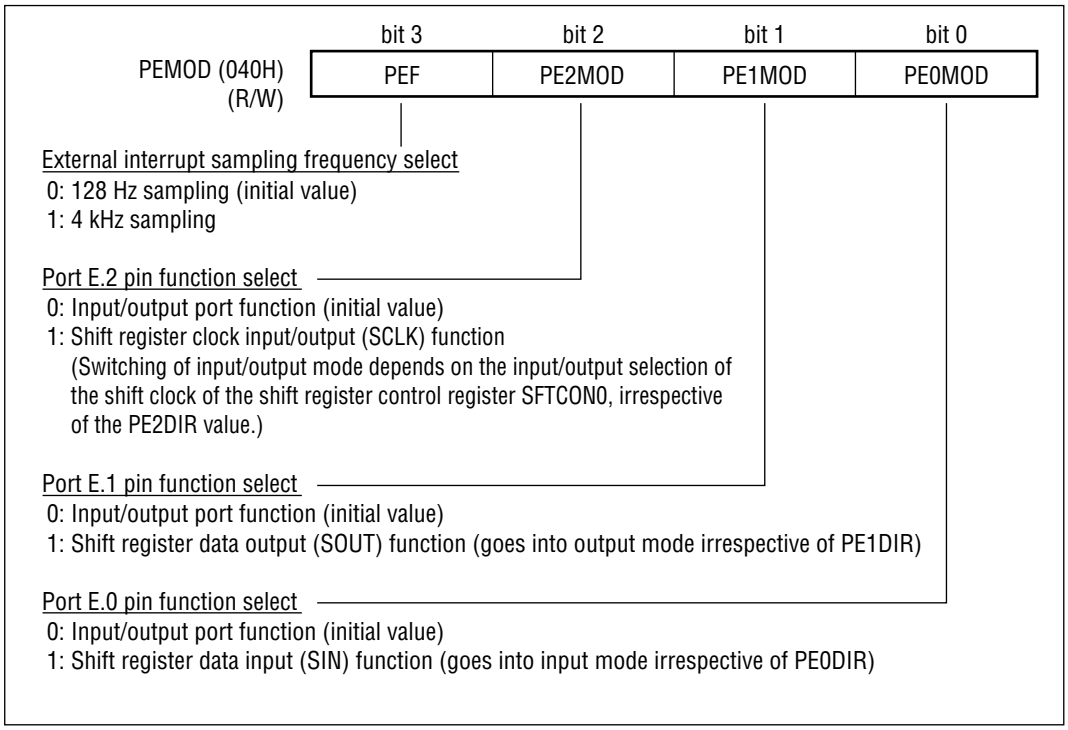
PEMOD is a 4-bit special function register (SFR) used to select the sampling frequency when PE.3 is used as an external interrupt. It is also used to select port E secondary functions other than external interrupt.

The external interrupt sampling frequency can be selected as either 128 Hz or 4 kHz.

Port E secondary functions are indicated in Table 12-4.

Table 12-4 Port E Secondary Functions

Port	Secondary function	Description
PE.0	SIN	Shift register data input
PE.1	SOUT	Shift register data output
PE.2	SCLK	Shift register clock I/O
PE.3	INT2	External interrupt 2



At system reset all bits in PEMOD are initialized to "0".

12.7.3 Port E.3 External Interrupt Function (External Interrupt 2)

Port E.3 has external interrupt 2 allocated as secondary function.

External interrupt generation for PE.3 is triggered by the falling edge of the 128 Hz or 4 kHz time base counter, which is the sampling clock.

After the port level changes, the interrupt request signal (XI2INT) is output, and the interrupt request flag (QXI2) is set. The maximum delay for this sequence is one cycle of the sampling clock (128 Hz or 4 kHz).

The interrupt start address for external interrupt 2 is 0018H.

Figure 12-16 shows the external interrupt 2 generation timing.

Figure 12-17 shows the equivalent circuit for external interrupt 2 control.

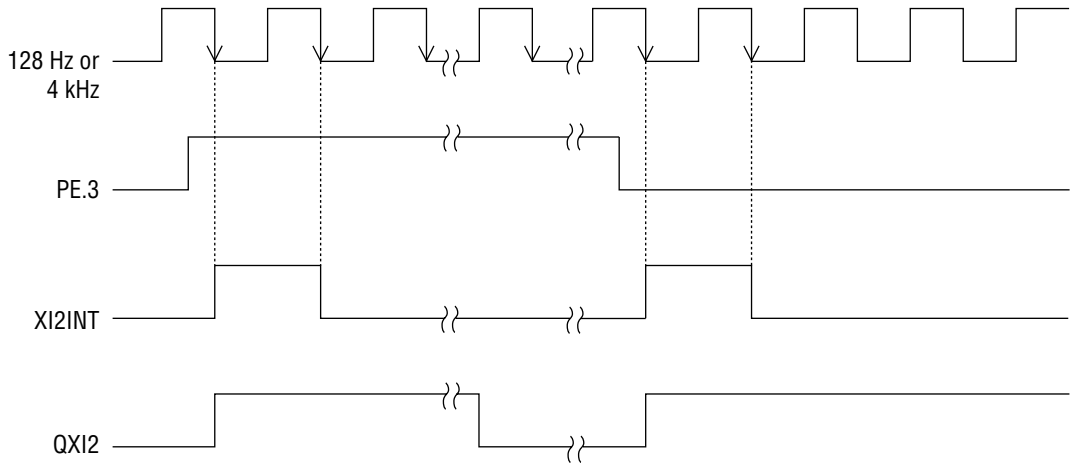


Figure 12-16 External Interrupt 2 Generation Timing

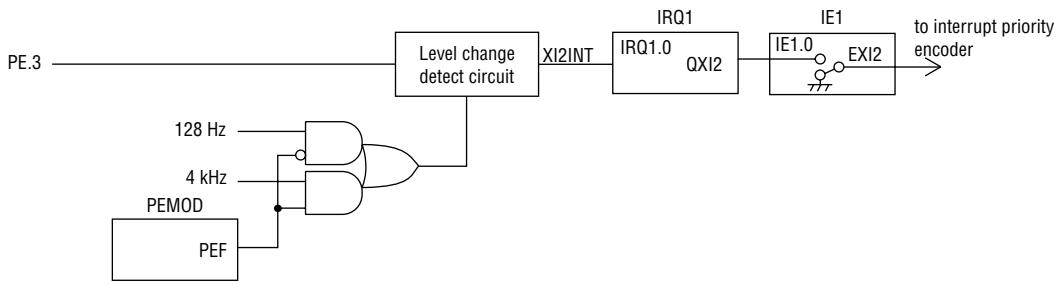


Figure 12-17 External Interrupt 2 Control Equivalent Circuit

Chapter 13

Melody Driver (MELODY)

Chapter 13 Melody Driver (MELODY)

13.1 Overview

The ML63187, ML63189B, and ML63193 have an internal melody circuit and buzzer circuit.

While automatically reading melody data in ROM (program memory) as specified by an MSA instruction, the melody circuit outputs a melody signal via the MD and MDB pins.

The melody circuit can select 29 different tones, 63 different tone lengths, and 15 different tempos.

The buzzer circuit has four different buzzer output modes at a frequency of 4 kHz. The buzzer driver signal is output via the MD and MDB pins.

Melody output is a higher priority operation than buzzer output.

13.2 Melody Driver Configuration

The melody driver configuration is shown in Figure 13-1.

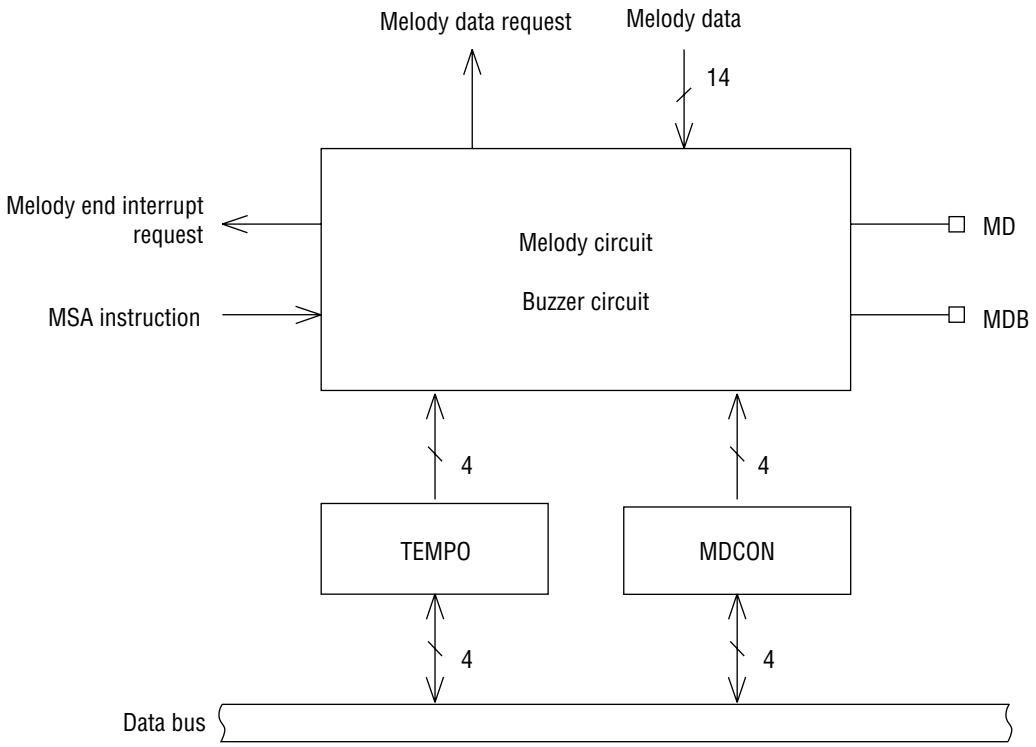
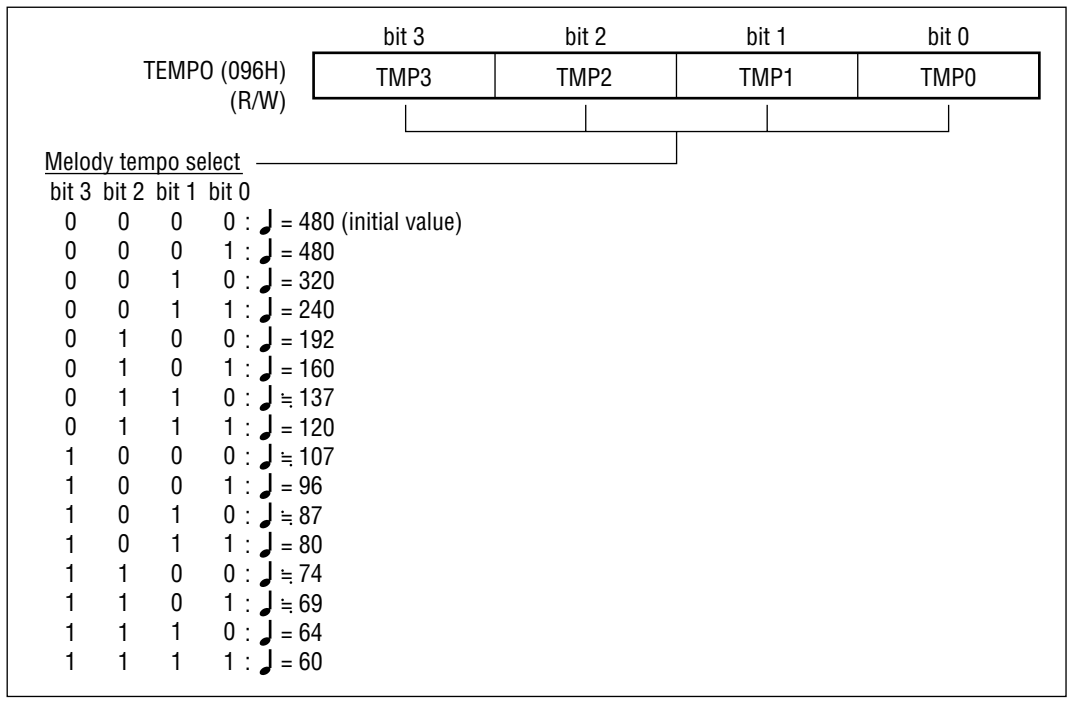


Figure 13-1 Melody Driver Configuration

13.3 Melody Driver Registers

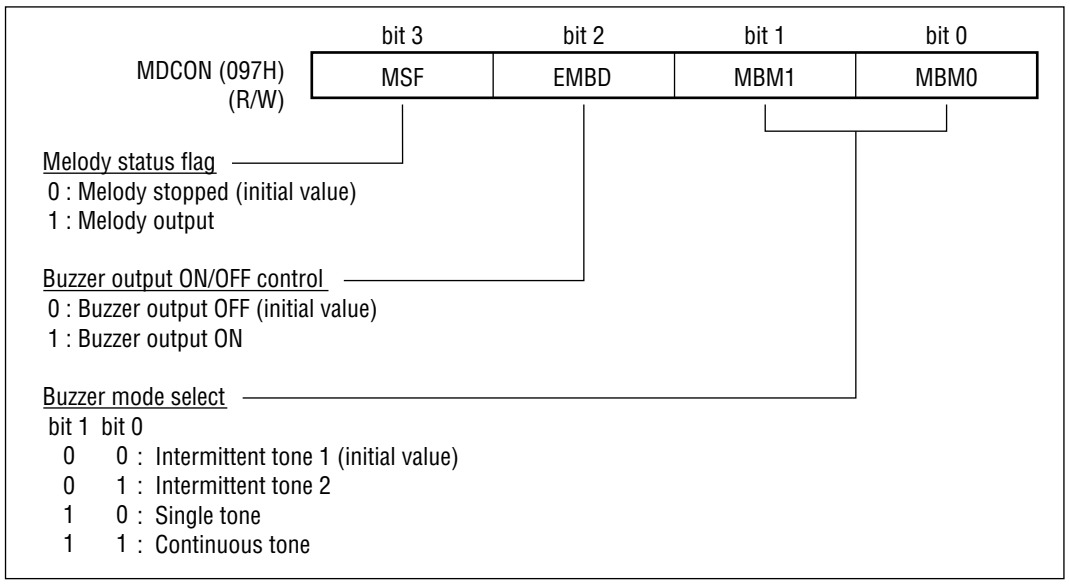
(1) Tempo Register (TEMPO)

TEMPO is a 4-bit special function register (SFR) that sets the tempo of the melody driver.



(2) Melody Driver Control Register (MDCON)

MDCON is a 4-bit special function register (SFR) that controls output of the melody driver.



bit 3: MSF

This flag indicates the melody output status.
When an MSA instruction starts the melody, MSF is set to "1". After output of the last melody data (END bit is "1"), MSF is cleared to "0".
Setting MSF to "0" during melody output will forcibly stop the melody output. If forcibly stopped, the melody output cannot be restarted at the address at which it was stopped.
At system reset, MSF is cleared to "0".

Note:

If MSF (bit 3 of MDCON) is set to "0" to stop melody output forcibly, it is required to set the stop address on the ROM table to the end-data address (8000H). In this case, set MSF to "0" after writing the melody end data that consists of two words of melody (silence with the END bit being "1") data. If this programming is not executed, melody output may not be stopped even if MSF is set to "0". Example programming is shown below.

```
;*Program part***********
    DI                          ; 0. Disable master interrupt (MIE).
    MSA  MDSTOP_DATA            ; 1. Write melody end data to the melody circuit.
    MOV  A,#0                   ; 2. Set the MSF to "0".
    MOV  MDCON,A                ;
    MOV  A,#1101b               ; 3. Clear melody end interrupt request (QMD).
    AND  IRQ0,A                 ;
    EI                          ; 4. Enable master interrupt (MIE).
;*ROM table data part****
;*Provide two words of melody data so that a melody will always be terminated even if a melody
;*request is issued twice.
MDSTOP_DATA:
    DW   8000H                  ; Silence data 1
    DW   8000H                  ; Silence data 2
;************************
```

The Development Support System (EASE63180 Emulator) differs from the IC in actual operation: In the EASE63180 Emulator, melody output will be stopped only by setting MSF to "0"; writing melody end data is not needed.

bit 2: EMBD

This bit turns the buzzer output ON or OFF.
At system reset, EMBD is cleared to "0" and buzzer output is turned OFF.
In the single tone output mode, setting EMBD to "1" turns ON the buzzer output. After the second falling edge of the 32 Hz output, EMBD is cleared to "0" and buzzer output is turned OFF.
If melody output is started during buzzer output, EMBD is cleared to "0" and the buzzer output is turned OFF.

bit 1, 0: MBM1, MBM0

These bits select the buzzer output mode.

Output of two types of intermittent tones, a single tone or a continuous tone can be selected.

At system reset, MBM1 and MBM0 are cleared to "0", selecting output of intermittent tone 1.

Buzzer output mode	Waveform
Intermittent tone 1	Intermittent tone waveform synchronized to 8 Hz output of time base counter
Intermittent tone 2	Intermittent tone waveform synchronized to the logical AND of 8 Hz signal output and a "L" level of 1 Hz signal output of the time base counter
Single tone	Single tone waveform beginning when EMBD is set to "1" until second falling edge of 32 Hz output of time base counter
Continuous tone	Continuous tone waveform that is constant while EMBD is "1"

Figure 13-2 shows the output waveforms of the melody driver output pins.

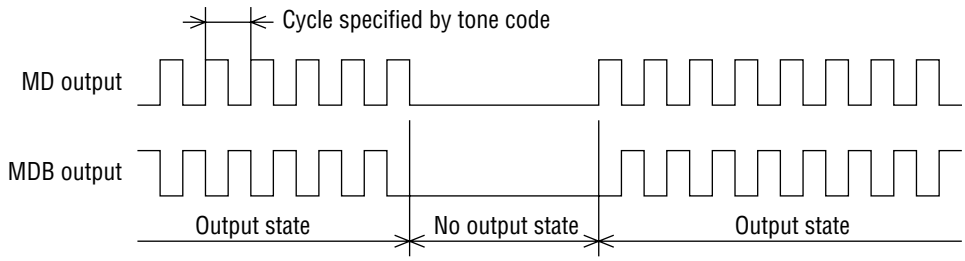


Figure 13-2 Output Waveforms of Melody Driver Output Pins

13.4 Melody Circuit Operation

After the melody tempo is set in the tempo register (TEMP), execution of an MSA instruction will start operation of the melody circuit.

The melody circuit outputs melody data while automatically reading melody data in ROM (program memory) as specified by an MSA instruction. When the last melody data is read (END bit is "1"), the melody circuit generates a melody end interrupt request. At this time, if an MSA instruction is executed, after the last melody data is output, melody output will continue from the melody data specified by the MSA instruction. If an MSA instruction is not executed, the melody output will stop after the last melody data is output.

MSF (bit 3 of MDCON) is a flag indicating the melody output status. When MSF is "1", the melody is being output, and when "0", the melody is stopped. Setting MSF to "0" during melody output will forcibly stop the melody output. If it is required to stop melody output forcibly, describe the program according to the "Note" on page 13-3. If forcibly stopped, the melody output cannot be restarted at the address at which it was stopped.

13.4.1 Tempo Data

Tempo data defines the basic tone length. Tempo data is set in the tempo register (TEMPO). The tempos (number of counts per minute) set by TEMPO are shown in Table 13-1.

Table 13-1 Melody Tempo

TEMPO					Tempo
TP3–0	TP3	TP2	TP1	TP0	
0H	0	0	0	0	♩ = 480
1H	0	0	0	1	♩ = 480
2H	0	0	1	0	♩ = 320
3H	0	0	1	1	♩ = 240
4H	0	1	0	0	♩ = 192
5H	0	1	0	1	♩ = 160
6H	0	1	1	0	♩ ≒ 137
7H	0	1	1	1	♩ = 120
8H	1	0	0	0	♩ ≒ 107
9H	1	0	0	1	♩ = 96
AH	1	0	1	0	♩ ≒ 87
BH	1	0	1	1	♩ = 80
CH	1	1	0	0	♩ ≒ 74
DH	1	1	0	1	♩ ≒ 69
EH	1	1	1	0	♩ = 64
FH	1	1	1	1	♩ = 60

13.4.2 Melody Data

Melody data is 14-bit format data in the program ROM defining tone, tone length and end tone. The melody data format is indicated in Figure 13-3.

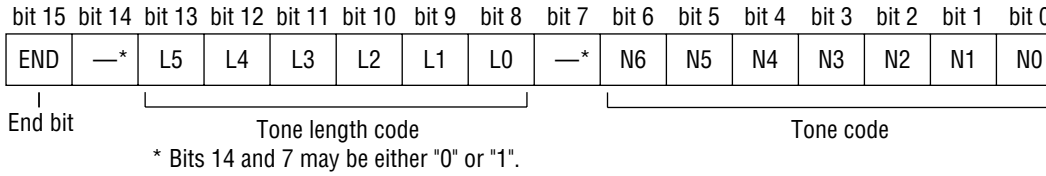


Figure 13-3 Melody Data Format

(1) Tone code

The tone code is set in bits 6 through 0 of the melody data. The frequencies that can be output by the melody circuit are defined as:

$$\frac{65536}{(N + 2)} \text{ Hz} \quad \text{(where N is an integer from 4 to 127)}$$

The relation between N and tone code bits is:

$N = 2^6N6 + 2^5N5 + 2^4N4 + 2^3N3 + 2^2N2 + 2^1N1 + 2^0N0$

If N6 through N2 are all set to "0", there is no melody output for the time specified by the tone length code. Values for N1 and N0 are irrelevant.

Table 13-2 indicates the relations between tones and tone codes.

Table 13-2 Tone and Tone Code Correspondence

Tone	Frequency (Hz)	Tone code							
		N6	N5	N4	N3	N2	N1	N0	N6–N0
C^1	529	1	1	1	1	0	1	1	7BH
Cis^1	560	1	1	1	0	0	1	1	73H
D^1	590	1	1	0	1	1	0	1	6DH
Dis^1	624	1	1	0	0	1	1	1	67H
E^1	662	1	1	0	0	0	0	1	61H
F^1	705	1	0	1	1	0	1	1	5BH
Fis^1	745	1	0	1	0	1	1	0	56H
G^1	790	1	0	1	0	0	0	1	51H
Gis^1	840	1	0	0	1	1	0	0	4CH
A^1	886	1	0	0	1	0	0	0	48H
Ais^1	936	1	0	0	0	1	0	0	44H
B^1	993	1	0	0	0	0	0	0	40H
C^2	1057	0	1	1	1	1	0	0	3CH
Cis^2	1111	0	1	1	1	0	0	1	39H
D^2	1192	0	1	1	0	1	0	1	35H

Table 13-2 Tone and Tone Code Correspondence (continued)

Tone	Frequency (Hz)	Tone code							
		N6	N5	N4	N3	N2	N1	N0	N6–N0
Dis^2	1260	0	1	1	0	0	1	0	32H
E^2	1338	0	1	0	1	1	1	1	2FH
F^2	1394	0	1	0	1	1	0	1	2DH
Fis^2	1490	0	1	0	1	0	1	0	2AH
G^2	1560	0	1	0	1	0	0	0	28H
Gis^2	1680	0	1	0	0	1	0	1	25H
A^2	1771	0	1	0	0	0	1	1	23H
Ais^2	1872	0	1	0	0	0	0	1	21H
B^2	1986	0	0	1	1	1	1	1	1FH
C^3	2114	0	0	1	1	1	0	1	1DH
D^3	2341	0	0	1	1	0	1	0	1AH
Dis^3	2521	0	0	1	1	0	0	0	18H
E^3	2621	0	0	1	0	1	1	1	17H
Fis^3	2979	0	0	1	0	1	0	0	14H

(2) Tone length code

The tone length code is set in melody data bits 13 through 8.

Table 13-3 indicates the relation between tone length and tone length code (L5 to L0).

The tone length that is set during execution of the MSA instruction is shorter by approximately 1 to 3 ms.

When all bits are set to "0", the tone length will be the same as the minimum tone length (the tone length with only L0 set to "1").

Table 13-3 Tone Length and Tone Length Code Correspondence

Tone length	Tone length code						
	L5	L4	L3	L2	L1	L0	L5–L0
	1	1	1	1	1	1	3FH
	1	0	1	1	1	1	2FH
	0	1	1	1	1	1	1FH
	0	1	0	1	1	1	17H
	0	0	1	1	1	1	0FH
	0	0	1	0	1	1	0BH
	0	0	0	1	1	1	07H
	0	0	0	1	0	1	05H
	0	0	0	0	1	1	03H
	0	0	0	0	1	0	02H
	0	0	0	0	0	1	01H

Tone lengths specified by the tone length code and the tempo data are expressed by the following:

$1.953125 \times (TP + 1) \times (L + 1)$ ms (where TP is an integer from 1 to 15, and L is an integer from 1 to 63)

TP is a value set in the tempo register (TEMPO), and has the following bit correspondence:

$$TP = 2^3TP3 + 2^2TP2 + 2^1TP1 + 2^0TP0$$

L is set by the tone length code, and has a bit correspondence with the tone length code as:

$$L = 2^5L5 + 2^4L4 + 2^3L3 + 2^2L2 + 2^1L1 + 2^0L0$$

(3) END bit

The END bit is set in bit 15 of the melody data. When the output of the last melody data is started (END bit is "1"), the melody circuit generates a melody end interrupt request, and stops the melody after the last melody data is output.

13.4.3 Melody Circuit Application Example

An example melody is shown in Figure 13-4.

Table 13-4 lists the note codes for the melody shown in Figure 13-4.

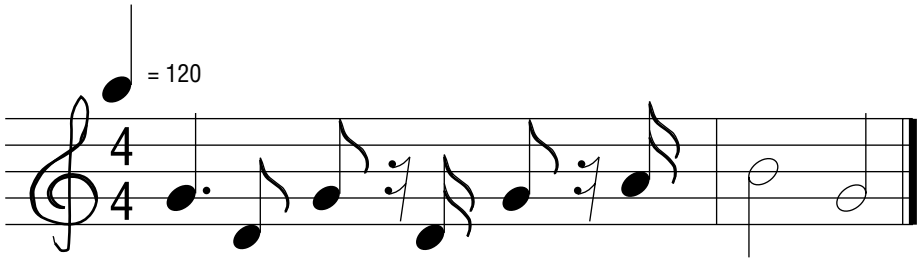


Figure 13-4 Example Melody

Table 13-4 Note Code Table

Note	Note code																Hex
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	END	—*	L5	L4	L3	L2	L1	L0	—*	N6	N5	N4	N3	N2	N1	N0	
G^2	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	2F28H
D^2	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	1	0F35H
G^2	0	0	0	0	1	1	1	1	0	0	1	0	1	0	0	0	0F28H
—	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0700H
D^2	0	0	0	0	0	1	1	1	0	0	1	1	0	1	0	1	0735H
G^2	0	0	0	0	1	1	1	1	0	0	1	0	1	0	0	0	0F28H
—	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1	0700H
A^2	0	0	0	0	0	1	1	1	0	0	1	0	0	0	1	1	0723H
B^2	0	0	1	1	1	1	1	1	0	0	0	1	1	1	1	1	3F1FH
G^2	1	0	1	1	1	1	1	1	0	0	1	0	1	0	0	0	BF28H

* Bits 14 and 7 may be "0" or "1", but in this example they are shown as "0".

13.5 Buzzer Circuit Operation

When EMBD (bit 2 of MDCON) is set to "1", a buzzer driver signal is sent to the melody driver output pins (MD, MDB).

Four buzzer output modes can be selected by MBM1 (bit 1 of MDCON) and MBM0 (bit 0 of MDCON): two types of intermittent tones, a single tone, or a continuous tone output. The buzzer output frequency is 4 kHz and has a 50% duty ratio.

In the intermittent tone 1 mode, a waveform synchronized to the 8 Hz output of the time base counter is output.

In the intermittent tone 2 mode, a waveform synchronized to the logical AND of 8 Hz signal output and a "L" level of 1 Hz signal of the time base counter is output.

In the single tone mode, output starts in synchronization with the rising edge of EMBD. At the second falling edge of the 32 Hz output of the time base counter, EMBD is cleared to "0" and output is stopped.

In the continuous tone mode, output is continued while EMBD is "1".

While the melody is being output (MSF (bit 3 of MDCON) = "1"), the buzzer output is turned OFF. If melody output is started during buzzer output, EMBD is cleared to "0", the buzzer output is stopped, and melody output is given priority.

Figure 13-5 shows the output waveforms of each mode. Shaded sections indicate the 4 kHz output frequency.

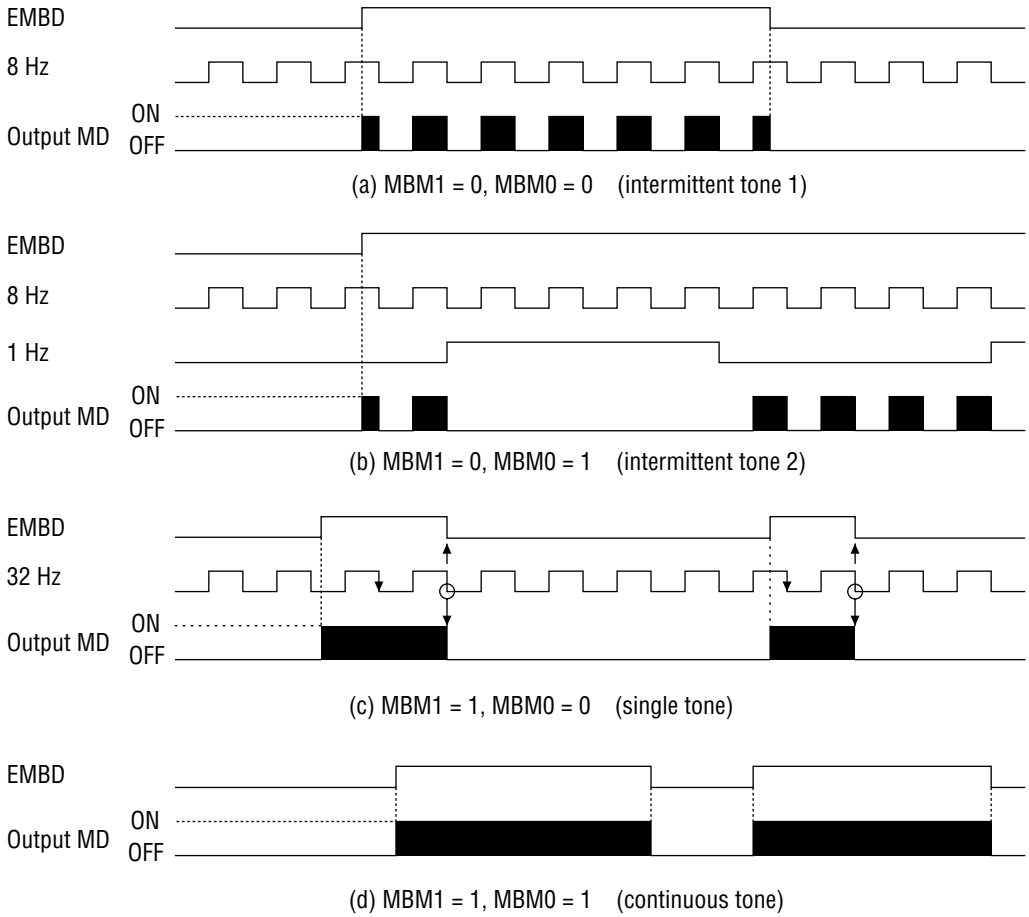


Figure 13-5 Buzzer Driver Output Waveforms in Each Output Mode

Chapter 14

Serial Port (SIO)

Chapter 14 Serial Port (SIO)

14.1 Overview

The ML63193 has a built-in serial communication port (serial port) for either synchronous or asynchronous communication.

The serial port implements the send and receive circuits in independent circuits, making it possible to send and receive simultaneously.

The send and receive modes can be UART mode (asynchronous communication mode) or synchronous mode (synchronous communication mode).

In synchronous mode an internal clock mode generates the shift clock internally, and an external clock mode receives an external shift clock.

Table 14-1 shows the serial port modes.

Table 14-1 Serial Port Modes

		Mode		Baud rate
Serial port	Send side	UART mode		Can be set to a user-specified value with timers 2, 3 (TM2, 3)
		Synchronous mode	Internal clock mode	32.768 kHz
			External clock mode	From external clock
	Receive side	UART mode		• 9600 bps • 4800 bps • 2800 bps • 1200 bps
		Synchronous mode	Internal clock mode	32.768 kHz
			External clock mode	From external clock

14.2 Serial Port Configuration

Figure 14-1 indicates the serial port configuration.

The serial port consists of the send/receive clock generator circuits, the send/receive control registers, the buffer registers to store send/receive data, send/receive data transfer shift registers, and the send/receive status registers.

PC.0/RXD is the send serial data input pin, PC.3/TXD is the send serial data output pin, PC.1/TXC is the serial send clock I/O pin, and PC.2/RXC is the serial receive clock I/O pin. Set I/O and secondary functions with the port control registers as needed for each communication mode.

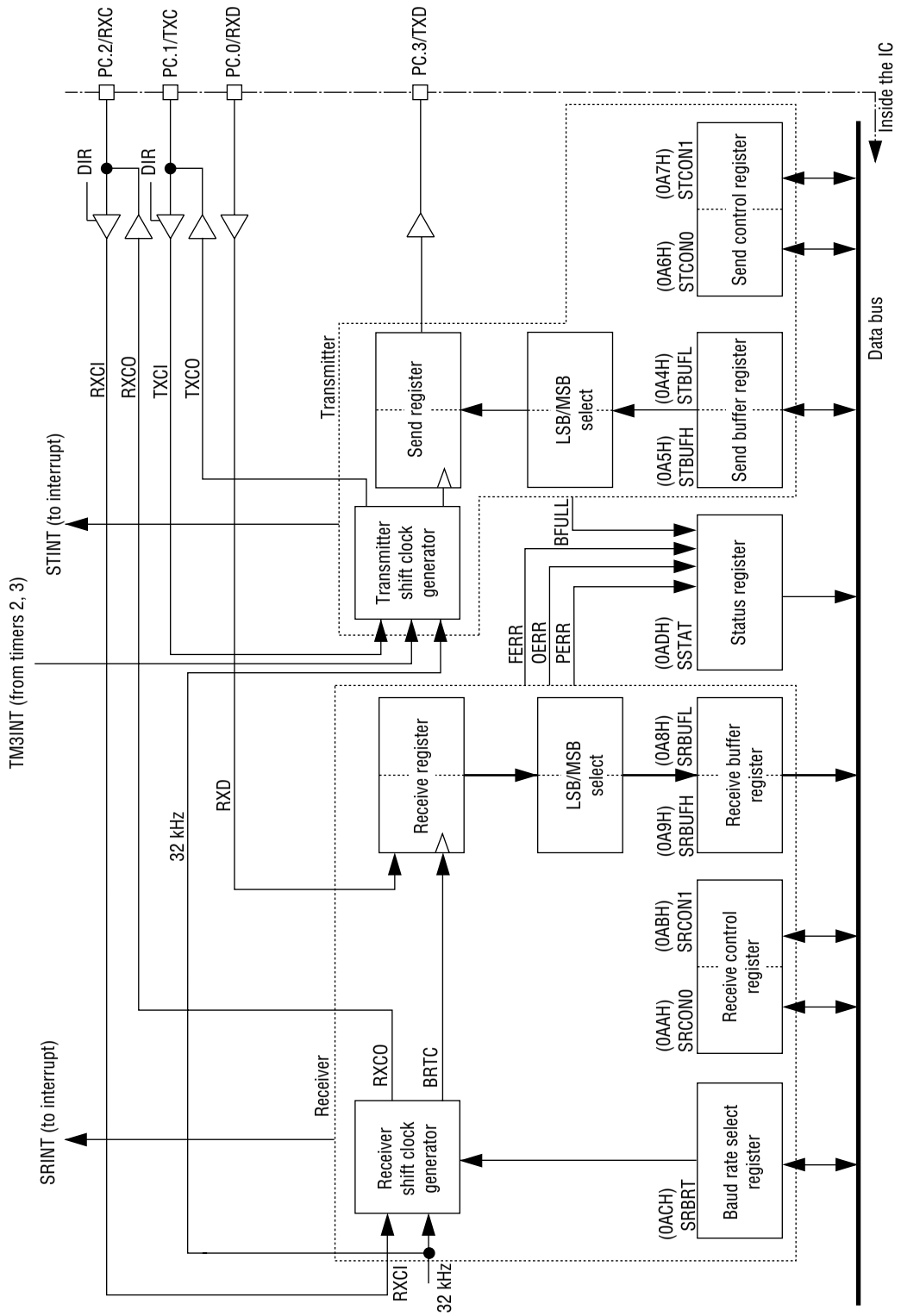
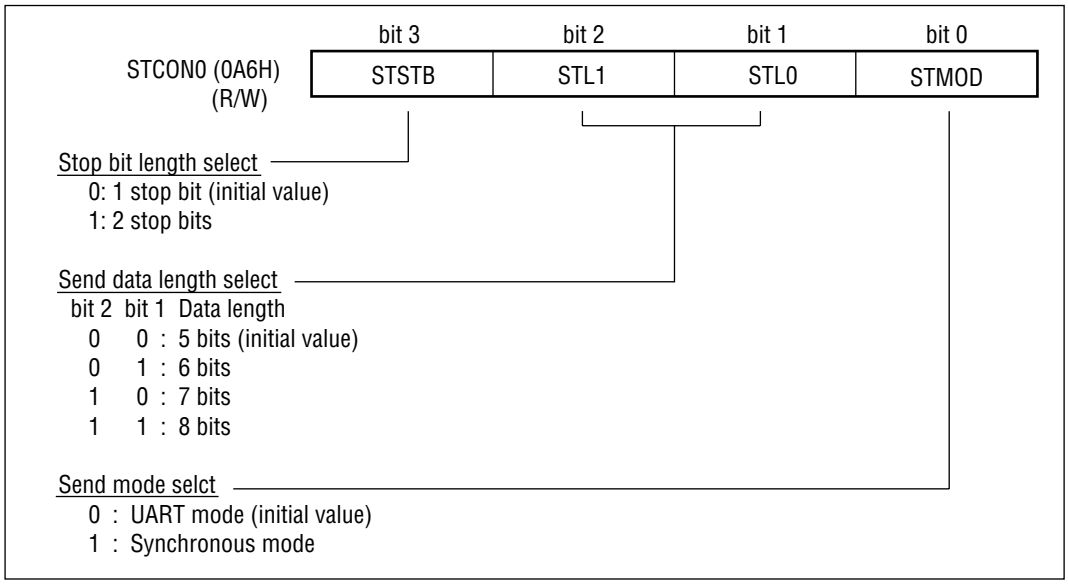


Figure 14-1 Serial Port Configuration

14.3 Serial Port Registers

(1) Send control registers 0/1 (STCON0, STCON1)

STCON0 and STCON1 are 4-bit special function registers (SFRs) to control the serial port send operation. STCON0 and STCON1 are initialized to "0" at system reset.



bit 3: STSTB (Serial Transmission STop Bit)

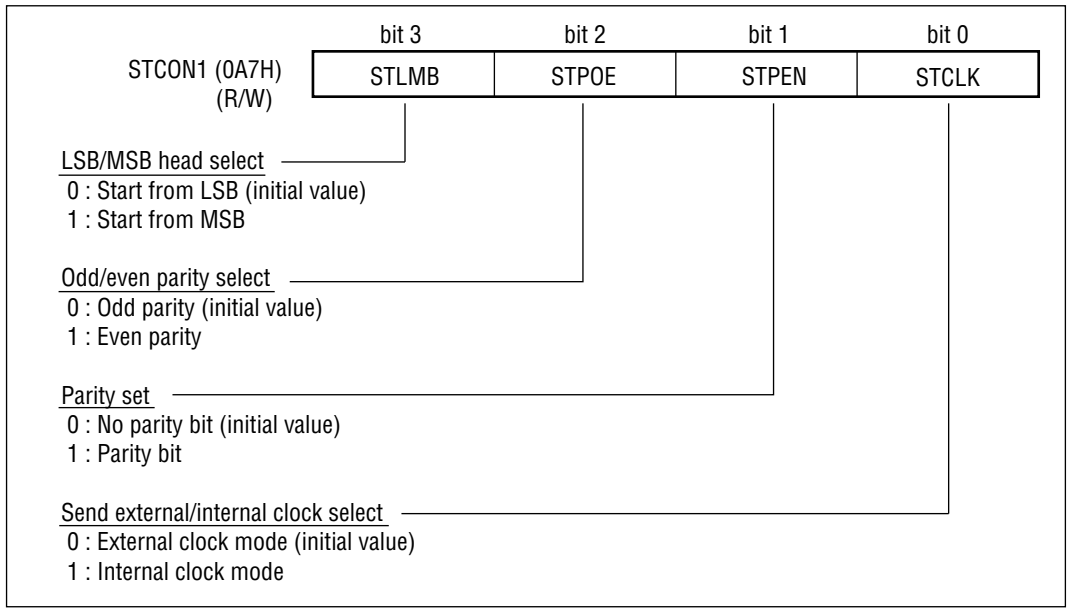
This bit specifies stop bit length. Valid only when bit 0 is "0" (UART mode).

bit 2, 1: STL1 (Serial Transmission Length select bit 1),
STL0 (Serial Transmission Length select bit 0)

These bits specify the send data length.

bit 0: STMOD (Serial Transmission MODe bit)

This bit specifies the serial port send operation mode.



bit 3: STLMB (Serial Transmission Least significant bit first or Most significant Bit first)

This bit specifies either LSB first or MSB first for send data.

bit 2: STPOE (Serial Transmission Parity Odd or Even number bit)

This bit specifies whether the parity bit is even or odd. Valid only when bit 1 is "1" (parity bit).

bit 1: STPEN (Serial Transmission Parity ENable bit)

This bit specifies whether or not a parity bit is added.

bit 0: STCLK (Serial Transmission CLock select bit)

This bit specifies the external/internal send clock for synchronous mode. Valid only when STMOD (bit 0 of STCON0) is "1" (synchronous mode).

(2) Send buffer registers (STBUFL, STBUFH)

	bit 3	bit 2	bit 1	bit 0
STBUFL (0A4H) (R/W)	TB3	TB2	TB1	TB0
STBUFH (0A5H) (R/W)	TB7	TB6	TB5	TB4

STBUFL and STBUFH are 4-bit special function registers (SFRs) that set send data for serial port send operation.

LSB/MSB selection (described later) allows the data send direction (LSB or MSB first) to be specified. Both STBUFL and STBUFH are initialized to "0" at system reset.

Send operation begins when send data is set to STBUFH. Be sure to set send data to STBUFL before setting data to STBUFH.

Also set the baud rate and send mode before beginning send operation.

If send operation is already under way when send data is set to STBUFH, send for the new data begins when the prior send has ended, and at the same time an interrupt request signal (STINT) is generated. In the STINT interrupt routine the program should first write the send data to STBUFL and STBUFH to assure no pauses in the send sequence.

(3) Send register

The send register is a shift register that handles the shift operation in send. At system reset it is cleared to 00H. The send register cannot be directly accessed from the CPU.

The hardware send flow is indicated in Figure 14-2, to explain the timing for transfer of data from STBUFL/H to the send register.

First set the send mode and baud rate. When send data is set to STBUFH, the status (SSTAT) buffer full flag (BFULL) is set to "1", and unless send operation is already under way the content of STBUFL/H is transferred to the send register and send operation begins. When send operation begins the BFULL flag is reset to "0", and the next send data can be set to STBUFL/H.

If prior data send operation is not complete, the send data is held in STBUFL/H until send is completed. In this case BFULL remains set to "1". When the prior send operation is complete the send data will be transferred from STBUFL/H to the send register, and send begins.


Note:

When BFULL is "1" it is possible to set data to STBUFL/H, but prior data set to STBUFL/H that is being held there is overwritten and lost. Always set data after verifying that the BFULL flag is "0".

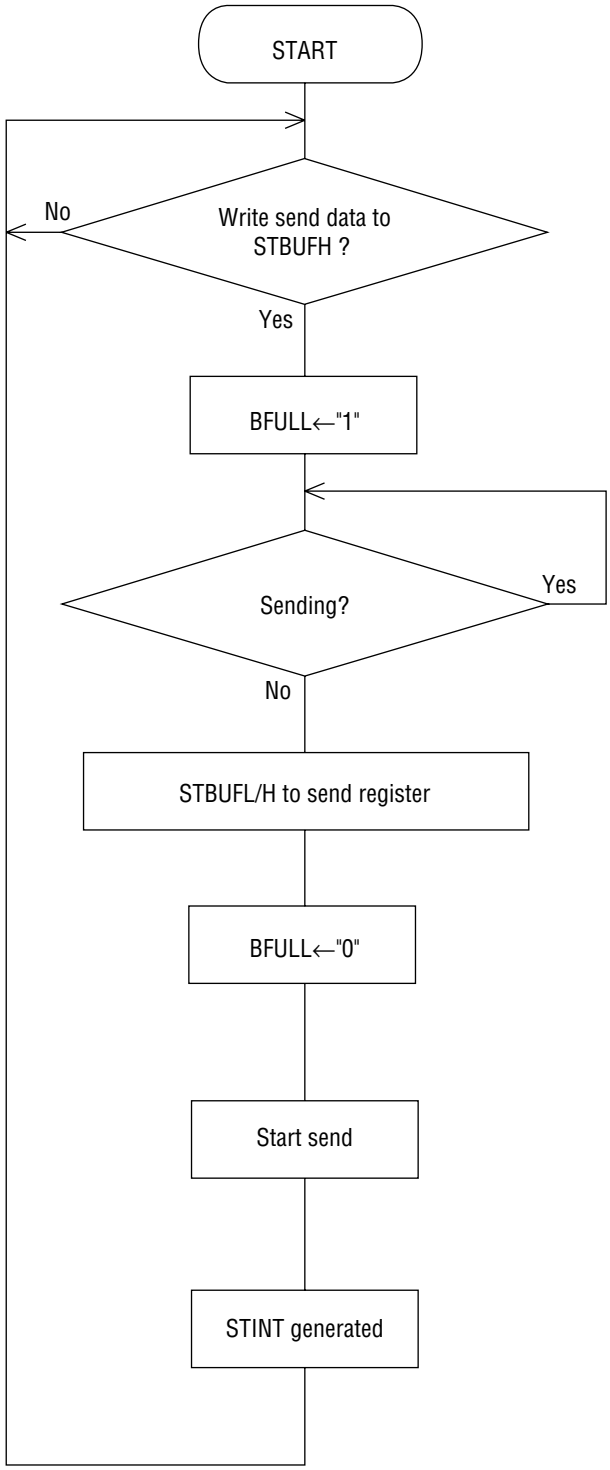
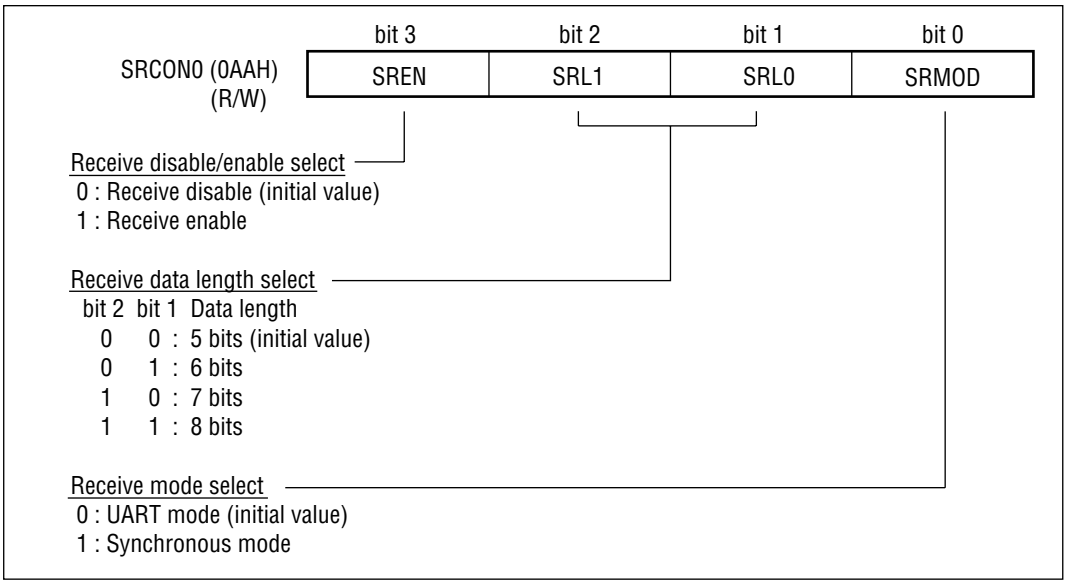


Figure 14-2 Hardware Send Operation Flow

(4) Receive control registers 0/1 (SRCON0, SRCON1)

SRCON0 and SRCON1 are 4-bit special function registers (SFRs) controlling serial port receive operation.

SRCON0 and SRCON1 are initialized to "0" at system reset.



bit 3: SREN (Serial Reception ENable bit)

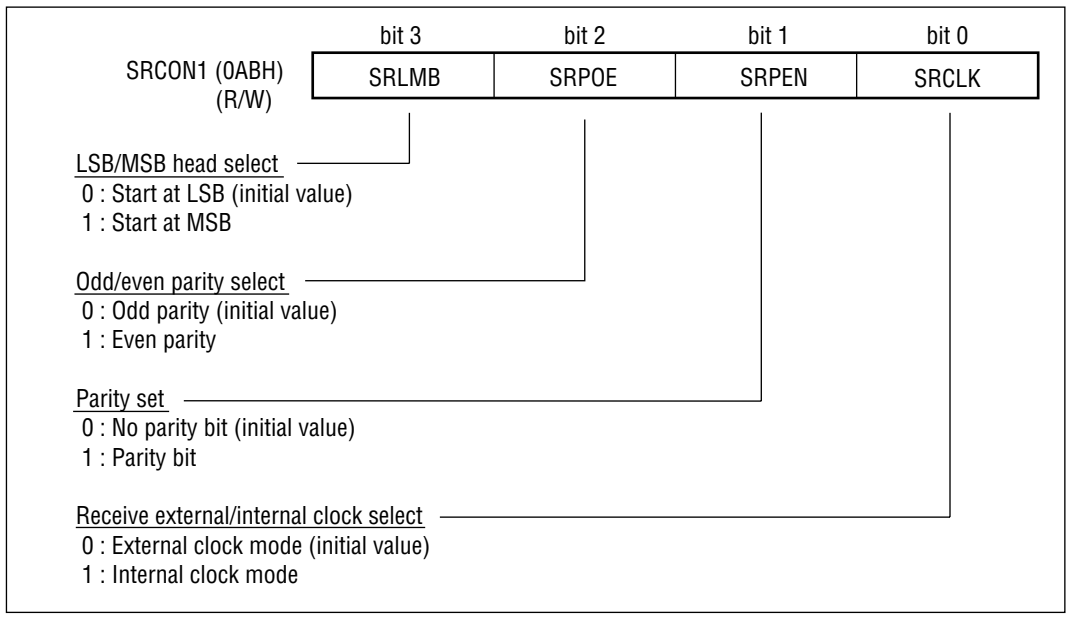
This bit specifies receive operation disable/enable. After receive is enabled in the synchronous mode, this bit is reset to "0" after receiving one frame of data. In the UART mode it does not change.

bit 2, 1: SRL1 (Serial Reception Length select bit 1),
SRL0 (Serial Reception Length select bit 0)

These bits specify the receive data length.

bit 0: SRMOD (Serial Reception MODe bit)

This bit specifies the serial port receive operation mode.



bit 3: SRLMB (Serial Reception Least significant bit first or Most significant Bit first)

This bit specifies either LSB first or MSB first for receive data.

bit 2: SRPOE (Serial Reception Parity Odd or Even number bit)

This bit specifies whether the parity bit is even or odd. Valid only when bit 1 is "1" (parity bit).

bit 1: SRPEN (Serial Reception Parity ENable bit)

This bit specifies whether or not a parity bit is added.

bit 0: SRCLK (Serial Reception CLocK select bit)

This bit specifies the external/internal receive clock for synchronous mode. Valid only when SRMOD (bit 0 of SRCON0) is "1" (synchronous mode).

(5) Receive register

The receive register is the shift register that handles shift operation at receive. It is initialized to 00H at system reset. It cannot be directly accessed by the CPU. When a receive operation is complete, the data read into the receive register is transferred to SRBUFL/H, and at the same time the receive interrupt request signal (SRINT) is generated.

(6) Receive buffer registers (SRBUFL, SRBUFH)

	bit 3	bit 2	bit 1	bit 0
SRBUFL (0A8H) (R)	RB3	RB2	RB1	RB0
	bit 3	bit 2	bit 1	bit 0
SRBUFH (0A9H) (R)	RB7	RB6	RB5	RB4

SRBUFL and SRBUFH are 4-bit special function registers (SFRs) used to hold the received data in serial port reception. SRBUFL and SRBUFH are initialized to "0" at system reset.

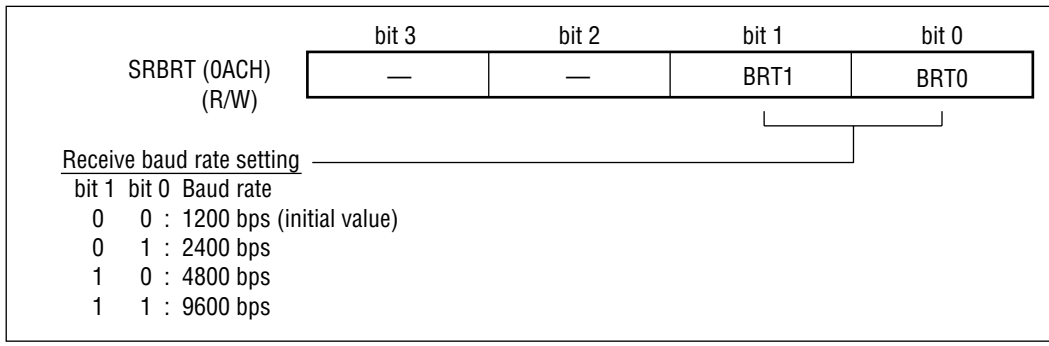
When receive operation is completed the contents of the receive register are sent to SRBUFL/H, and the receive interrupt request (SRINT) is generated. The contents of SRBUFL/H are held until the next receive operation is completed.

If data from a prior receive operation is in SRBUFL/H and new data is received, an overrun error will result. When an overrun error is generated, new received data cannot be loaded into SRBUFL/H.

(7) Receive baud rate setting register (SRBRT)

SRBRT is a 4-bit special function register (SFR) used to set the receive baud rate for serial port receive operation in UART mode.

SRBRT is initialized to 0CH at system reset.



bit 1, 0: BRT1 (Baud RaTe select bit1), BRT0 (Baud RaTe select bit 0)

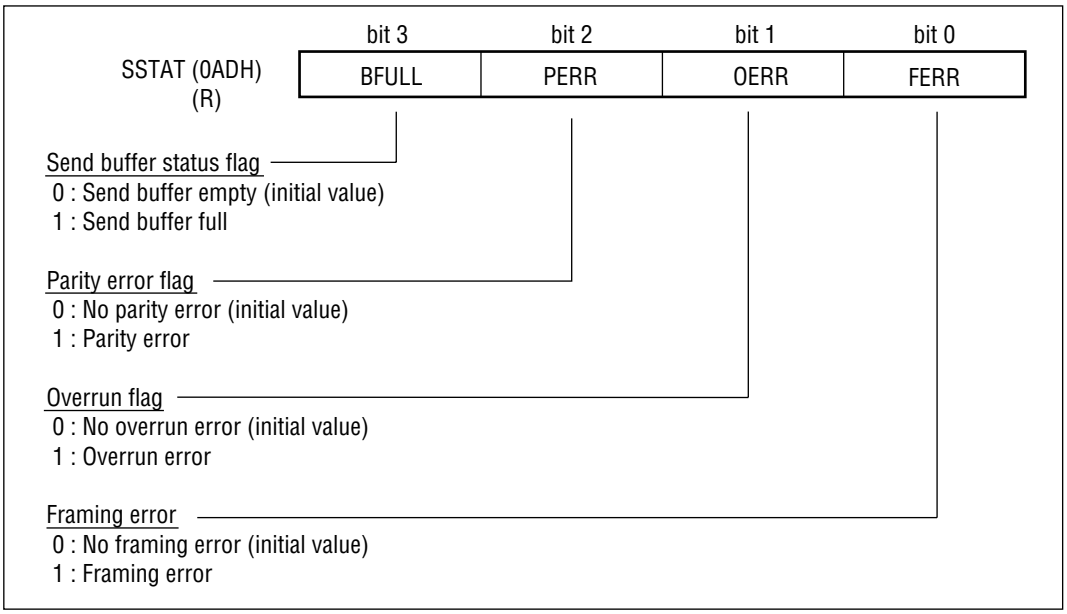
These bits set the receive baud rate.

(8) Serial status register (SSTAT)

SSTAT is a 4-bit special function register (SFR) used to indicate the status of serial port send/receive.

SSTAT is initialized to "0" at system reset.

SSTAT is a read-only register, and the content is reset every time it is read.



bit 3: BFULL (send Buffer FULL flag)

This bit is enabled in both UART and synchronous modes, and is set to "1" when send data is set to STBUFL/H in the send mode, and reset to "0" when the send data is transferred to the send register.

When BFULL is set to "1" and send data is set (written) to STBUFL/H, the previous data set to those registers is overwritten and lost. Always set data only after verifying that the BFULL flag is "0".

bit 2: PERR (Parity ERRor flag)

This bit is enabled in both UART and synchronous modes, and is set to "1" when the parity for the received data does not match the parity bit attached to the data.

bit 1: OERR (Overrun ERRor flag)

This bit is enabled in both UART and synchronous modes, and is set to "1" when data reception is completed and the data received the previous time has still not been transferred to the CPU. In this case, the new data cannot be transferred to SRBUFL/H.

bit 0: FERR (Framing ERRor flag)

This is only enabled in the UART mode and is set to "1" in the following instances.

(1) when a "1" is detected in start bit sampling

(2) when a "0" is detected in stop bit sampling

In either case a receive interrupt request signal (SRINT) is generated.

14.4 Serial Port Operation Description

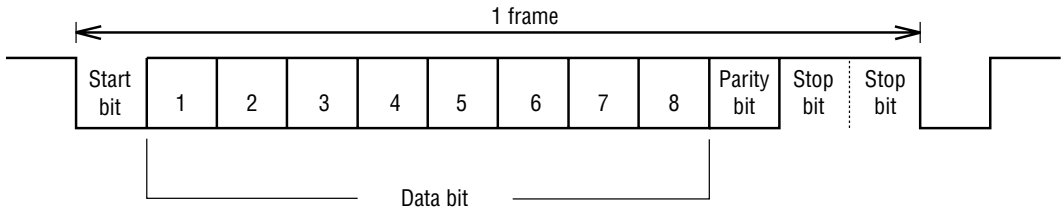
14.4.1 Data Format

(1) UART mode

The data format for the UART mode is shown in Figure 14-3.

SRCON0/1 and STCON0/1 can be set to specify a data bit length of 5 to 8 bits. The parity bit can be enabled/disabled. If enabled it can be set to even or odd. Stop bit length can be set to 1 or 2 bits.

The combination of these parameters gives a range of from 7 to 12 bits for send/receive data frames.



- 1 frame
  - MAX ····· 12 bits
  - MIN ····· 7 bits
- Data bit length: 5 to 8 bits, variable
- Parity bit: enable/disable
  Odd/even select
- Stop bits: 1 or 2 stop bits select

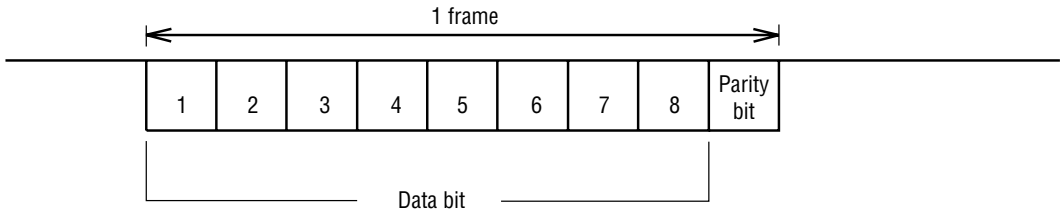
Figure 14-3 UART Mode Data Format

(2) Synchronous mode

The data format for the UART mode is shown in Figure 14-4.

SRCON0/1 and STCON0/1 can be set to specify a data bit length of 5 to 8 bits. The parity bit can be enabled/disabled, and if enabled can be set to even or odd.

The combination of these parameters gives a range of from 5 to 9 bits for send/receive data frames.



- 1 frame
  - MAX ····· 9 bits
  - MIN ····· 5 bits
- Data bit length: 5 to 8 bits, variable
- Parity bit: enable/disable
  Odd/even select

Figure 14-4 Synchronous Mode Data Format

14.4.2 Send Operation Description

The serial port send circuit has a two-stage configuration. This consists of the send register and the send buffer register (STBUFL/H), so it is possible to set send data to STBUFL/H while sending the previous data. When the serial status flag is (SSTAT) BFULL flag is 1, however, it indicates that STBUFL/H send data has not yet been transferred to the send register. Always verify that the BFULL flag is 0 before transferring data.

(1) UART mode

The UART mode is specified by setting STMOD (bit 0 of STCON0) to "0". Figure 14-5 is the UART mode send timing chart. The UART mode send procedure is described below. The send baud rate is set first, then the timer, and then the send format (data bit length, parity bit, etc.) in STCON0, STCON1. The TM3INT signal supplied from timer 2, 3 is the baud rate clock.

Ⓐ Set send data to STBUFL/H.

Ⓑ The send data is transferred from STBUFL/H to the send register, and send operation begins. At the same time the serial port send interrupt request (STINT) is generated.

Ⓒ Verify that BFULL = "0", then set the next send data to STBUFL/H.

Ⓓ When send operation is complete, the send data set to STBUFL/H is transferred to the send register, and send operation begins. At the same time the serial port send interrupt request (STINT) is generated.

Repeat operation Ⓒ the required number of times.

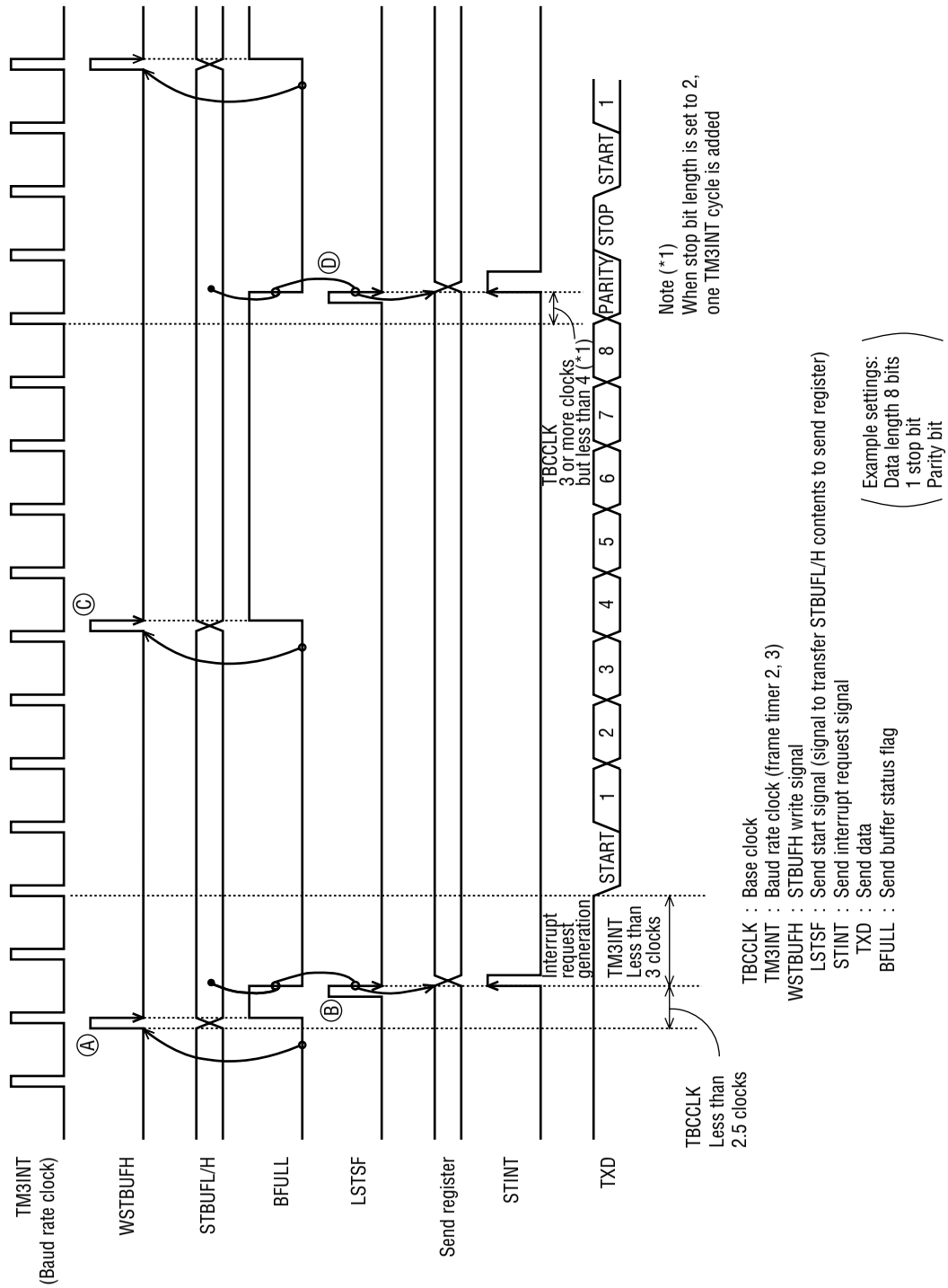


Figure 14-5 UART Mode Send Timing Chart

(2) Synchronous internal clock mode

The synchronous internal clock mode is selected by setting STMOD (bit 0 of STCON0) to "1", and STCLK (bit 0 of STCON1) to "1".

Figure 14-6 is the send timing chart for the synchronous internal clock mode.

The synchronous internal clock send procedure is described below.

First the send format (data bit length, parity bit, etc.) is set to STCON0 and STCON1.

Ⓐ Set send data to STBUFL/H.

Ⓑ The send data is transferred from STBUFL/H to the send register, and send operation begins. At the same time the interrupt request signal (STINT) is generated.

Ⓒ Check that BFULL = "0", then set the next send data to STBUFL/H.

Ⓓ When the send operation is complete, the send data set to STBUFL/H is transferred to the send register, and the send operation begins. At the same time, the serial port send interrupt signal (STINT) is generated.

Repeat step Ⓒ the required number of times.

In the synchronous internal clock mode the send baud rate is fixed at the crystal oscillation frequency, that is, the frequency (32.768 kHz) of the time base clock (TBCCLK).

After data is set to STBUFH, the send clock (TXCO) generates between 2 and 3.5 clocks of the TBCCLK source, and a send operation starts.

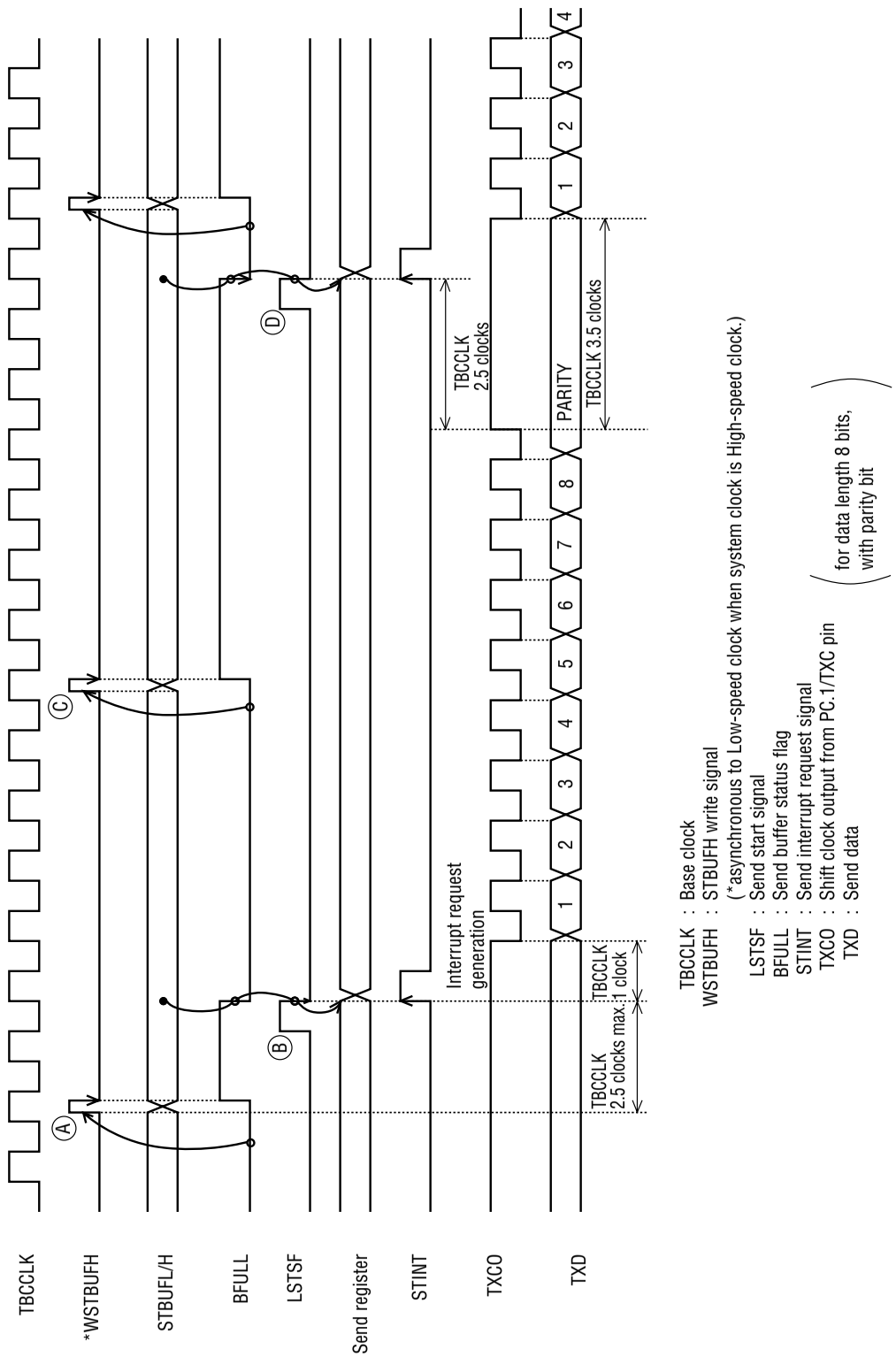


Figure 14-6 Send Timing Chart for Synchronous Internal Clock Mode

(3) Synchronous external clock mode

The synchronous external clock mode is selected by setting STMOD (bit 0 of STCON0) to "1", and STCLK (bit 0 of STCON1) to "0".

Figure 14-7 is the send timing chart for the synchronous external clock mode.

The synchronous external clock send procedure is described below.

First set the send format (data bit length, parity bit, etc.) to STCON0 and STCON1.

Ⓐ Set send data to STBUFL/H.

Ⓑ The send data is transferred from STBUFL/H to the send register, and at the same time the interrupt request signal (STINT) is generated.

Ⓒ Send operation is started by the send shift clock (TXCI).

Ⓓ Check that BFULL = "0", then set the next send data to STBUFL/H.

Ⓔ When the send operation is complete, the send data set to STBUFL/H is transferred to the send register. At the same time, the serial port send interrupt signal (STINT) is generated.

Repeat step Ⓓ the required number of times.

In the synchronous external clock mode the send baud rate is determined by the input shift clock (TXCI).

To send data continuously, keep an interval of at least 3.5 clocks (approx. 107 µs) of TBCCLK for one frame of clocked (TXCI) send data.

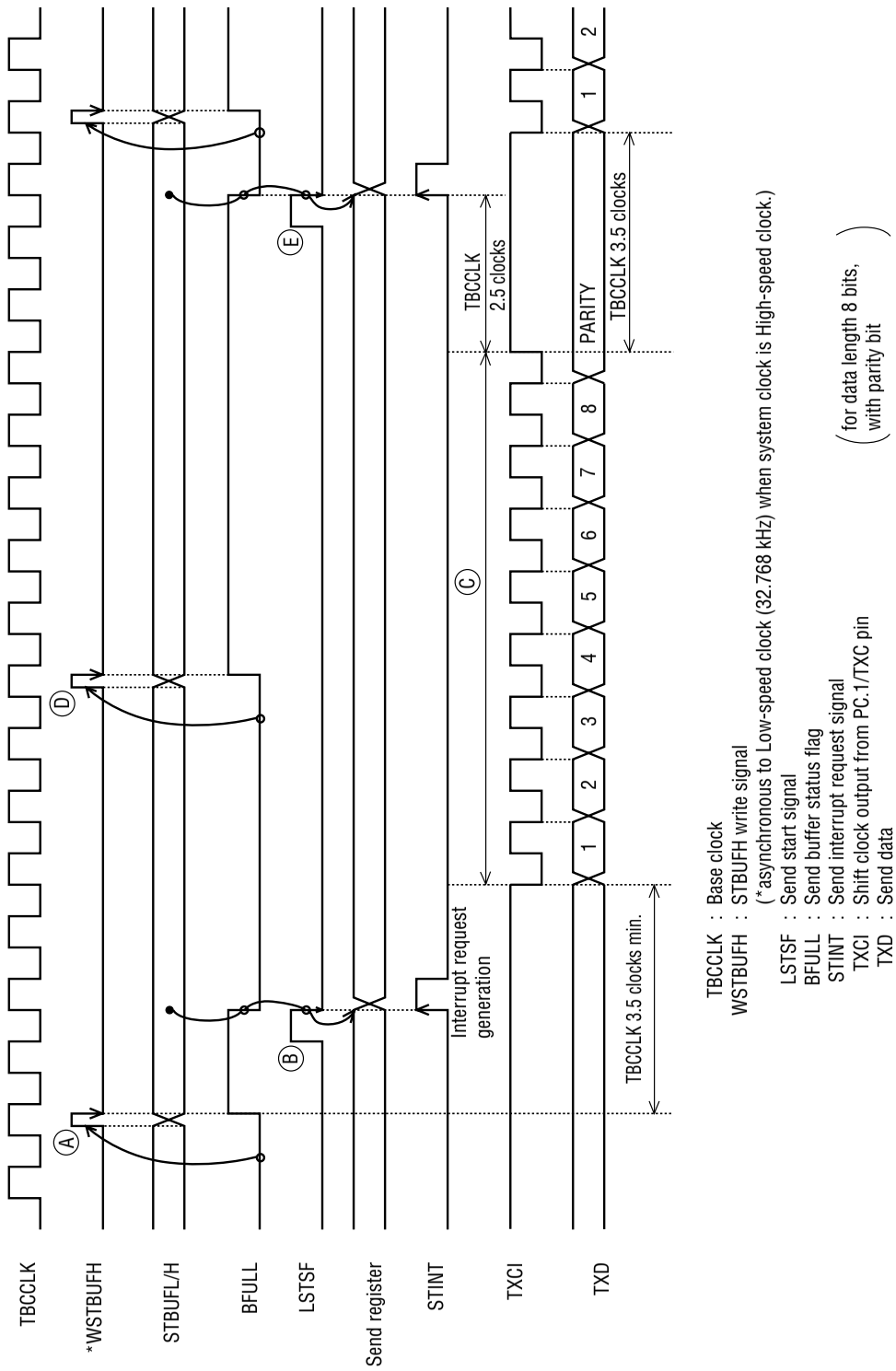


Figure 14-7 Send Timing Chart for Synchronous External Clock Mode

14.4.3 Receive Operation Description

(1) UART mode

The UART mode is specified by setting SRMOD (bit 0 of SRCON0) to "0". Figure 14-8 is the UART mode receive timing chart. The UART mode receive procedure is described below.

First set the receive baud rate in the receive baud rate setting register (SRBRT). Supported baud rates for UART mode receive are 1200, 2400, 4800, and 9600 bps.

Set the receive format (data bit length, parity bit, etc.) in SRCON0 and SRCON1.

Ⓐ Set SREN (bit 3 of SRCON0) to "1" to enable receive.

Ⓑ At the negative edge of the receive data (RXD) start bit, receive operation will start.

Ⓒ Receive operation ends.

If a framing or overrun error occurs the FERR or OERR flag of the status register (SSTAT) will be set to "1".

Ⓓ Received data is transferred to SRBUFL/H.

If a parity error occurs, the PERR flag of the status register (SSTAT) is set to "1".

Ⓔ The serial port receive interrupt request (SRINT) is generated.

Receive data is received until receive is disabled (SREN = "0"). When receive is ended, reset the receive enable/disable flag (SREN) to "0".

The receive data sampling clock (SRSMPL) is based on the low-speed clock supply, not on the high-speed clock. This allows receive operations to be executed while in the energy-saving mode.

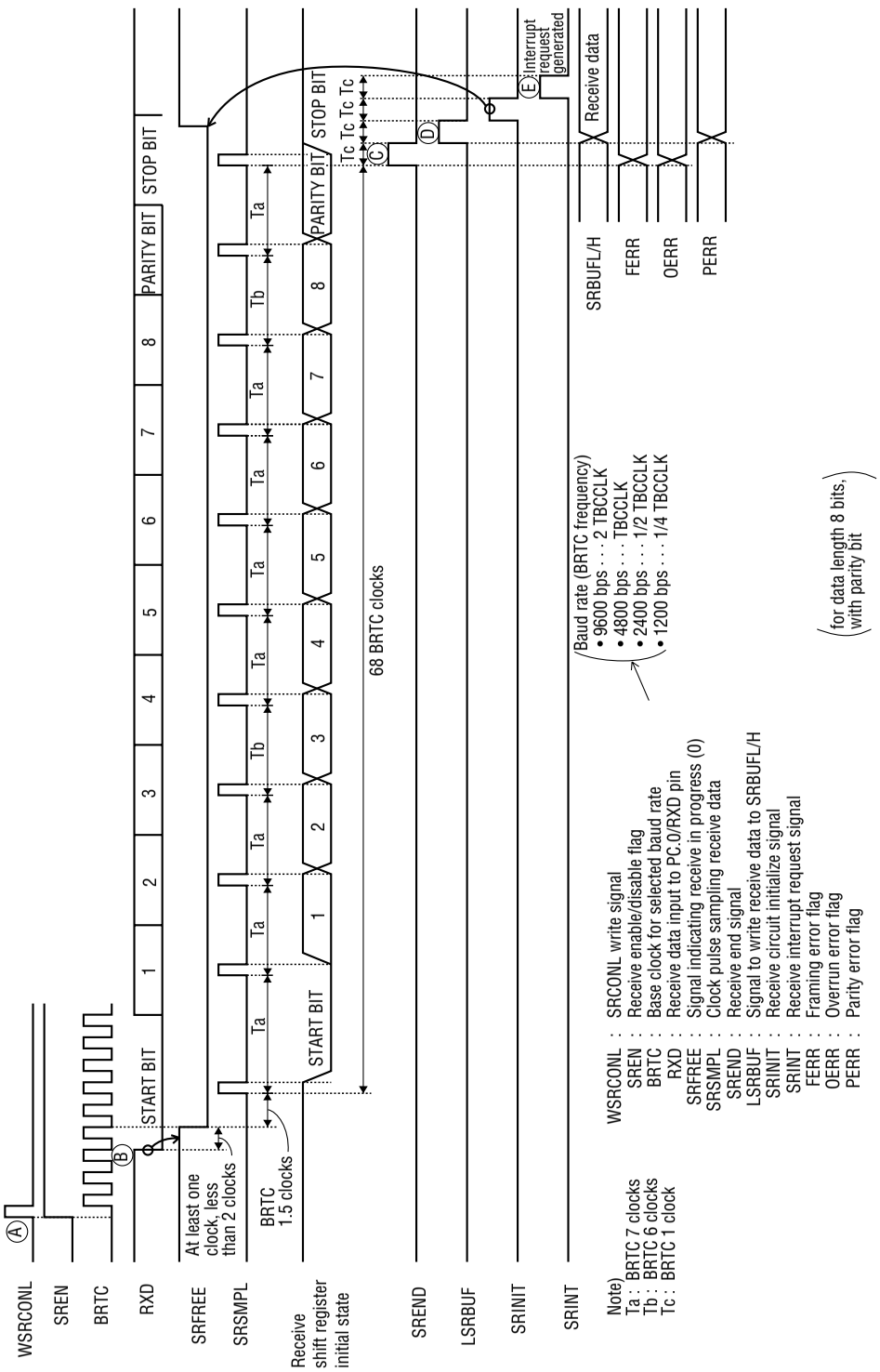


Figure 14-8 UART Mode Receive Timing Chart

(2) Synchronous internal clock mode

The synchronous internal clock mode is selected by setting SRMOD (bit 0 of SRCON0) to "1" and SRCLK (bit 0 of SRCON1) to "1".

Figure 14-9 is the receive timing chart for the synchronous internal clock mode.

The synchronous internal clock receive procedure is indicated below.

First set the receive format (data bit length, parity bit, etc.) in SRCON1 and SRCON0.

Ⓐ Set SREN (bit 3 of SRCON0) to "1" (receive enable).

Ⓑ After 3 to 4 BRTC clock cycles later the receive shift clock (RXCO) is generated, and the receive operation starts.

(The shift clock is supplied from the PC.2/RXC pin.)

Ⓒ At the positive edge of RXCO the data received from the PC.0/RXD pin is written to the receive register.

Ⓓ Receive operation ends.

If an overrun error occurs the OERR flag in status register (SSTAT) is set to "1".

Ⓔ Received data is transferred to SRBUFL/H.

If a parity error occurs, the PERR flag of status register (SSTAT) is set to "1".

Ⓕ The serial port receive interrupt request signal (SRINT) is generated.

Ⓖ At the negative edge of SRINT, SREN is reset to "0".

Repeat step Ⓐ the required number of times. In the synchronous internal clock mode the receive baud rate is fixed to TBCCLK.

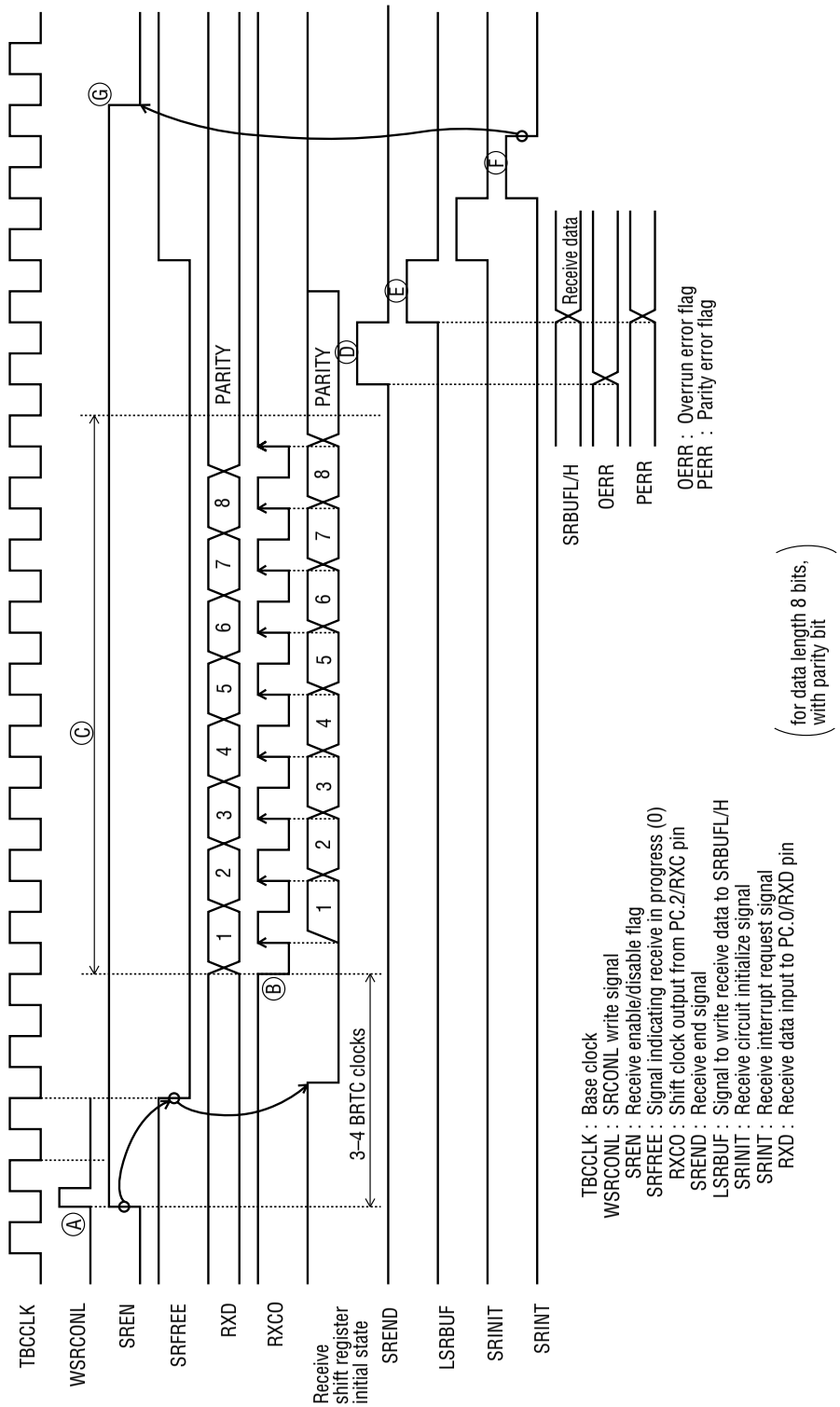


Figure 14-9 Synchronous Internal Clock Mode Receive Timing Chart

(3) Synchronous external clock mode

The synchronous external clock mode is selected by setting SRMOD (bit 0 of SRCON0) to "1" and SRCLK (bit 0 of SRCON1) to "0".

Figure 14-10 is the receive timing chart for the synchronous external clock mode.

The synchronous external clock receive procedure is indicated below.

First set the receive format (data bit length, parity bit, etc.) in SRCON1 and SRCON0.

Ⓐ Set SREN (bit 3 of SRCON0) to "1" (receive enable).

Ⓑ At the positive edge of the receive shift clock input through PC.2/RXC pin, the receive data from PC.0/RXD pin is written to the receive register.

Ⓒ Receive operation ends.

If an overrun error occurs the OERR flag in status register (SSTAT) is set to "1".

Ⓓ Received data is transferred to SRBUFL/H.

If a parity error occurs, the PERR flag of status register (SSTAT) is set to "1".

Ⓔ The serial port receive interrupt request signal (SRINT) is generated.

Ⓕ At the negative edge of SRINT, SREN is reset to "0".

Repeat step Ⓐ the required number of times.

In the synchronous external clock mode the receive baud rate is determined by the external clock (RXCI). Allow at least five clocks (approx. 153 μs) of TBCCLK between the time the receive is enabled (SREN = "1") and the time the external clock (RXCI) is input.

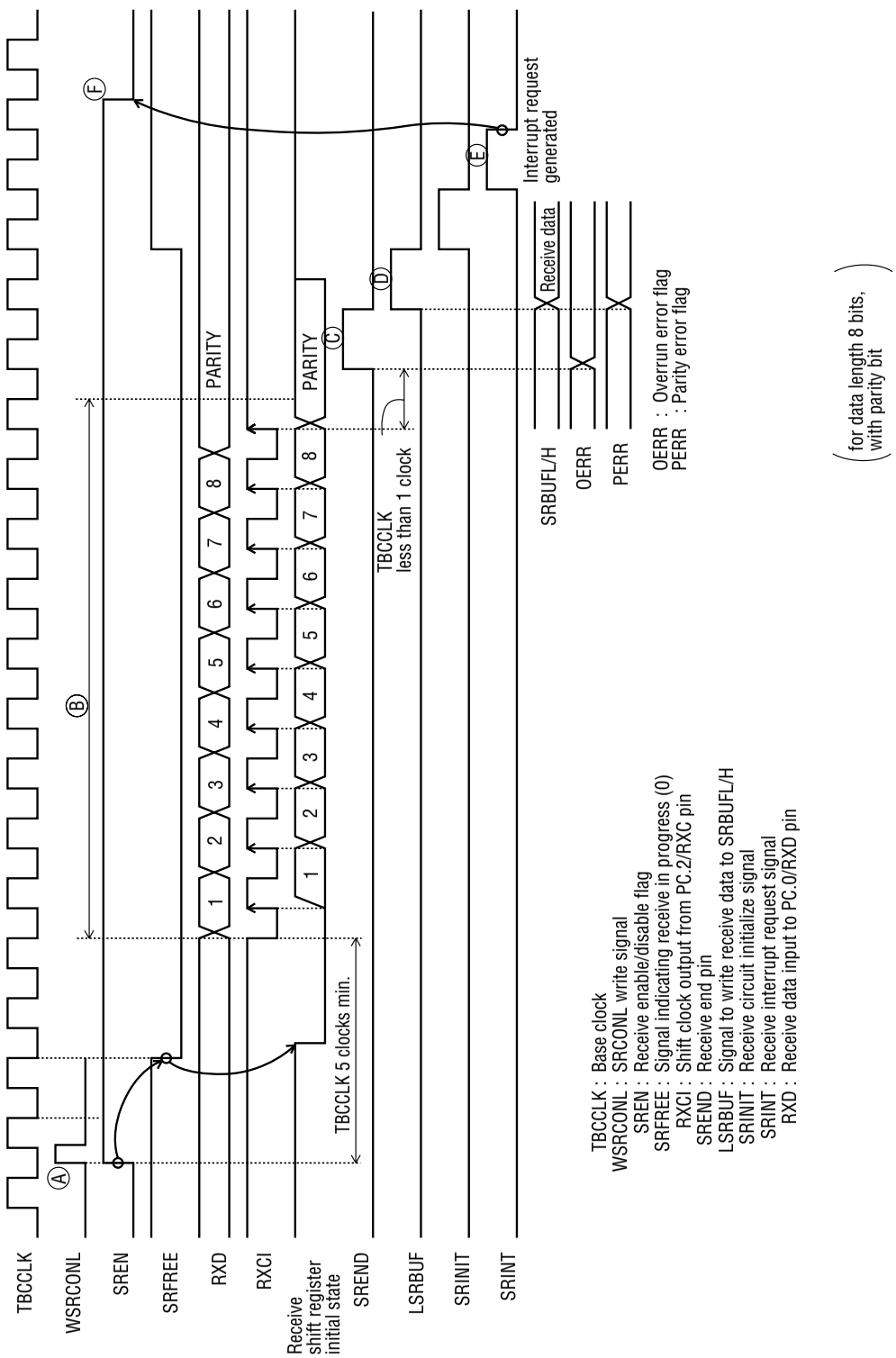


Figure 14-10 Synchronous External Clock Mode Receive Timing Chart

14.5 Send/Receive Data LSB/MSB First Select

Either LSB first or MSB first for send can be selected by setting STLMB (bit 3 of STCON1).

Either LSB first or MSB first for receive can be selected by setting SRLMB (bit 3 of SRCON1).

14.5.1 Selecting Send Data LSB/MSB First

Set STLMB (bit 3 of STCON1) to "0" to select LSB first for send.

The correspondence between LSB first send data and the send buffer register bit is shown in Figure 14-11. In this case, the LSB is TB0 (bit 0 of STBUFL)

Set STLMB to "1" to send the MSB first.

The correspondence between MSB first send data and the send buffer register bit is shown in Figure 14-12. In this case, the MSB is TB7 (bit 3 of STBUFH).

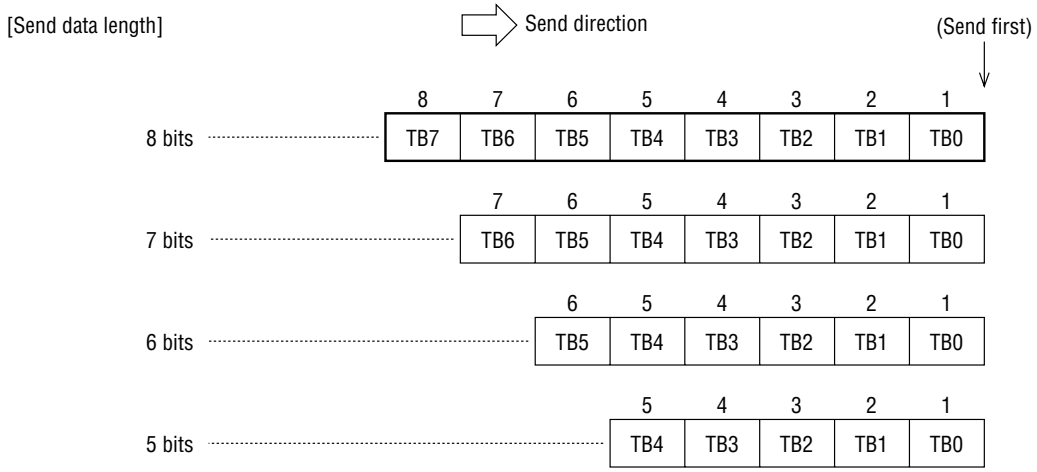


Figure 14-11 Correspondence Between LSB First Send Data and Send Buffer Register

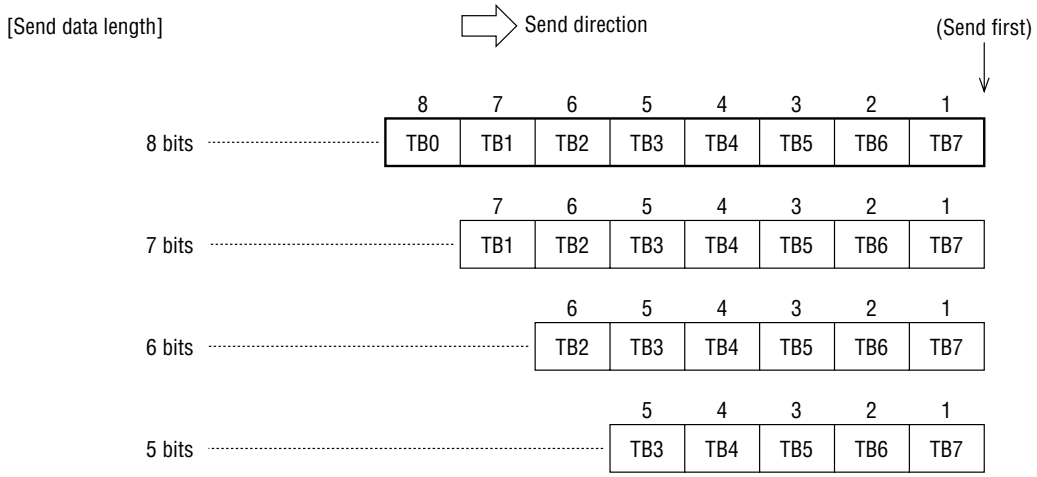


Figure 14-12 Correspondence Between MSB First Send Data and Send Buffer Register

14.5.2 Selecting Receive Data LSB/MSB First

When the LSB is first in receive data, set SRLMB (bit 3 of SRCON1) to "0".

If the MSB is first, set SRLMB to "1".

The correspondence between receive data and SRBUFL/H bits for LSB first receive is shown in Figure 14-13, and for MSB first receive in Figure 14-14.

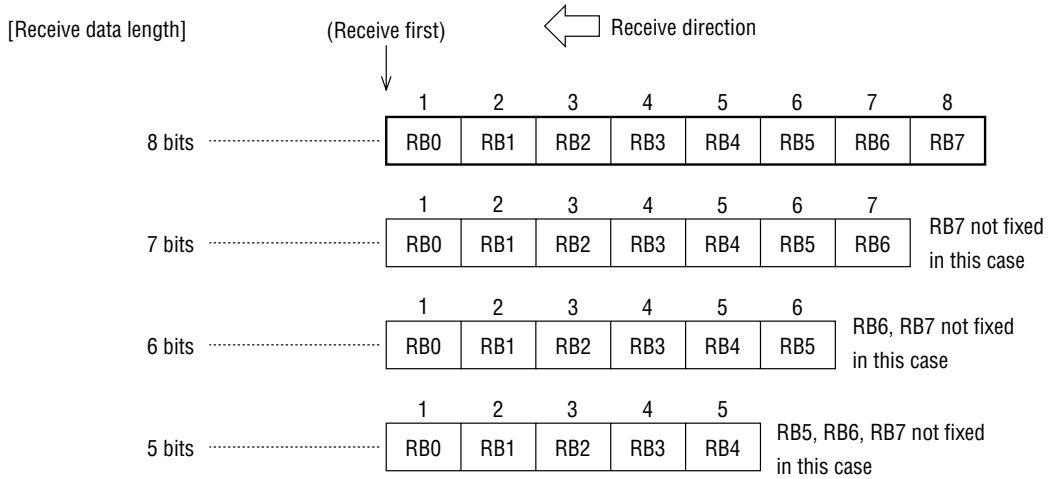


Figure 14-13 Correspondence Between LSB First Receive Data and Receive Buffer Register

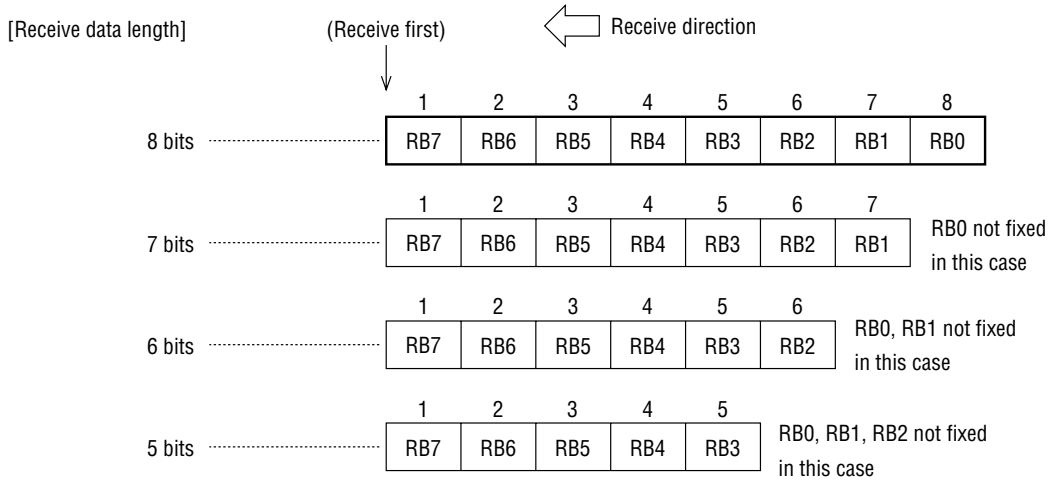


Figure 14-14 Correspondence Between MSB First Receive Data and Receive Buffer Register

Chapter 15

Shift Register (SFT)

Chapter 15 Shift Register (SFT)

15.1 Overview

The ML63187, ML63189B, and ML63193 have one internal 8-bit shift register channel for clock synchronous communication.

The shift register is synchronized with the clock specified by the shift register control register 0 (SFTCON0), and can perform 8-bit data send and receive simultaneously. When 8-bit data transfer is completed, a shift register interrupt request is generated.

15.2 Shift Register Configuration

The shift register configuration is shown in Figure 15-1.

PE.0/SIN, PE1/SOUT, and PE.2/SCLK are the shift data input pin, the shift data output pin and the shift clock input /output pin respectively. Set the secondary function by using port mode register.

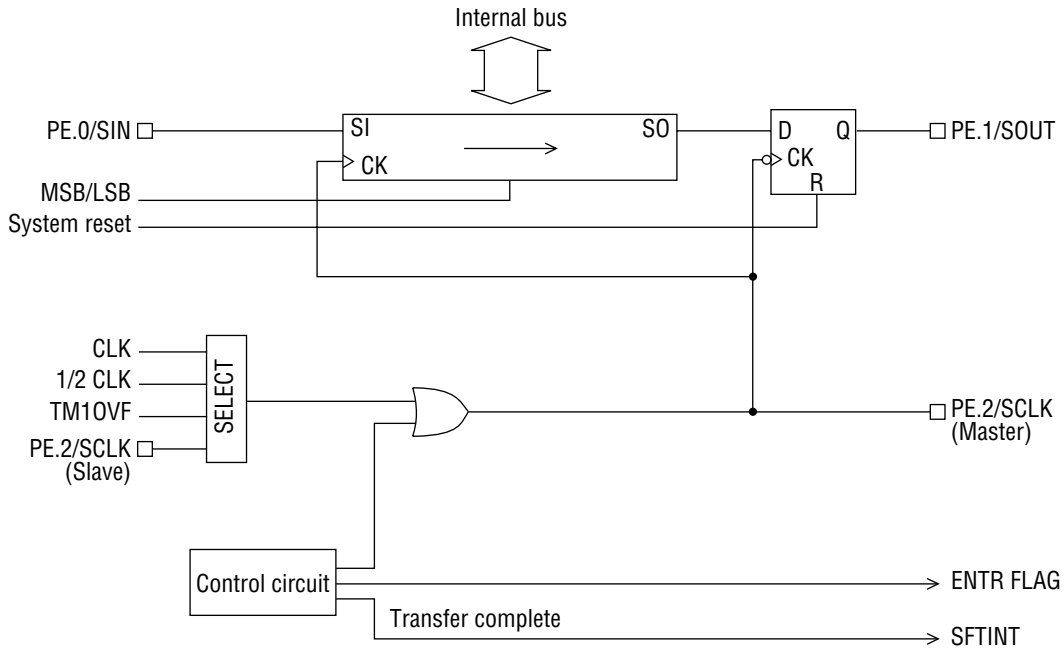


Figure 15-1 Shift Register Configuration

15.3 Shift Registers

(1) Shift registers L/H (SFTRL, SFTRH)

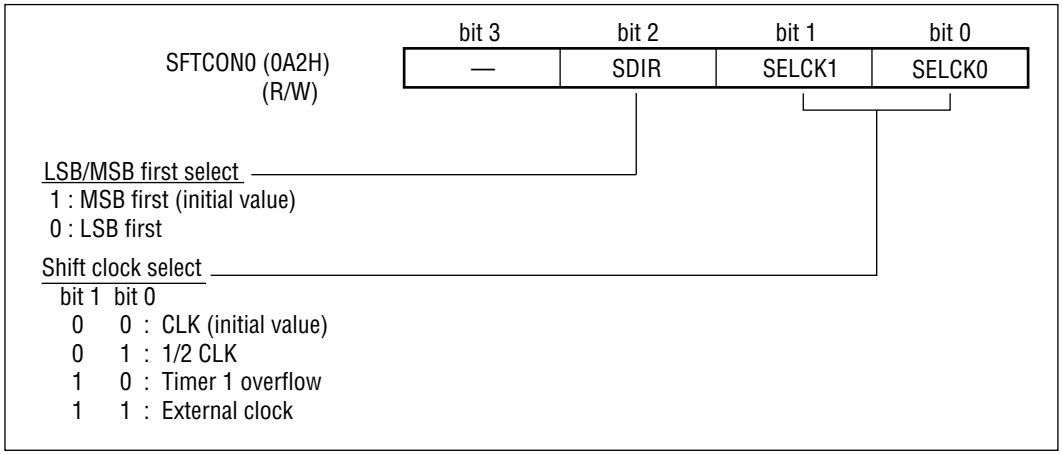
SFTRL and SFTRH are 4-bit special function registers (SFRs) used to write shift register send data and to read receive data.

	bit 3	bit 2	bit 1	bit 0
SFTRL (0A0H) (R/W)	SD3	SD2	SD1	SD0
SFTRH (0A1H) (R/W)	SD7	SD6	SD5	SD4

SFTRL and SFTRH are set to "0" at system reset.

(2) Shift register control registers (SFTCON0, SFTCON1)

SFTCON0 and SFTCON1 are 4-bit special function registers (SFRs) that control shift register operation. At system reset both are initialized to "0".



bit 2: SDIR

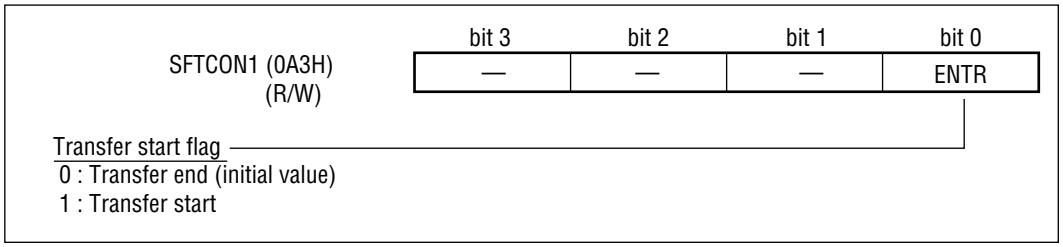
This bit selects the transfer order for 8-bit send/receive data.

When the SDIR bit is "0" it means MSB first, and when "1", LSB first.

bit 1, 0: SELCK1, SELCK0

These bits select the shift clock.

If set to CLK, 1/2 CLK or timer 1 overflow the system operates in master mode. If set to external clock the system operates in slave mode.



bit 0: ENTR

When ENTR is set to "1", transfer starts, and when 8-bit transfer ends, it is automatically set to "0".

15.4 Shift Register Operation

The shift register can be set to master or slave mode, and to MSB first or LSB first. The send data is written to the shift register (SFTRL, SFTRH), and transfer is started by setting bit 0 (ENTR) of the shift control register 1 (SFTCON1) to "1". After 8-bit data transfer (send/receive), operation ends.

Bits 1, 0 (SELCK1, SELCK0) of the shift control register 0 (SFTCON0) can set the shift clock to CLK, 1/2 CLK or timer 1 overflow. This operation is master mode and the shift clock is output to the PE.2/SCLK pin.

When the shift clock is set to external clock, the system operates in slave mode, and operation is to the clock input through the PE.2/SCLK pin. If eight or more clocks are input consecutively, the ninth and following clocks are ignored.

In both master and slave modes, the shift register is synchronized to the shift clock falling edge, and shift-out data is output from the first bit through the PE.1/SOUT pin. In synchronization with the shift clock rising edge, shift-in data is input from the first bit through the PE.0/SIN pin.

For external devices, shift-in data changes on the falling edge of the shift clock, and shift-out data changes on the rising edge of the shift clock.

When 8-bit data transfer is complete, bit 0 (ENTR) of SFTCON1 is cleared to "0". When transfer is completed, the interrupt request signal (SFTINT) is generated (see Figure 15-2).

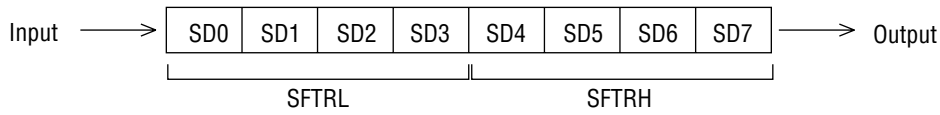
The output pin state at system reset and between transfers (from the end of one 8-bit transfer until the next transfer starts) is shown in Table 15-1 (when set to the output secondary function).

Table 15-1 Output Pin States

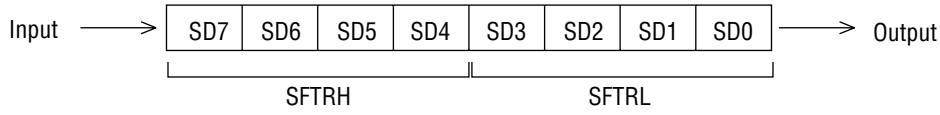
Pin name	At system reset	Between transfers
PE.2/SCLK	"H"	"H"
PE.1/SOUT	"L"	Last transfer data of transfer

MSB/LSB first is set to bit 2 (SDIR) of SFTCON0.

• SDIR = 0 : MSB first mode



• SDIR = 1 : LSB first mode



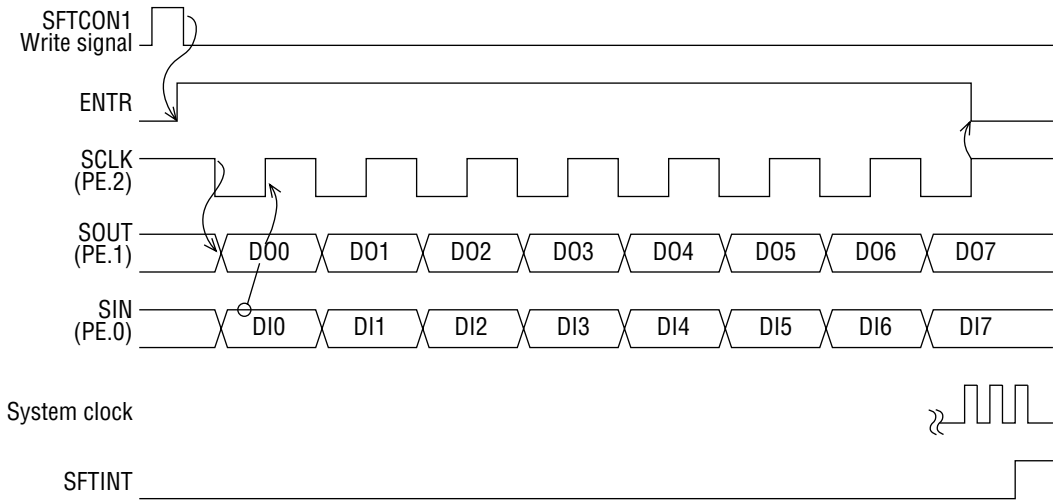


Figure 15-2 Shift Register Operation Timing

Note :

Setting the ENTR bit to "1" in the slave mode should be done when the PE.2/SCLK pin is high.

If SFTRL/SFTRH are written during transfer, the transfer data (send and receive) is destroyed. In this case, terminate the transfer and start over again.

Even when receiving only, transfer begins with setting the ENTR bit to "1".

15.5 Shift Register Application Example

An example of register setting for clock synchronous communication using shift register is described below.

(1) Set the supported port modes (secondary function).

Port control register	Master mode	
PEMOD	Bit 2 = "1"	(PE.2/SCLK)
	Bit 1 = "1"	(PE.1/SOUT)
	Bit 0 = "1"	(PE.0/SIN)

(2) Select the shift clock with SELCK1, SELCK0 (SFTCON0 bits 1, 0)(master/slave mode select).

(3) Select MSB first/LSB first with SDIR (SFTCON0 bit 2). ("0" for MSB first, "1" for LSB first).

(4) Set ESFT (IE3 bit 2) to "1" and enable the shift register interrupt.

(5) Set the MIE (master interrupt enable flag) to "1", and enable all interrupts.

(6) Write send data to SFTRL and SFTRH.

(7) Set ENTR (bit 0 of SFTCON1) to "1", and start the transfer.

With the above settings the shift register begins to operate, and the CPU receives the shift register interrupt. Whether 8-bit transfer has been completed can be checked by monitoring QSFT (bit 2 of IRQ3) or ENTR (bit 0 of SFTCON1).

Chapter 16

LCD Driver (LCD)

Chapter 16 LCD Driver (LCD)

16.1 Overview

The ML63187, ML63189B, and ML63193 have an internal dot matrix LCD driver. They also have 64 segment outputs and can drive up to 1024 (64 seg. × 16 com.) dots. The LCD driver can be software-selected to all OFF, all ON or power down mode, 1/4 or 1/5 bias, selectable duty from 1/1 to 1/16, and adjustable (16-tone) contrast.

16.2 LCD Driver Configuration

The LCD driver configuration is shown in Figure 16-1.

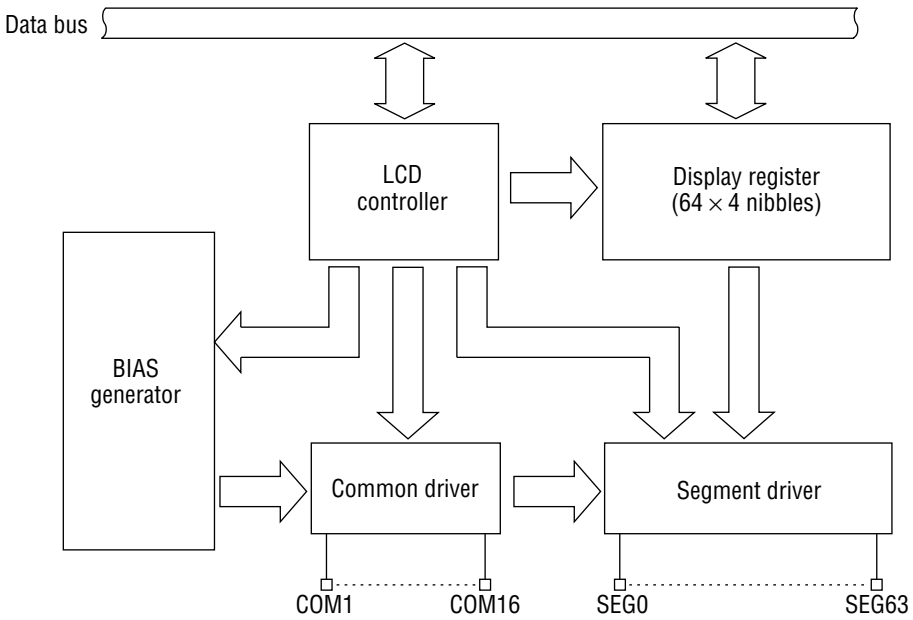
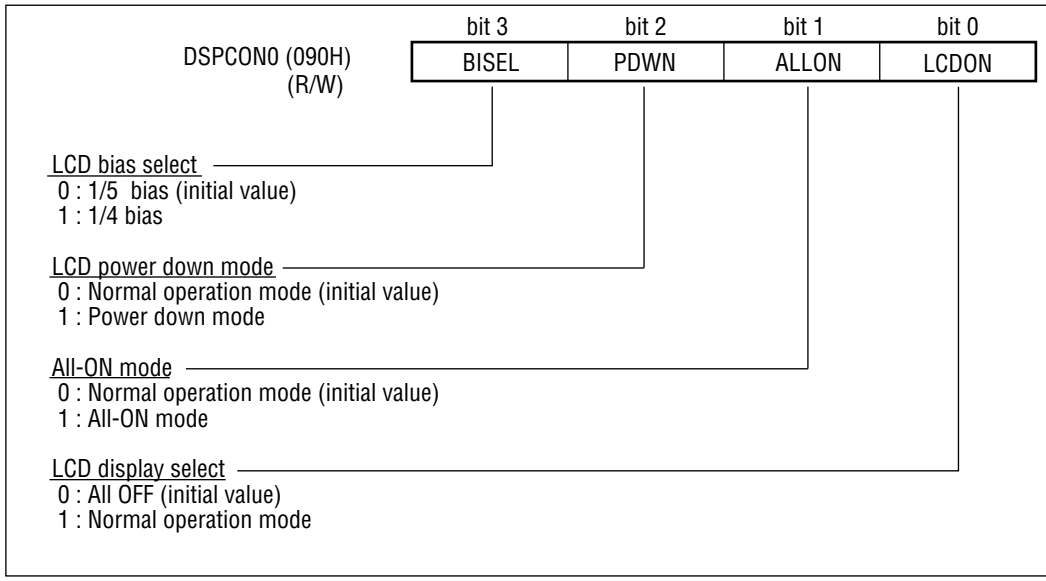


Figure 16-1 LCD Driver Configuration

16.3 LCD Driver Registers

(1) Display control register 0 (DSPCON0)

DSPCON0 is a 4-bit special function register (SFR) controlling LCD driver operation.



bit 3: BISEL
This bit selects 1/4 or 1/5 bias.
At system reset it is "0", selecting 1/5 bias.

bit 2: PDWN
This bit selects the LCD power down mode. When PDWN is set to "1", the bias generation circuit stops its voltage lowering/raising operation and pins COM1–16 and SEG0–63 are all set to the V_{SS} level, reducing supply current. At system reset it is cleared to "0".

bit 1: ALLON
When ALLON is set to "1" all segment drivers are turned on. The ALLON bit has priority over the LCDON bit. At system reset it is cleared to "0".

bit 0: LCDON
When the LCDON bit is set to "1", the display data in the display register is output to the segment drivers. At system reset it is cleared to "0", and all segment drivers are turned off.

(2) Display control register 1 (DSPCON1)

DSPCON1 is a 4-bit special function register (SFR) used to select the LCD driver duty.

At system reset, bits of DSPCON1 are initialized to "0".

DSPCON1 (091H) (R/W)

bit 3	bit 2	bit 1	bit 0
DT3	DT2	DT1	DT0

Duty select

bit 3	bit 2	bit 1	bit 0	
0	0	0	0	: 1/16 duty (initial value)
0	0	0	1	: 1/1 duty
0	0	1	0	: 1/2 duty
0	0	1	1	: 1/3 duty
0	1	0	0	: 1/4 duty
0	1	0	1	: 1/5 duty
0	1	1	0	: 1/6 duty
0	1	1	1	: 1/7 duty
1	0	0	0	: 1/8 duty
1	0	0	1	: 1/9 duty
1	0	1	0	: 1/10 duty
1	0	1	1	: 1/11 duty
1	1	0	0	: 1/12 duty
1	1	0	1	: 1/13 duty
1	1	1	0	: 1/14 duty
1	1	1	1	: 1/15 duty

(3) Display contrast register (DSPCNT)

DSPCNT is a 4-bit special function register (SFR) used to adjust display contrast.

At system reset, bits of DSPCON1 are initialized to "0".

DSPCNT (092H) (R/W)

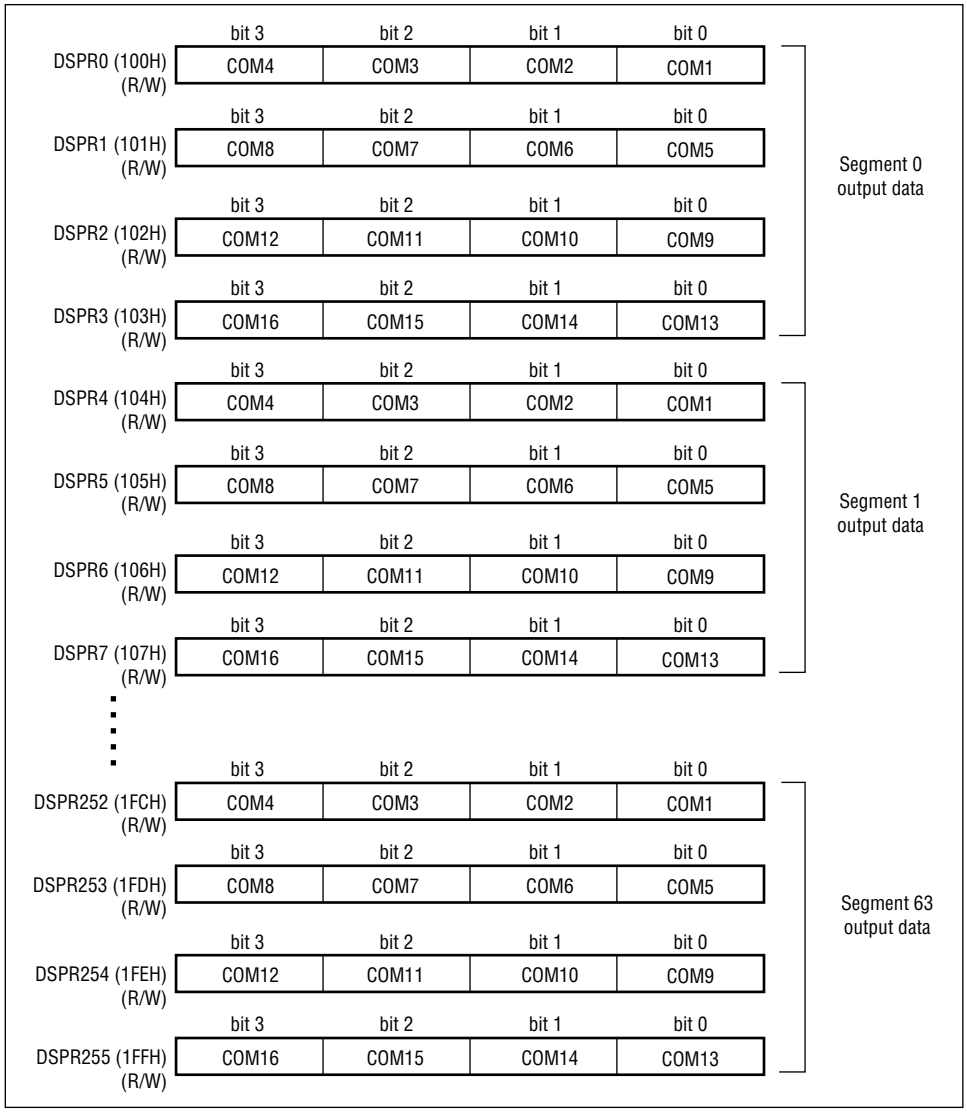
bit 3	bit 2	bit 1	bit 0
CN3	CN2	CN1	CN0

Contrast select

bit 3	bit 2	bit 1	bit 0	
0	0	0	0	: Light (initial value)
0	0	0	1	:
0	0	1	0	:
0	0	1	1	:
0	1	0	0	:
0	1	0	1	:
0	1	1	0	:
0	1	1	1	:
1	0	0	0	:
1	0	0	1	:
1	0	1	0	:
1	0	1	1	:
1	1	0	0	:
1	1	0	1	:
1	1	1	0	:
1	1	1	1	: Dark

(4) Display registers (DSPR0 to DSPR255)

DSPR0 to DSPR255 are segment output data registers for the dot matrix LCD driver allocated to RAM BANK 1. The correspondence between display registers and segment outputs is shown below.



Notes:

- When a display register bit is set to "1", the corresponding LCD dot lights. When reset to "0" it goes off.
- To keep stable display state, each individual LCD dot should be set to ON/OFF with bit operation instructions.
- At system reset the display registers (DSPR0 to DSPR255) are undefined and should be initialized.

16.4 LCD Driver Operation

The display duty is selected from 1/1 to 1/16 using DSPCON. The frame frequency for each duty ratio is indicated in Table 16-1. Depending on the duty selected, the common signal (COM1 to COM16) is generated, and data written in synchronization with that common signal to the display registers (DSPR0 to DSPR255) is output to the segment driver. The segment driver uses bits 0, 1 (ALLON, LCDON) of the display control register 0 (DSPCON0) to control all OFF or all ON modes.

When PDWN (bit 2 of DSPCON0) is set to "1", the LCD power down mode is enabled. In the LCD power-down mode the bias generation circuit operation stops, and COM1–16 and SEG0–63 pins are all output at the V_{SS} level to reduce supply current.

BISEL (bit3 of DSPCON0) selects 1/4 or 1/5 bias.

DSPCNT controls the LCD contrast of 16 tones (V_{DDH} = 2.4 V or more).

When the LCD driver is not used, select the power-down mode and set all the bits of the display control register (DSPCNT) to "0" to save the supply current.

Table 16-1 Frame Frequency for Each Duty

DSPCON1					Duty	Frame frequency
DT3–0	DT3	DT2	DT1	DT0		
0H	0	0	0	0	1/16	64 Hz
1H	0	0	0	1	1/1	1024 Hz
2H	0	0	1	0	1/2	512 Hz
3H	0	0	1	1	1/3	approx. 341 Hz
4H	0	1	0	0	1/4	256 Hz
5H	0	1	0	1	1/5	approx. 205 Hz
6H	0	1	1	0	1/6	approx. 171 Hz
7H	0	1	1	1	1/7	approx. 146 Hz
8H	1	0	0	0	1/8	128 Hz
9H	1	0	0	1	1/9	approx. 114 Hz
0AH	1	0	1	0	1/10	approx. 102 Hz
0BH	1	0	1	1	1/11	approx. 93 Hz
0CH	1	1	0	0	1/12	approx. 85 Hz
0DH	1	1	0	1	1/13	approx. 79 Hz
0EH	1	1	1	0	1/14	approx. 73 Hz
0FH	1	1	1	1	1/15	approx. 68 Hz

16.5 Bias Generator (BIAS)

The bias generator is used to multiply and divide the voltage (V_{DD2}) generated in the constant voltage circuit with an external capacitor connected to pins C1, C2 to generate V_{DD1} to V_{DD5} bias voltages for the LCD driver.

The LCD power down mode stops the voltage lowering/raising operation of the bias generation circuit in order to reduce supply current.

Figure 16-2 shows the bias generator configuration for 1/5 bias, and Figure 16-3 shows the configuration for 1/4 bias. For details of the backup circuit and the constant-voltage circuit, see Chapter 19, "Backup Circuit."

Tables 16-2 and 16-3 show the table of display contrast adjusting voltages.

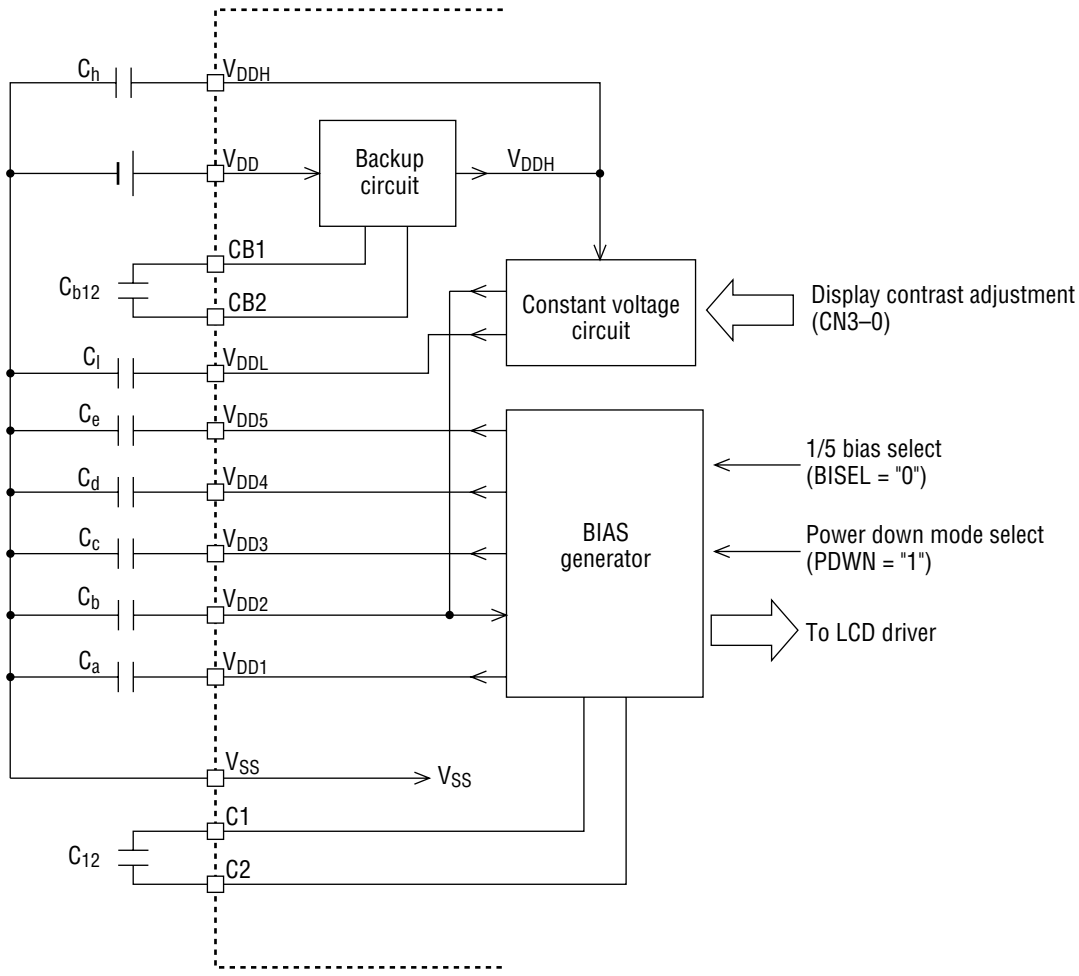


Figure 16-2 Bias Generator Configuration for 1/5 Bias

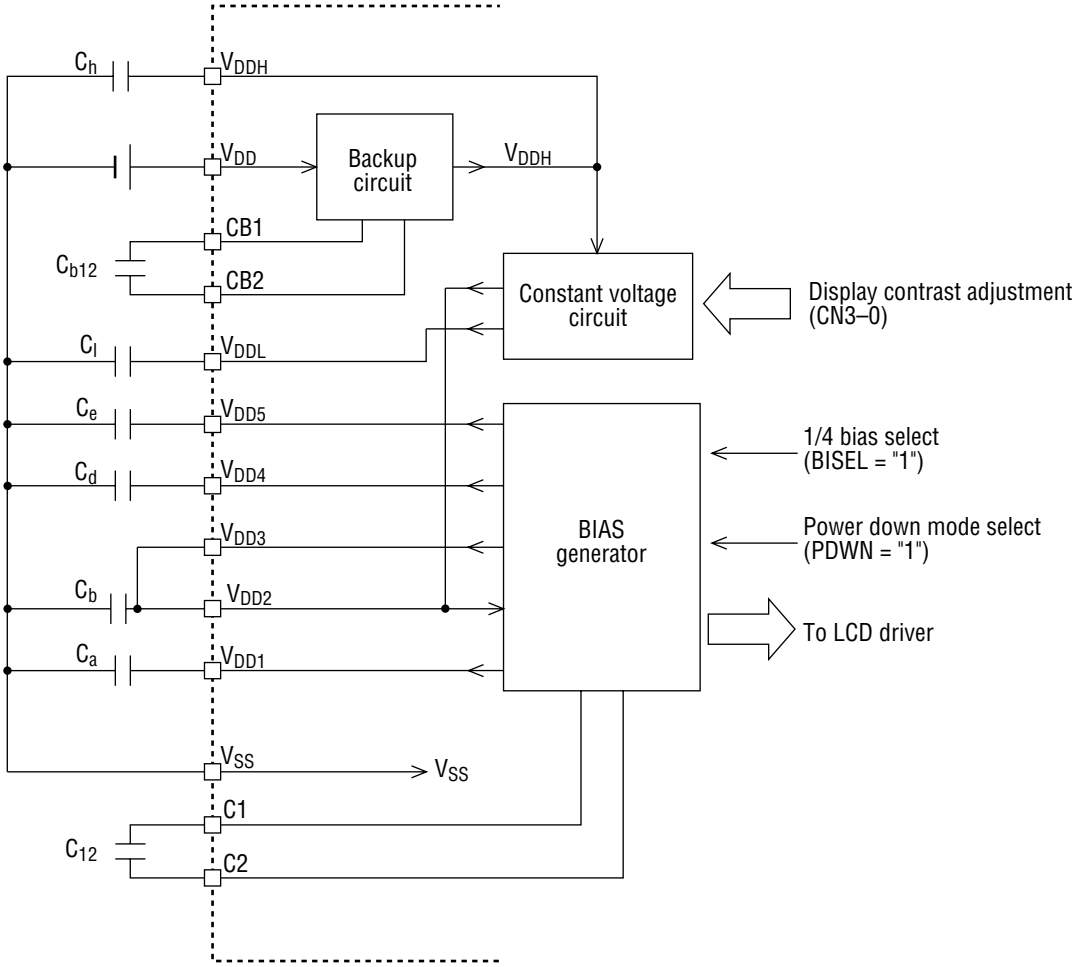


Figure 16-3 Bias Generator Configuration for 1/4 Bias

Table 16-2 Display Contrast Adjusting Voltages (V_{DD2})

(Ta = 25°C, V_{SS} = 0 V)

DSPCNT					V_{DD2} Voltage (V)			Contrast
CN3–0	CN3	CN2	CN1	CN0	Min.	Typ.	Max.	
0H	0	0	0	0	1.70	1.80	1.90	Light
1H	0	0	0	1	1.74	1.84	1.94	
2H	0	0	1	0	1.78	1.88	1.98	
3H	0	0	1	1	1.82	1.92	2.02	
4H	0	1	0	0	1.86	1.96	2.06	
5H	0	1	0	1	1.90	2.00	2.10	
6H	0	1	1	0	1.94	2.04	2.14	
7H	0	1	1	1	1.98	2.08	2.18	
8H	1	0	0	0	2.02	2.12	2.22	
9H	1	0	0	1	2.06	2.16	2.26	
0AH	1	0	1	0	2.10	2.20	2.30	
0BH	1	0	1	1	2.14	2.24	2.34	
0CH	1	1	0	0	2.18	2.28	2.38	
0DH	1	1	0	1	2.22	2.32	2.42	
0EH	1	1	1	0	2.26	2.36	2.46	
0FH	1	1	1	1	2.30	2.40	2.50	Dark

Table 16-3 Display Contrast Adjusting Voltages (V_{DD1}, V_{DD3}, V_{DD4}, V_{DD5})

(V_{SS} = 0 V)

BISEL	Mode	Power supply	Voltage (V)		
			Min.	Typ.	Max.
0	1/5 bias	V_{DD1}	Typ. – 0.1	$1/2 \times V_{DD2}$*	Typ. + 0.1
		V_{DD3}	Typ. – 0.3	$3/2 \times V_{DD2}$*	Typ. + 0.3
		V_{DD4}	Typ. – 0.4	$2 \times V_{DD2}$*	Typ. + 0.4
		V_{DD5}	Typ. – 0.5	$5/2 \times V_{DD2}$*	Typ. + 0.5
1	1/4 bias	V_{DD1}	Typ. – 0.1	$1/2 \times V_{DD2}$*	Typ. + 0.1
		V_{DD3}	Typ. – 0.2	V_{DD2}*	Typ. + 0.2
		V_{DD4}	Typ. – 0.3	$3/2 \times V_{DD2}$*	Typ. + 0.3
		V_{DD5}	Typ. – 0.4	$2 \times V_{DD2}$*	Typ. + 0.4

V_{DD2}*: Typical V_{DD2} in Table 16-2

16.6 LCD Driver Output Waveform

Figures 16-4 (a) and 16-4 (b) show the output waveforms for 1/16 duty and 1/5 bias, and Figures 16-5 (a) and 16-5 (b) show the output waveforms for 1/8 duty and 1/4 bias.

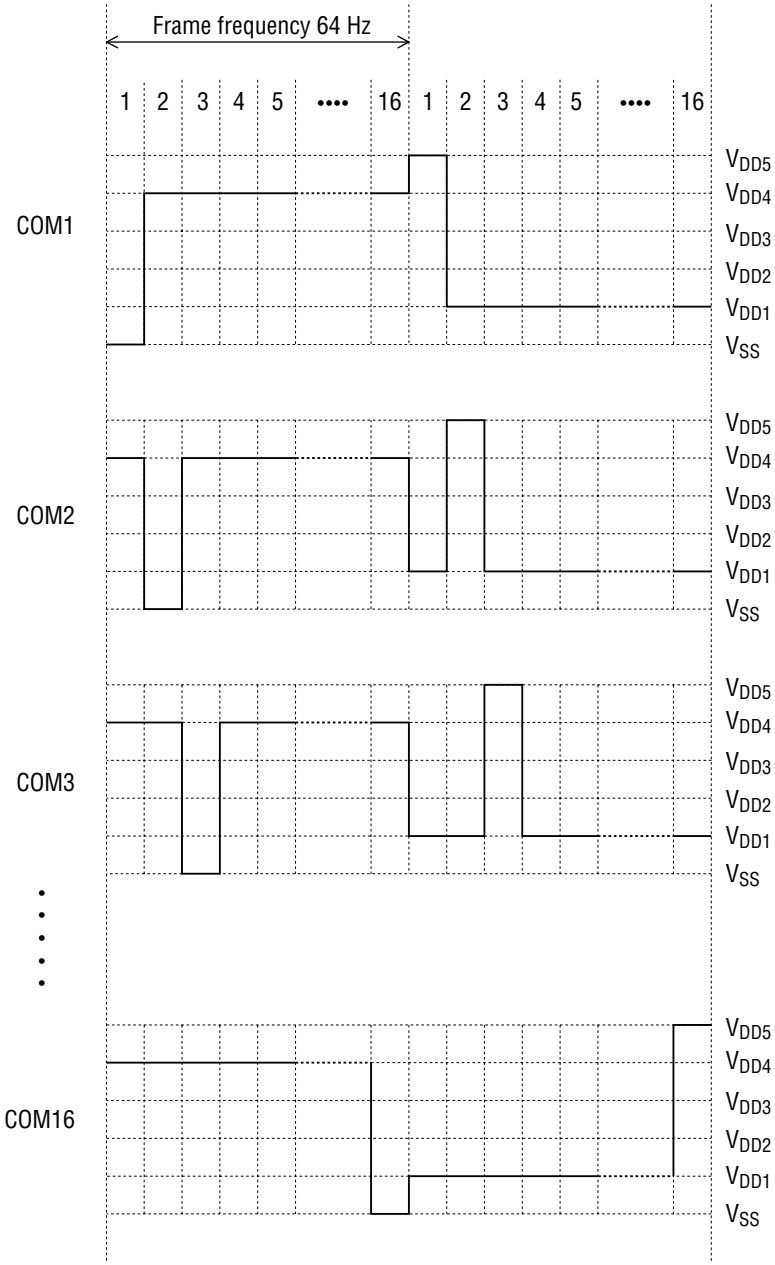


Figure 16-4 (a) 1/16 Duty, 1/5 Bias Common Output Waveform

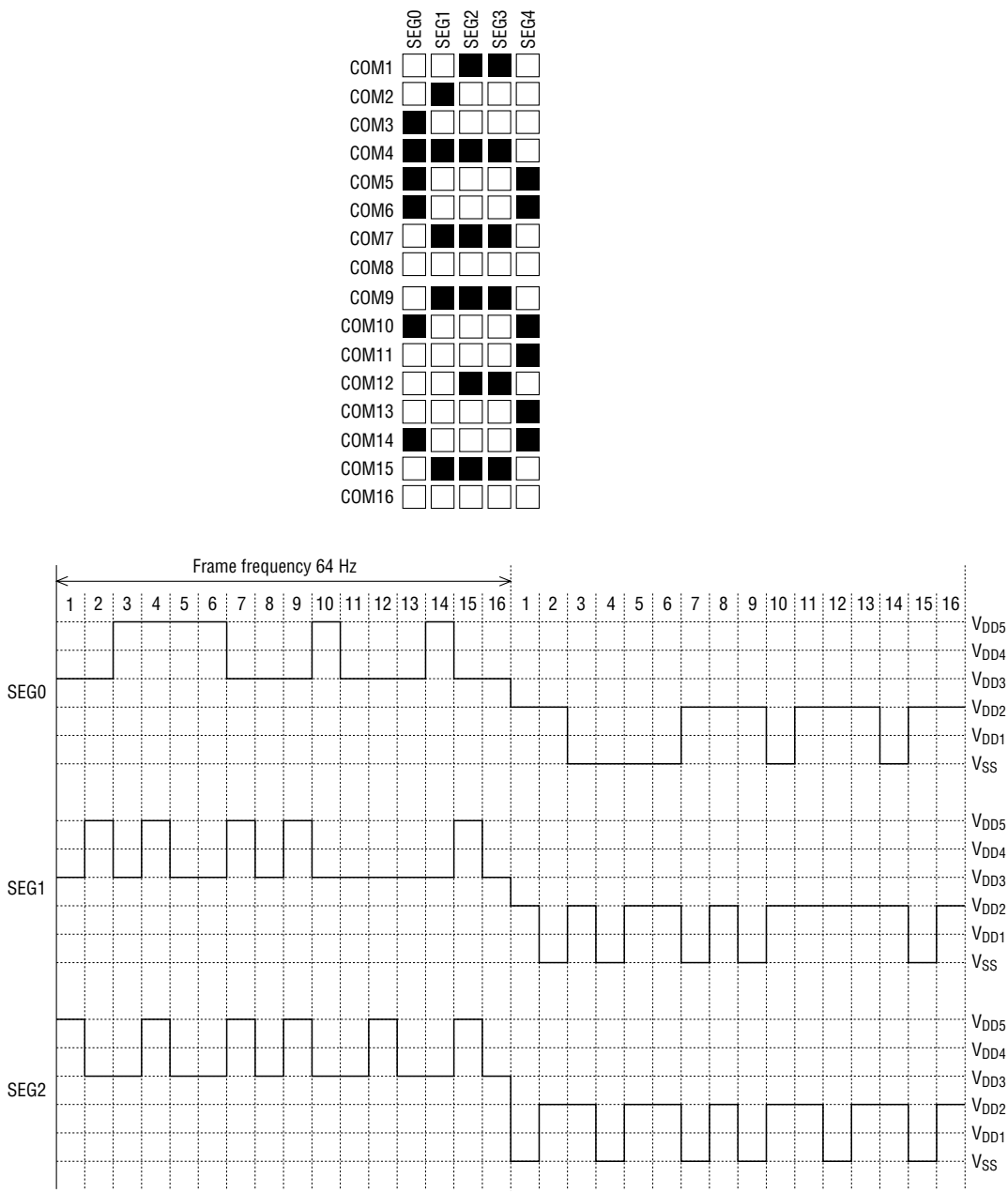


Figure 16-4 (b) 1/16 Duty, 1/5 Bias Segment Output Waveform

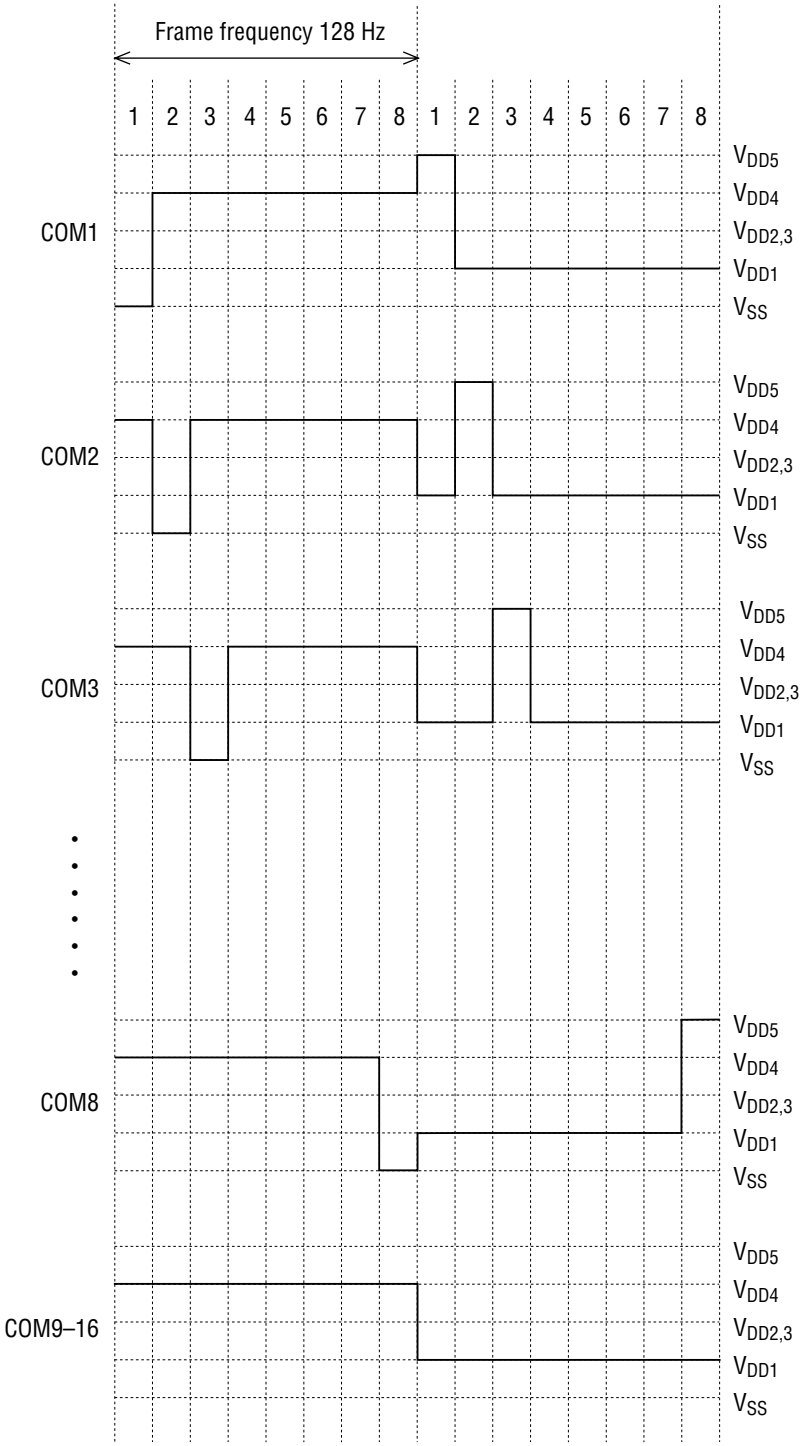


Figure 16-5 (a) 1/8 Duty, 1/4 Bias Common Output Waveform

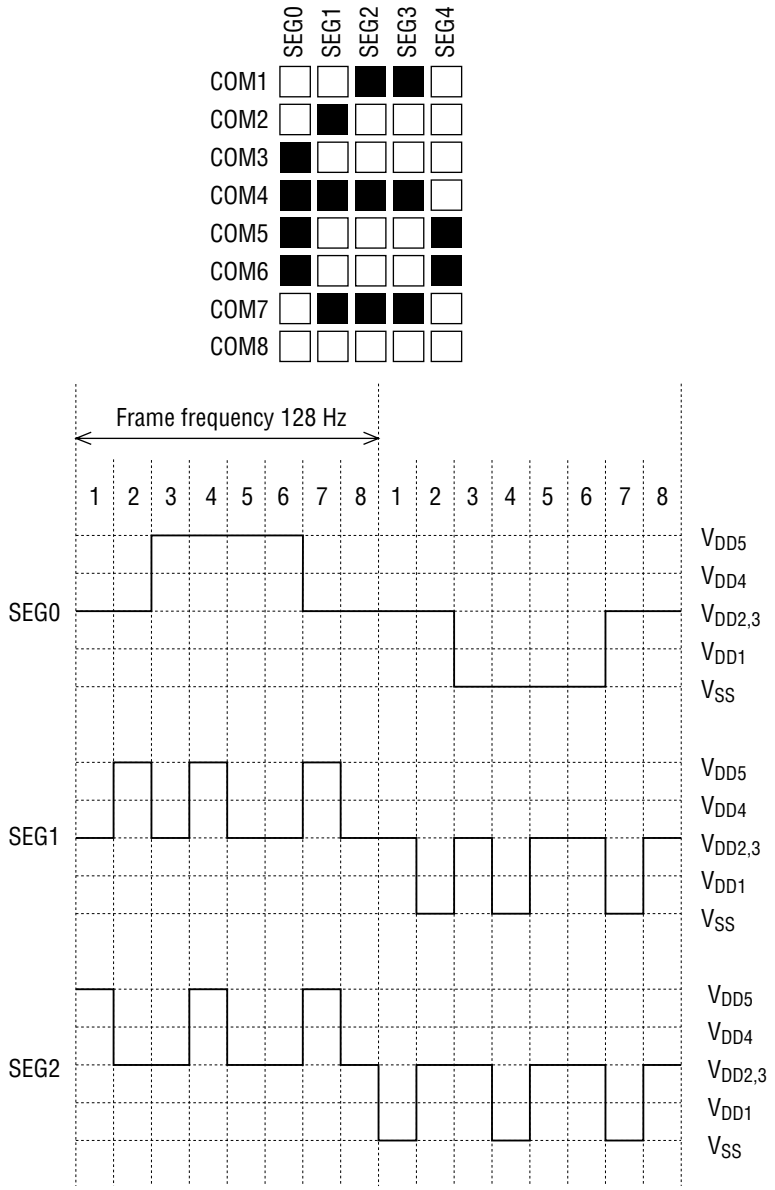


Figure 16-5 (b) 1/8 Duty, 1/4 Bias Segment Output Waveform

Chapter 17

Multiplication/Division Circuit (MULDIV)

Chapter 17 Multiplication/Division Circuit (MULDIV)

17.1 Overview

The ML63193 has an 8-bit × 8-bit = 16-bit multiplication (MUL) and a 16-bit/8-bit = 16-bit division (DIV), implemented with an internal circuit.

The registers used are shown in Table 17-1.

Table 17-1 Registers Used in Multiplication and Division Circuit

Register name	Symbol	Address	bit 3	bit 2	bit 1	bit 0	R/W	Value at system reset
Multiplication/division condition register	MDCR	086H	OV	EF	DIVS	MULS	R/W	0H
C register L	CRL	087H	CR3	CR2	CR1	CR0	R/W	0H
C register H	CRH	088H	CR7	CR6	CR5	CR4	R/W	0H
D register L	DRL	089H	DR3	DR2	DR1	DR0	R/W	0H
D register H	DRH	08AH	DR7	DR6	DR5	DR4	R/W	0H
E register L	ERL	08BH	ER3	ER2	ER1	ER0	R/W	0H
E register H	ERH	08CH	ER7	ER6	ER5	ER4	R/W	0H
F register L	FRL	08DH	FR3	FR2	FR1	FR0	R/W	0H
F register H	FRH	08EH	FR7	FR6	FR5	FR4	R/W	0H

For multiplication the C register is multiplied by the E register. The result is stored in the DC register (D: high-order 8 bits, C: low-order 8 bits) after 5 machine cycles.

For division the D register is divided by the E register. The result is stored in the DC register (dividend) and F register (remainder) after 10 machine cycles.

17.2 Multiplication and Division Registers

17.2.1 Calculation Registers

The multiplication and division calculation registers (CRL, CRH, DRL, DRH, ERL, ERH, FRL, FRH) are 4-bit special function registers (SFRs), used to set multiplier, multiplicand, divisor, and dividend and store results.

	bit 3	bit 2	bit 1	bit 0
CRL (087H) (R/W)	CR3	CR2	CR1	CR0
CRH (088H) (R/W)	CR7	CR6	CR5	CR4

	bit 3	bit 2	bit 1	bit 0
DRL (089H) (R/W)	DR3	DR2	DR1	DR0
DRH (08AH) (R/W)	DR7	DR6	DR5	DR4

	bit 3	bit 2	bit 1	bit 0
ERL (08BH) (R/W)	ER3	ER2	ER1	ER0
ERH (08CH) (R/W)	ER7	ER6	ER5	ER4

	bit 3	bit 2	bit 1	bit 0
FRL (08DH) (R/W)	FR3	FR2	FR1	FR0
FRH (08EH) (R/W)	FR7	FR6	FR5	FR4

The multiplication and division calculation registers are used as follows.

[Multiplication]

DR•CR←CR × ER

CR (CRH, CRL): Holds the multiplicand. After multiplication, holds the low-order 8 bits of the result.

ER (ERH, ERL): Holds the multiplier. After multiplication, holds data.

DR (DRH, DRL): After execution, the high-order 8 bits of the result are stored.

If the result of multiplication cannot be stored in the low-order 8 bits (DR is not 0), the multiplication/division condition register (MDCR) OV flag is set to "1". When bit 0 (MULS) of MDCR is set to "1", multiplication starts, and the result is output to the appropriate registers five machine cycles later.

[Division]

DR•CR←DR•CR/ER

FR←DR•CR mod ER

DR (DRH, DRL): The high-order 8 bits of the number being divided are set here. After execution, this register holds the high-order 8 bits of the result.

CR (CRH, CRL): The low-order 8 bits of the number being divided are set here. After execution, this register holds the low-order 8 bits of the result.

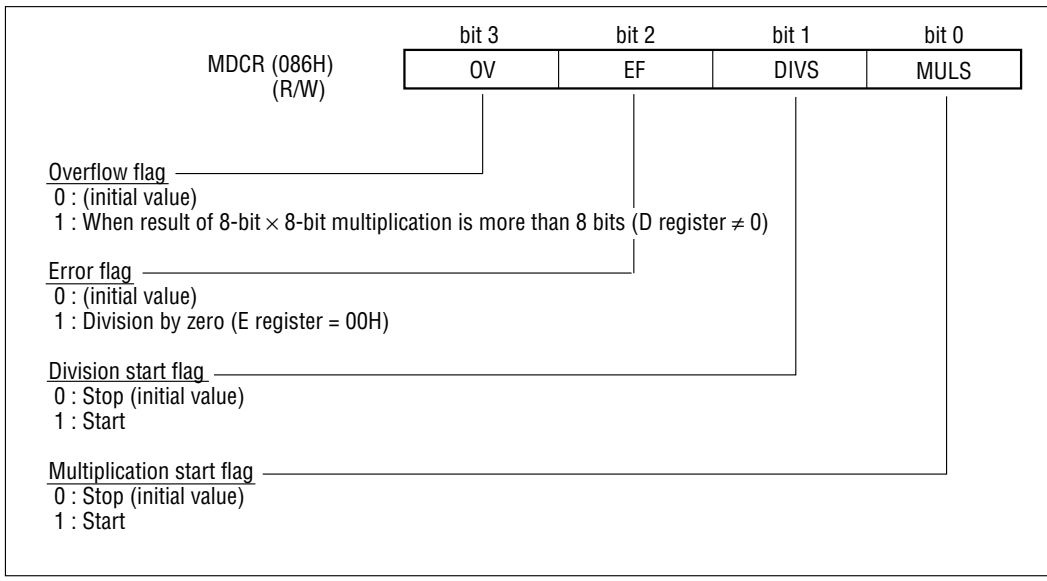
ER (ERH, ERL): The divisor is set here. After execution, this register holds data.

FR (FRH, FRL): After execution, this register holds the remainder.

If division is executed with ER = 00H (division by zero), the MDCR EF flag is set to "1". After division by zero the DC register value is 0FFFFH, and the pre-execution value from the C register is set to the F register. When bit 1 (DIVS) of MDCR is set to "1", division begins and the result is output to the appropriate registers ten machine cycles later.

17.2.2 Multiplication/Division Condition Register

The multiplication/division condition register (MDCR) is a 4-bit special function register (SFR) with a multiplication/division start flag and a status flag indicating the status of the operation when finished.



bit 3: OV (OVerflow flag)

Set to "1" when there is a carry (D register other than 00H) to the high-order 8 bits in multiplication, and otherwise cleared to "0".

This bit is initialized to "0" at system reset.

bit 2: EF (Error Flag)

Set to "1" when the E register is "0" in division, and otherwise cleared to "0".

This bit is initialized to "0" at system reset.

bit 1: DIVS (DIV Start)

Division is started when this bit is set to "1", and is completes in ten machine cycles. When division is complete DIVS is reset to "0".

This bit initializes to "0" at system reset.

bit 0: MULS (MUL Start)

This flag starts multiplication when set to "1", and multiplication is completes in five machine cycles. MULS is cleared to "0" when multiplication is complete.

This bit is reset to "0" at system reset.

17.3 Multiplication/Division Execution

Multiplication and division execution is handled as follows.

[Multiplication]

1. Multiplicand set to C register (CRH, CRL)
2. Multiplier set to E register (ERH, ERL)
3. MDCR MULS flag set to "1".

[Division]

1. High-order 8 bits of number being divided set to D register (DRH, DRL), and low-order 8 bits to C register (CRH, CRL).
2. Divisor set to E register (ERH, ERL).
3. MDCR DIVS flag set to "1".

Chapter 18

Battery Low Detect Circuit (BLD)

Chapter 18 Battery Low Detect Circuit (BLD)

18.1 Overview

The ML63187, ML63189B, and ML63193 have an internal battery low detect circuit (BLD).

The battery low detect circuit detects when the battery voltage (supply voltage V_{DD}) falls below the judgment voltage value. Four levels of judgment voltage can be selected by the BLDCON bits.

Judgment voltage values (Ta = 25°C): 1.05 ±0.10 V, 1.20 ±0.10 V, 1.80 ±0.10 V, 2.40 ±0.10 V

Note:

- When verifying BLD operation, the operation must be verified with an evaluation sample device.

  The OTP (MSM63P180) and development/support tool (EASE63180) do not support BLD.
  (The BLD judgment voltage value of the ML63187, ML63189B, and ML63193 is different from that of the MSM63182, MSM63184B, MSM63188, MSM63182A, MSM63184A, and MSM63188A of the same series.)

18.2 Battery Low Detect Circuit Configuration

The battery low detect circuit consists of a judgment circuit and a judgment voltage select circuit. Figure 18-1 shows the circuit configuration.

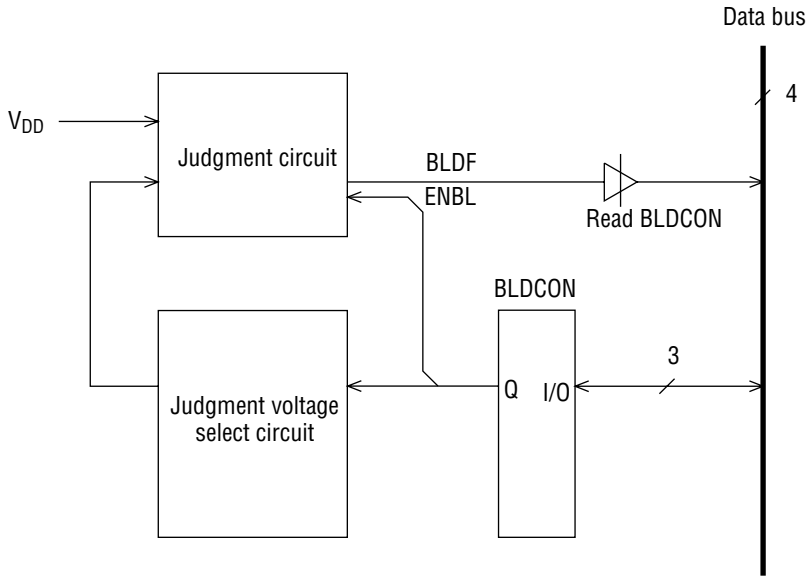


Figure 18-1 Battery Low Detect Circuit

18.3 Judgment Voltage

The value of the judgment voltage is selected by the software by setting the LD1 (bit 1 of BLDCON) and LD0 (bit 0 of BLDCON) bits.

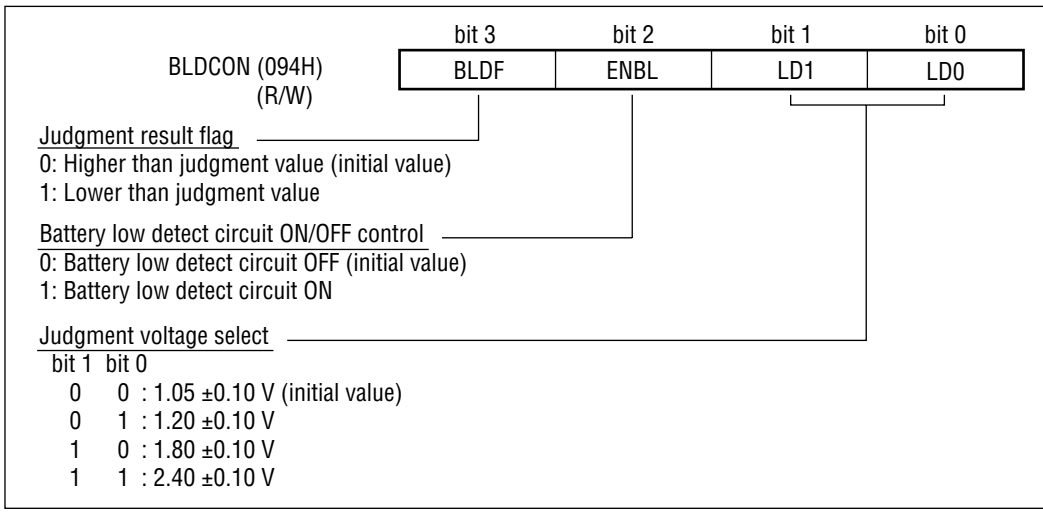
Table 18-1 lists judgment voltage and precision values.

Table 18-1 Judgment Voltage

LD1	LD0	Judgment voltage (V)	Precision (V)	Remarks
0	0	1.05	±0.10	Ta = 25°C
0	1	1.20	±0.10	Ta = 25°C
1	0	1.80	±0.10	Ta = 25°C
1	1	2.40	±0.10	Ta = 25°C

18.4 Battery Low Detect Circuit Register

- Battery low detect control register (BLDCON)
  BLDCON is a 4-bit special function register (SFR) that controls the battery low detect circuit.



bit 3: BLDF

This flag indicates the judgement result of the battery low detect circuit.
This bit is set to "1" when V_{DD} is lower than the judgment voltage selected by LD0 and LD1, and is set to "0" when V_{DD} is higher. This bit is "0" when the BLD circuit stops operation.
This bit is read-only and writes are invalid.

bit 2: ENBL

This bit turns the battery low detect circuit ON or OFF.
When ENBL is set to "1", the battery low detect circuit is ON. When ENBL is set to "0", the battery low detect circuit is OFF.
At system reset, this bit is cleared to "0".

bit 1, 0: LD1, LD0

These bits select the judgment voltage.
At system reset, these bits are cleared to "0".

18.5 Battery Low Detect Circuit Operation

The battery low circuit is turned ON or OFF by ENBL (bit 2 of BLDCON), and outputs to BLDF (bit 3 of BLDCON) the result of a comparison with the judgment voltage.

ENBL is the enable control bit for the battery low detect circuit. Setting ENBL to "1" turns ON the battery low detect circuit. Setting ENBL to "0" turns OFF the battery low detect circuit and BLD current supply drops to zero.

BLDF is the judgment result flag. If BLDF is "1", the power supply voltage is lower than the judgment voltage. If BLDF is "0", the power supply voltage is higher than the judgment voltage. BLDF is valid when ENBL is "1".

The judgment circuit of the battery low detect circuit requires time to become stable. Therefore, after setting ENBL to "1", wait at least 1 ms before reading BLDF. No load should be applied to the power supply voltage during the detection.

Figure 18-2 shows an example operation timing.

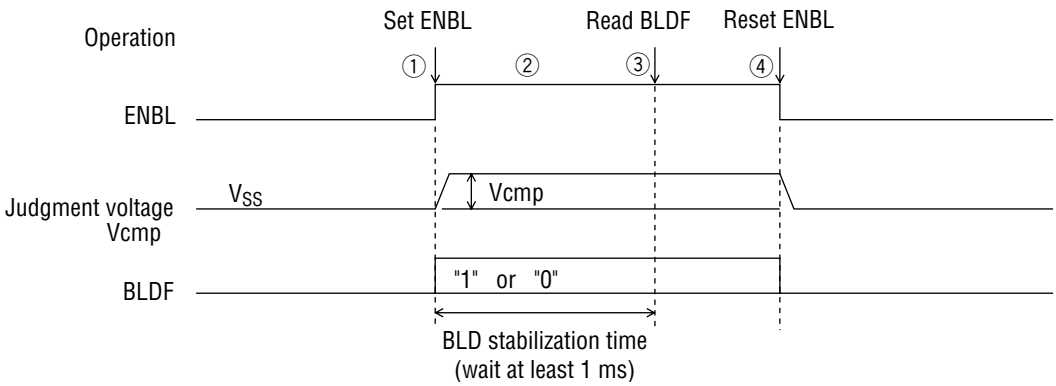


Figure 18-2 Operation Timing Example

Figure 18-2 shows the following operations.

① ENBL is set to "1" to turn ON the BLD.

② Operation starts with no load applied to power supply system and waits for BLD stabilization time interval (at least 1 ms).

③ Judgment result flag (BLDF) is read.

④ ENBL is cleared to "0".

Chapter 19

Backup Circuit (BACKUP)

Chapter 19 Backup Circuit (BACKUP)

19.1 Overview

The ML63187, ML63189B, and ML63193 contain a voltage backup circuit that doubles the power supply voltage. The backup circuit is used when the power supply voltage is 1.8 V or less.

By operating the backup circuit, the CPU can be run even when the power supply voltage is 0.9 V.

The voltage boosted by the backup circuit is supplied as V_{DDH} to the constant voltage circuit and to the high-speed oscillation circuit.

The constant voltage circuit generates V_{DDL} (voltage for internal logic) and V_{DD2} (bias reference voltage for LCDs).

Depending upon whether the backup circuit is ON or OFF, the following voltages are supplied to V_{DDH} (voltage supplied to the constant voltage circuit and high-speed oscillation circuit).

- When backup circuit is ON

  Voltage that is doubled by the backup circuit
- When backup circuit is OFF

  Power supply voltage

Power supply specifications are determined depending upon whether the backup circuit is used.

When backup circuit is used • • • V_{DD} = 0.9 to 2.7 V

When backup circuit is not used • • • V_{DD} = 1.8 to 5.5 V

19.2 Power Supply Circuit Configuration

19.2.1 Power Supply Circuit Configuration When Backup Circuit is Used

Figure 19-1 shows the power supply circuit configuration when the backup circuit is used.

To use the backup circuit, connect a capacitor (C_{b12}) between the CB1 and CB2 pins, or connect a capacitor (C_h) between V_{DDH} and V_{SS}.

In addition, at the beginning of the program, set the backup select bit BACKUP (bit 0 of BUPCON) to "1". The backup select bit is described in a later section.

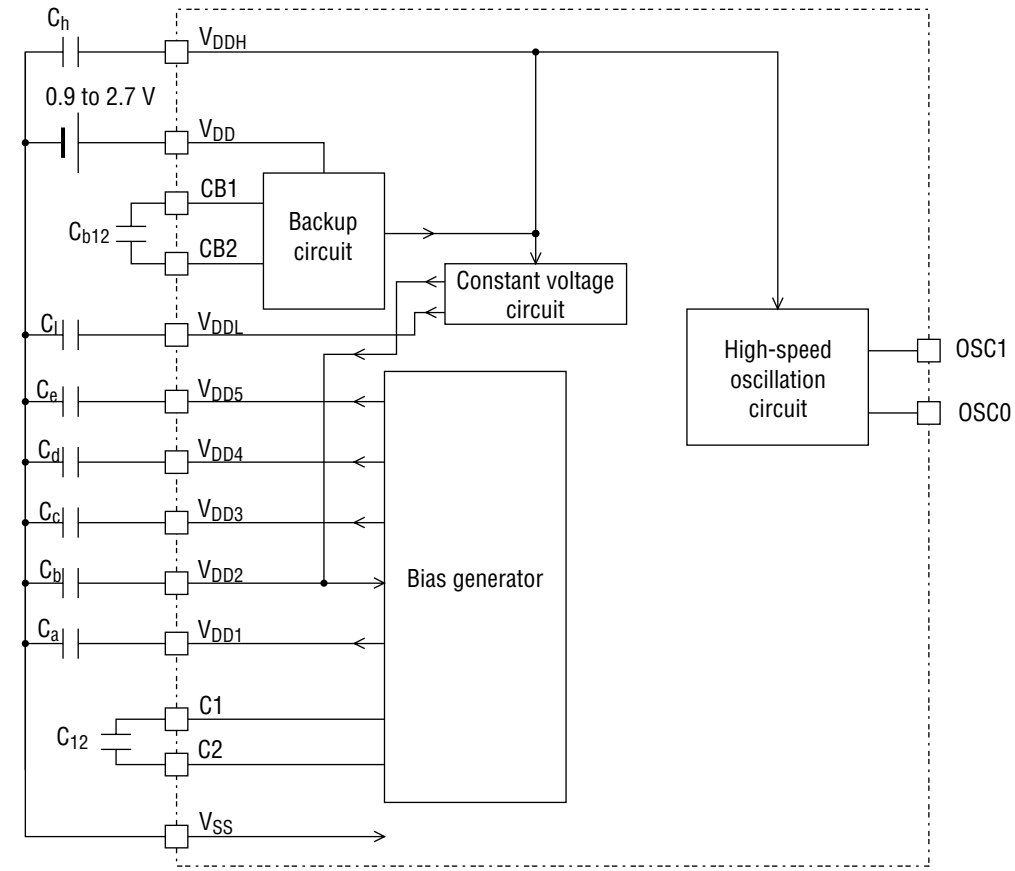


Figure 19-1 Power Supply Circuit Configuration When Backup Circuit is Used

Notes:

- In systems that use the backup circuit, connect an external capacitor (C_{b12}) between the CB1 and CB2 pins.
- The backup circuit cannot be switched ON/OFF once operation has begun. Design peripheral circuits such as external capacitor C_{b12} to meet the ON/OFF specification of the backup circuit.

19.2.2 Power Supply Circuit Configuration When Backup Circuit is Not Used

Figure 19-2 shows the power supply circuit configuration when the backup circuit is not used.

When the backup circuit is not used, leave pins CB1 and CB2 unconnected (open) and connect V_{DDH} to V_{DD}.

In addition, at the beginning of the program, set the later described backup select bit (BACKUP) to "0". (At system reset BACKUP is "1".)

If BACKUP is "1", the backup circuit will operate and supply current will increase.

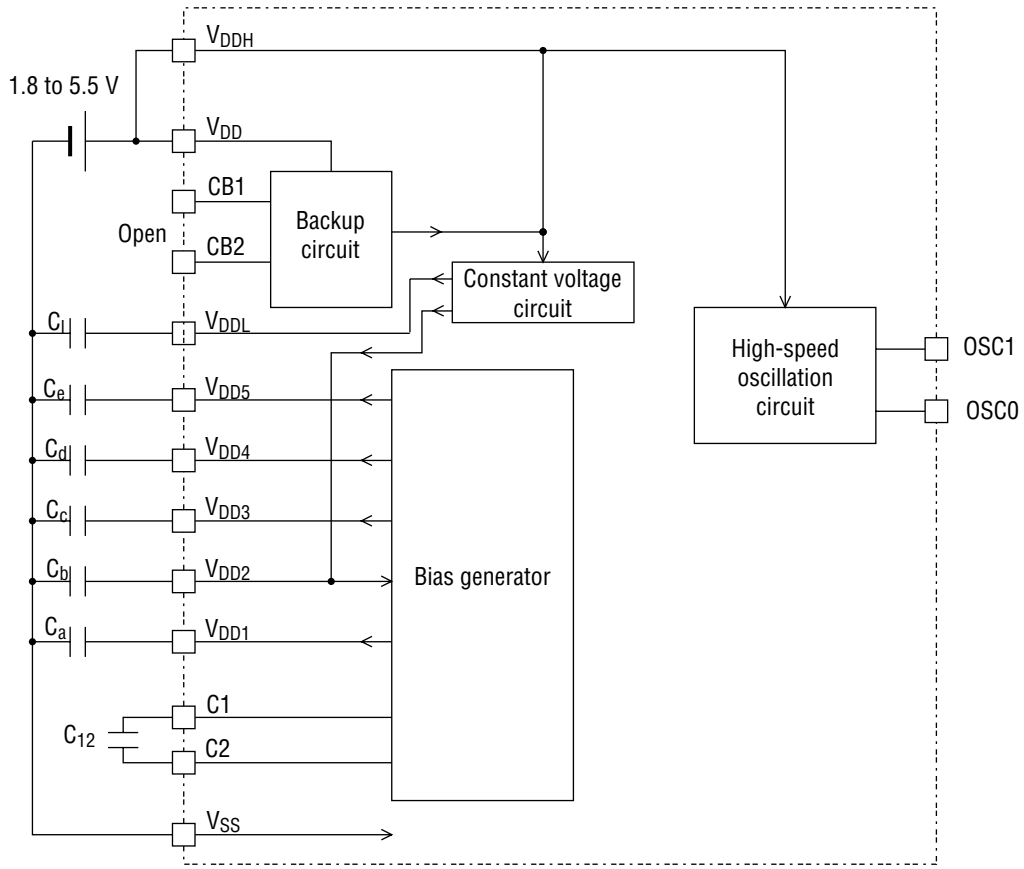


Figure 19-2 Power Supply Circuit Configuration When Backup Circuit is Not Used

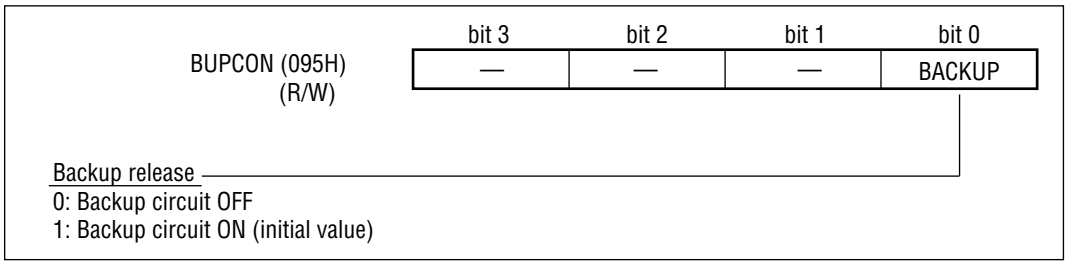
Note:

- The backup circuit cannot be switched ON/OFF once operation has begun. Design peripheral circuits such as external capacitor C_{b12} to meet the ON/OFF specification of the backup circuit.

19.3 Backup Circuit Register

- Backup control register (BUPCON)

BUPCON is a 4-bit special function register (SFR) that sets the backup circuit ON or OFF.



bit 0: BACKUP

At system reset, BACKUP is set to "1" and the backup function is turned ON.

To release (turn OFF) the backup circuit, clear the BACKUP bit to "0" to stop the switching operation for boosting the voltage.

19.4 Power Supply Circuit Operation

When the backup circuit is used, the V_{DDH} output is forcibly switched to the V_{DD} level while the time base counter is reset (RESET0 = "1"). Approximately 62.5 ms after system reset is released, the backup circuit is turned ON, and the V_{DDH} output is boosted to twice the V_{DD} level. When the backup circuit is turned OFF, the V_{DDH} output immediately returns to the V_{DD} level.

When the backup circuit is not used, externally connect the V_{DDH} output to the V_{DD} pin.

The V_{DDL} output is forcibly switched to the V_{DD} level while the time base counter is reset, and changes to approximately 1.5 V immediately after reset is released. If ENOSC (bit 1 of FCON) is set to "1", the V_{DDL} output switches to the V_{DDH} level. If ENOSC is cleared to "0", the V_{DDL} output returns to approximately 1.5 V.

The V_{DD2} output (bias reference voltage for LCDs) is forcibly switched to the V_{DD} level while the time base counter is reset, and outputs the voltage (1.8 to 2.4 V) selected by the display control register (DSPCNT) after reset is released.

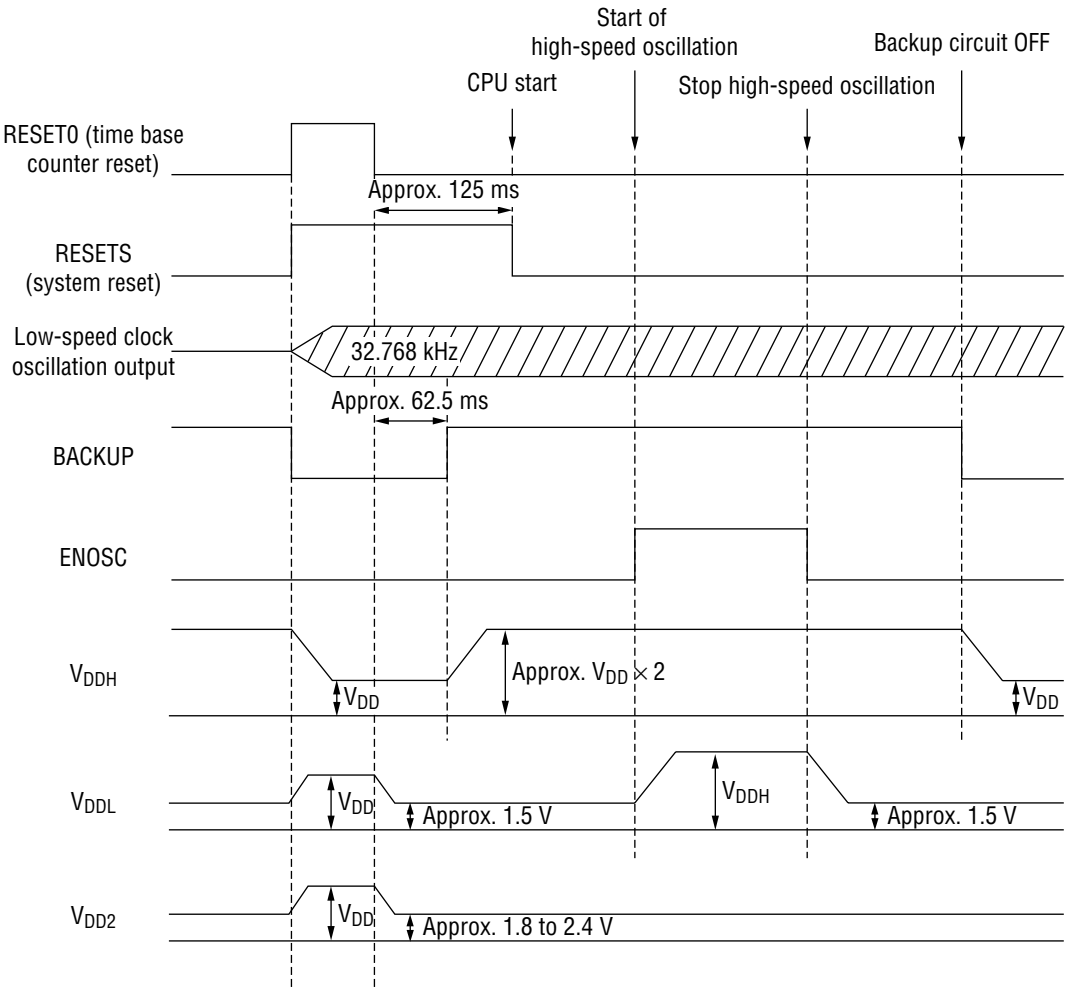


Figure 19-3 Power Supply Circuit Operation Waveforms

Appendixes

Appendix A List of Special Function Registers

The Special Function Registers of the ML63187, ML63189B, and ML63193 are listed in Table A. The solid black circles (●) indicate that the device is provided with the particular register. The solid lines (—) indicate that the device is not provided with the particular register.

Table A Special Function Register List

Register name	Symbol	Address	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset	ML 63187	ML 63189B	ML 63193
Port 0 data register	P0D	000H	P03	P02	P01	P00	R	Undefined	—	●	●
Reserved		001H to 008H									
Port 9 data register	P9D	009H	P93	P92	P91	P90	R/W	0H	—	●	●
Port A data register	PAD	00AH	PA3	PA2	PA1	PA0	R/W	0H			
Port B data register	PBD	00BH	PB3	PB2	PB1	PB0	R/W	0H	●	●	●
Port C data register	PCD	00CH	PC3	PC2	PC1	PC0	R/W	0H	—	—	●
Reserved		00DH									
Port E data register	PED	00EH	PE3	PE2	PE1	PE0	R/W	0H	●	●	●
Reserved		00FH									
Port 0 control register 0	P0CON0	010H	P03MD	P02MD	P01MD	P00MD	R/W	0H	—	●	●
Port 0 control register 1	P0CON1	011H	—	—	P0PUD	P0F	R/W	0CH			
Port 0 interrupt enable register	P0IE	012H	P03IE	P02IE	P01IE	P00IE	R/W	0H			
Reserved		013H to 026H									
Port 9 control register 0	P9CON0	027H	P91MD1	P91MD0	P90MD1	P90MD0	R/W	0H	—	●	●
Port 9 control register 1	P9CON1	028H	P93MD1	P93MD0	P92MD1	P92MD0	R/W	0H			
Port 9 direction register	P9DIR	029H	P93DIR	P92DIR	P91DIR	P90DIR	R/W	0H			
Port A control register 0	PACON0	02AH	PA1MD1	PA1MD0	PA0MD1	PA0MD0	R/W	0H			
Port A control register 1	PACON1	02BH	PA3MD1	PA3MD0	PA2MD1	PA2MD0	R/W	0H			
Port A direction register	PADIR	02CH	PA3DIR	PA2DIR	PA1DIR	PA0DIR	R/W	0H			
Reserved		02DH									
Port B control register 0	PBCON0	02EH	PB1MD1	PB1MD0	PB0MD1	PB0MD0	R/W	0H	●	●	●
Port B control register 1	PBCON1	02FH	PB3MD1	PB3MD0	PB2MD1	PB2MD0	R/W	0H			
Port B direction register	PBDIR	030H	PB3DIR	PB2DIR	PB1DIR	PB0DIR	R/W	0H			
Port B interrupt enable register	PBIE	031H	PB3IE	PB2IE	PB1IE	PB0IE	R/W	0H			
Port B mode register	PBMOD	032H	PBF	—	PB1MOD	PB0MOD	R/W	4H			
Port C control register 0	PCCON0	033H	PC1MD1	PC1MD0	PC0MD1	PC0MD0	R/W	0H	—	—	●
Port C control register 1	PCCON1	034H	PC3MD1	PC3MD0	PC2MD1	PC2MD0	R/W	0H			
Port C direction register	PCDIR	035H	PC3DIR	PC2DIR	PC1DIR	PC0DIR	R/W	0H			
Port C interrupt enable register	PCIE	036H	PC3IE	PC2IE	PC1IE	PC0IE	R/W	0H			
Port C mode register 0	PCMOD0	037H	—	—	—	PCF	R/W	0EH			
Port C mode register 1	PCMOD1	038H	PC3MOD	PC2MOD	PC1MOD	PC0MOD	R/W	0H			

Table A Special Function Register List (continued)

Register name	Symbol	Address	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset	ML 63187	ML 63189B	ML 63193
Reserved		039H to 03CH									
Port E control register 0	PECON0	03DH	PE1MD1	PE1MD0	PE0MD1	PE0MD0	R/W	0H	●	●	●
Port E control register 1	PECON1	03EH	PE3MD1	PE3MD0	PE2MD1	PE2MD0	R/W	0H			
Port B direction register	PEDIR	03FH	PE3DIR	PE2DIR	PE1DIR	PE0DIR	R/W	0H			
Port E mode register	PEMOD	040H	PEF	PE2MOD	PE1MOD	PE0MOD	R/W	0H			
Reserved		041H to 04FH									
Interrupt enable register 0	IE0	050H	—	EXI0	EMD	—	R/W	9H	●	●	—
			EXI1	EXI0	EMD	—		1H	—	—	●
Interrupt enable register 1	IE1	051H	—	—	—	EXI2	R/W	0EH	●	—	—
			EXI5	—	—	EXI2		6H	—	●	●
Interrupt enable register 2	IE2	052H	ETM3	ETM2	ETM1	ETM0	R/W	0H	●	●	●
Interrupt enable register 3	IE3	053H	E10Hz	ESFT	—	—	R/W	3H	●	●	—
			E10Hz	ESFT	EST	ESR		0H	—	—	●
Interrupt enable register 4	IE4	054H	E2Hz	E4Hz	E16Hz	E32Hz	R/W	0H	●	●	●
Interrupt request register 0	IRQ0	055H	—	QXI0	QMD	QWDT	R/W	8H	●	●	—
			QXI1	QXI0	QMD	QWDT		0H	—	—	●
Interrupt request register 1	IRQ1	056H	—	—	—	QXI2	R/W	0EH	●	—	—
			QXI5	—	—	QXI2		6H	—	●	●
Interrupt request register 2	IRQ2	057H	QTM3	QTM2	QTM1	QTM0	R/W	0H	●	●	●
Interrupt request register 3	IRQ3	058H	Q10Hz	QSFT	—	—	R/W	3H	●	●	—
			Q10Hz	QSFT	QST	QSR		0H	—	—	●
Interrupt request register 4	IRQ4	059H	Q2Hz	Q4Hz	Q16Hz	Q32Hz	R/W	0H	●	●	●
Reserved		05AH to 05FH									
Time base counter register 0	TBCR0	060H	16Hz	32Hz	64Hz	128Hz	R/W	0H	●	●	●
Time base counter register 1	TBCR1	061H	1Hz	2Hz	4Hz	8Hz	R/W	0H			
Frequency control register	FCON	062H	—	OSCSEL	ENOSC	CPUCLK	R/W	8H			
Reserved		063H									
100 Hz timer counter register	T100CR	064H	100C3	100C2	100C1	100C0	R/W	Undefined	●	●	●
10 Hz timer counter register	T10CR	065H	10C3	10C2	10C1	10C0	R/W	0H			
100 Hz timer counter control register	T100CON	066H	—	—	—	ECNT	R/W	0EH			
Reserved		067H									
Timer 0 data register L	TM0DL	068H	T0D3	T0D2	T0D1	T0D0	R/W	0H	●	●	●
Timer 0 data register H	TM0DH	069H	T0D7	T0D6	T0D5	T0D4	R/W	0H			
Timer 1 data register L	TM1DL	06AH	T1D3	T1D2	T1D1	T1D0	R/W	0H			
Timer 1 data register H	TM1DH	06BH	T1D7	T1D6	T1D5	T1D4	R/W	0H			

Table A Special Function Register List (continued)

Register name	Symbol	Address	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset	ML 63187	ML 63189B	ML 63193
Timer 0 counter register L	TM0CL	06CH	T0C3	T0C2	T0C1	T0C0	R/W	0H			
Timer 0 counter register H	TM0CH	06DH	T0C7	T0C6	T0C5	T0C4	R/W	0H			
Timer 1 counter register L	TM1CL	06EH	T1C3	T1C2	T1C1	T1C0	R/W	0H			
Timer 1 counter register H	TM1CH	06FH	T1C7	T1C6	T1C5	T1C4	R/W	0H			
Timer 0 control register 0	TM0CON0	070H	—	FMEAS0	TM0ECAP	TM0RUN	R/W	8H			
Timer 0 control register 1	TM0CON1	071H	—	—	TM0CL1	TM0CL0	R/W	0CH			
Timer 1 control register 0	TM1CON0	072H	—	—	TM1ECAP	TM1RUN	R/W	0CH			
Timer 1 control register 1	TM1CON1	073H	—	—	TM1CL1	TM1CL0	R/W	0CH			
Timer 0 status register	TM0STAT	074H	—	—	TM0CAP	TM0OVF	R	0CH			
Timer 1 status register	TM1STAT	075H	—	—	TM1CAP	TM1OVF	R	0CH			
Timer 2 data register L	TM2DL	076H	T2D3	T2D2	T2D1	T2D0	R/W	0H			
Timer 2 data register H	TM2DH	077H	T2D7	T2D6	T2D5	T2D4	R/W	0H			
Timer 3 data register L	TM3DL	078H	T3D3	T3D2	T3D1	T3D0	R/W	0H	●	●	●
Timer 3 data register H	TM3DH	079H	T3D7	T3D6	T3D5	T3D4	R/W	0H			
Timer 2 counter register L	TM2CL	07AH	T2C3	T2C2	T2C1	T2C0	R/W	0H			
Timer 2 counter register H	TM2CH	07BH	T2C7	T2C6	T2C5	T2C4	R/W	0H			
Timer 3 counter register L	TM3CL	07CH	T3C3	T3C2	T3C1	T3C0	R/W	0H			
Timer 3 counter register H	TM3CH	07DH	T3C7	T3C6	T3C5	T3C4	R/W	0H			
Timer 2 control register 0	TM2CON0	07EH	—	FMEAS2	—	TM2RUN	R/W	0AH			
Timer 2 control register 1	TM2CON1	07FH	—	—	TM2CL1	TM2CL0	R/W	0CH			
Timer 3 control register 0	TM3CON0	080H	—	—	—	TM3RUN	R/W	0EH			
Timer 3 control register 1	TM3CON1	081H	—	—	TM3CL1	TM3CL0	R/W	0CH			
Timer 2 status register	TM2STAT	082H	—	—	—	TM2OVF	R	0EH			
Timer 3 status register	TM3STAT	083H	—	—	—	TM3OVF	R	0EH			
Reserved		084H and 085H									
Multiplication/division condition register	MDCR	086H	OV	EF	DIVS	MULS	R/W	0H			
C register L	CRL	087H	CR3	CR2	CR1	CR0	R/W	0H			
C register H	CRH	088H	CR7	CR6	CR5	CR4	R/W	0H			
D register L	DRL	089H	DR3	DR2	DR1	DR0	R/W	0H			
D register H	DRH	08AH	DR7	DR6	DR5	DR4	R/W	0H	—	—	●
E register L	ERL	08BH	ER3	ER2	ER1	ER0	R/W	0H			
E register H	ERH	08CH	ER7	ER6	ER5	ER4	R/W	0H			
F register L	FRL	08DH	FR3	FR2	FR1	FR0	R/W	0H			
F register H	FRH	08EH	FR7	FR6	FR5	FR4	R/W	0H			
Reserved		08FH									
Display control register 0	DSPCON0	090H	BISEL	PDWN	ALLON	LCDON	R/W	0H			
Display control register 1	DSPCON1	091H	DT3	DT2	DT1	DT0	R/W	0H	●	●	●
Display contrast register	DSPCNT	092H	CN3	CN2	CN1	CN0	R/W	0H			
Reserved		093H									

Table A Special Function Register List (continued)

Register name	Symbol	Address	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset	ML 63187	ML 63189B	ML 63193
Battery low detect control register	BLDCON	094H	BLDF	ENBL	LD1	LD0	R/W	0H	●	●	●
Backup control register	BUPCON	095H	—	—	—	BACKUP	R/W	0FH	●	●	●
Tempo register	TEMPO	096H	TMP3	TMP2	TMP1	TMP0	R/W	0H	●	●	●
Melody driver control register	MDCON	097H	MSF	EMBD	MBM1	MBM0	R/W	0H			
Reserved		098H to 09EH									
Watchdog timer control register	WDTCON	09FH	d3	d2	d1	d0	W	—	●	●	●
Shift register L	SFTRL	0A0H	SD3	SD2	SD1	SD0	R/W	0H			
Shift register H	SFTRH	0A1H	SD7	SD6	SD5	SD4	R/W	0H			
Shift register control register 0	SFTCON0	0A2H	—	SDIR	SELCK1	SELCK0	R/W	8H			
Shift register control register 1	SFTCON1	0A3H	—	—	—	ENTR	R/W	0EH			
Serial port send buffer L	STBUFL	0A4H	TB3	TB2	TB1	TB0	R/W	0H	—	—	●
Serial port send buffer H	STBUFH	0A5H	TB7	TB6	TB5	TB4	R/W	0H			
Serial port send control register 0	STCON0	0A6H	STSTB	STL1	STL0	STMOD	R/W	0H			
Serial port send control register 1	STCON1	0A7H	STLMB	STPOE	STPEN	STCLK	R/W	0H			
Serial port receive buffer L	SRBUFL	0A8H	RB3	RB2	RB1	RB0	R	0H			
Serial port receive buffer H	SRBUFH	0A9H	RB7	RB6	RB5	RB4	R	0H			
Serial port receive control register 0	SRCON0	0AAH	SREN	SRL1	SRL0	SRMOD	R/W	0H			
Serial port receive control register 1	SRCON1	0ABH	SRLMB	SRPOE	SRPEN	SRCLK	R/W	0H			
Serial port receive baud rate setting register	SRBRT	0ACH	—	—	BRT1	BRT0	R/W	0CH			
Serial port status register	SSTAT	0ADH	BFULL	PERR	0ERR	FERR	R	0H			
Reserved		0AEH to 0F1H									
RA register 0	RA0	0F2H	a3	a2	a1	a0	R/W	0H	●	●	●
RA register 1	RA1	0F3H	a7	a6	a5	a4	R/W	0H			
RA register 2	RA2	0F4H	a11	a10	a9	a8	R/W	0H			
RA register 3	RA3	0F5H	a15	a14	a13	a12	R/W	0H			
Register stack pointer	RSP	0F6H	rsp3	rsp2	rsp1	rsp0	R/W	0H			
Stack pointer	SP	0F7H	sp3	sp2	sp1	sp0	R	0H			
Reserved		0F8H									
Y register	Y	0F9H	y3	y2	y1	y0	R/W	0H	●	●	●
X register	X	0FAH	x3	x2	x1	x0	R/W	0H			
L register	L	0FBH	l3	l2	l1	l0	R/W	0H			
H register	H	0FCH	h3	h2	h1	h0	R/W	0H			
Current bank register	CBR	0FDH	c3	c2	c1	c0	R/W	0H			
Extra bank register	EBR	0FEH	e3	e2	e1	e0	R/W	0H			
Master interrupt enable flag register	MIEF	0FFH	—	—	—	MIE	R	0EH			

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset	ML 63187	ML 63189B	ML 63193
Display register 0	DSPR0	100H	SEG0	COM4	COM3	COM2	COM1	R/W	Undefined	●	●	●
Display register 1	DSPR1	101H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 2	DSPR2	102H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 3	DSPR3	103H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 4	DSPR4	104H	SEG1	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 5	DSPR5	105H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 6	DSPR6	106H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 7	DSPR7	107H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 8	DSPR8	108H	SEG2	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 9	DSPR9	109H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 10	DSPR10	10AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 11	DSPR11	10BH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 12	DSPR12	10CH	SEG3	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 13	DSPR13	10DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 14	DSPR14	10EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 15	DSPR15	10FH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 16	DSPR16	110H	SEG4	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 17	DSPR17	111H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 18	DSPR18	112H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 19	DSPR19	113H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 20	DSPR20	114H	SEG5	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 21	DSPR21	115H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 22	DSPR22	116H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 23	DSPR23	117H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 24	DSPR24	118H	SEG6	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 25	DSPR25	119H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 26	DSPR26	11AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 27	DSPR27	11BH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 28	DSPR28	11CH	SEG7	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 29	DSPR29	11DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 30	DSPR30	11EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 31	DSPR31	11FH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 32	DSPR32	120H	SEG8	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 33	DSPR33	121H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 34	DSPR34	122H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 35	DSPR35	123H		COM16	COM15	COM14	COM13	R/W	Undefined			

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset	ML 63187	ML 63189B	ML 63193
Display register 36	DSPR36	124H	SEG9	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 37	DSPR37	125H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 38	DSPR38	126H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 39	DSPR39	127H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 40	DSPR40	128H	SEG10	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 41	DSPR41	129H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 42	DSPR42	12AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 43	DSPR43	12BH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 44	DSPR44	12CH	SEG11	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 45	DSPR45	12DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 46	DSPR46	12EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 47	DSPR47	12FH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 48	DSPR48	130H	SEG12	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 49	DSPR49	131H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 50	DSPR50	132H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 51	DSPR51	133H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 52	DSPR52	134H	SEG13	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 53	DSPR53	135H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 54	DSPR54	136H		COM12	COM11	COM10	COM9	R/W	Undefined	●	●	●
Display register 55	DSPR55	137H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 56	DSPR56	138H	SEG14	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 57	DSPR57	139H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 58	DSPR58	13AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 59	DSPR59	13BH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 60	DSPR60	13CH	SEG15	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 61	DSPR61	13DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 62	DSPR62	13EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 63	DSPR63	13FH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 64	DSPR64	140H	SEG16	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 65	DSPR65	141H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 66	DSPR66	142H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 67	DSPR67	143H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 68	DSPR68	144H	SEG17	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 69	DSPR69	145H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 70	DSPR70	146H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 71	DSPR71	147H		COM16	COM15	COM14	COM13	R/W	Undefined			

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset	ML 63187	ML 63189B	ML 63193
Display register 72	DSPR72	148H	SEG18	COM4	COM3	COM2	COM1	R/W	Undefined	●	●	●
Display register 73	DSPR73	149H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 74	DSPR74	14AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 75	DSPR75	14BH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 76	DSPR76	14CH	SEG19	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 77	DSPR77	14DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 78	DSPR78	14EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 79	DSPR79	14FH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 80	DSPR80	150H	SEG20	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 81	DSPR81	151H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 82	DSPR82	152H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 83	DSPR83	153H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 84	DSPR84	154H	SEG21	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 85	DSPR85	155H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 86	DSPR86	156H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 87	DSPR87	157H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 88	DSPR88	158H	SEG22	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 89	DSPR89	159H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 90	DSPR90	15AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 91	DSPR91	15BH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 92	DSPR92	15CH	SEG23	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 93	DSPR93	15DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 94	DSPR94	15EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 95	DSPR95	15FH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 96	DSPR96	160H	SEG24	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 97	DSPR97	161H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 98	DSPR98	162H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 99	DSPR99	163H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 100	DSPR100	164H	SEG25	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 101	DSPR101	165H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 102	DSPR102	166H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 103	DSPR103	167H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 104	DSPR104	168H	SEG26	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 105	DSPR105	169H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 106	DSPR106	16AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 107	DSPR107	16BH		COM16	COM15	COM14	COM13	R/W	Undefined			

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset	ML 63187	ML 63189B	ML 63193
Display register 108	DSPR108	16CH	SEG27	COM4	COM3	COM2	COM1	R/W	Undefined	●	●	●
Display register 109	DSPR109	16DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 110	DSPR110	16EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 111	DSPR111	16FH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 112	DSPR112	170H	SEG28	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 113	DSPR113	171H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 114	DSPR114	172H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 115	DSPR115	173H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 116	DSPR116	174H	SEG29	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 117	DSPR117	175H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 118	DSPR118	176H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 119	DSPR119	177H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 120	DSPR120	178H	SEG30	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 121	DSPR121	179H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 122	DSPR122	17AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 123	DSPR123	17BH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 124	DSPR124	17CH	SEG31	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 125	DSPR125	17DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 126	DSPR126	17EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 127	DSPR127	17FH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 128	DSPR128	180H	SEG32	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 129	DSPR129	181H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 130	DSPR130	182H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 131	DSPR131	183H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 132	DSPR132	184H	SEG33	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 133	DSPR133	185H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 134	DSPR134	186H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 135	DSPR135	187H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 136	DSPR136	188H	SEG34	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 137	DSPR137	189H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 138	DSPR138	18AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 139	DSPR139	18BH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 140	DSPR140	18CH	SEG35	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 141	DSPR141	18DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 142	DSPR142	18EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 143	DSPR143	18FH		COM16	COM15	COM14	COM13	R/W	Undefined			

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset	ML 63187	ML 63189B	ML 63193
Display register 144	DSPR144	190H	SEG36	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 145	DSPR145	191H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 146	DSPR146	192H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 147	DSPR147	193H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 148	DSPR148	194H	SEG37	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 149	DSPR149	195H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 150	DSPR150	196H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 151	DSPR151	197H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 152	DSPR152	198H	SEG38	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 153	DSPR153	199H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 154	DSPR154	19AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 155	DSPR155	19BH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 156	DSPR156	19CH	SEG39	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 157	DSPR157	19DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 158	DSPR158	19EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 159	DSPR159	19FH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 160	DSPR160	1A0H	SEG40	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 161	DSPR161	1A1H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 162	DSPR162	1A2H		COM12	COM11	COM10	COM9	R/W	Undefined	●	●	●
Display register 163	DSPR163	1A3H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 164	DSPR164	1A4H	SEG41	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 165	DSPR165	1A5H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 166	DSPR166	1A6H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 167	DSPR167	1A7H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 168	DSPR168	1A8H	SEG42	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 169	DSPR169	1A9H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 170	DSPR170	1AAH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 171	DSPR171	1ABH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 172	DSPR172	1ACH	SEG43	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 173	DSPR173	1ADH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 174	DSPR174	1AEH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 175	DSPR175	1AFH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 176	DSPR176	1B0H	SEG44	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 177	DSPR177	1B1H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 178	DSPR178	1B2H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 179	DSPR179	1B3H		COM16	COM15	COM14	COM13	R/W	Undefined			

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset	ML 63187	ML 63189B	ML 63193
Display register 180	DSPR180	1B4H	SEG45	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 181	DSPR181	1B5H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 182	DSPR182	1B6H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 183	DSPR183	1B7H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 184	DSPR184	1B8H	SEG46	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 185	DSPR185	1B9H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 186	DSPR186	1BAH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 187	DSPR187	1BBH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 188	DSPR188	1BCH	SEG47	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 189	DSPR189	1BDH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 190	DSPR190	1BEH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 191	DSPR191	1BFH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 192	DSPR192	1C0H	SEG48	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 193	DSPR193	1C1H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 194	DSPR194	1C2H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 195	DSPR195	1C3H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 196	DSPR196	1C4H	SEG49	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 197	DSPR197	1C5H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 198	DSPR198	1C6H		COM12	COM11	COM10	COM9	R/W	Undefined	●	●	●
Display register 199	DSPR199	1C7H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 200	DSPR200	1C8H	SEG50	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 201	DSPR201	1C9H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 202	DSPR202	1CAH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 203	DSPR203	1CBH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 204	DSPR204	1CCH	SEG51	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 205	DSPR205	1CDH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 206	DSPR206	1CEH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 207	DSPR207	1CFH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 208	DSPR208	1D0H	SEG52	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 209	DSPR209	1D1H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 210	DSPR210	1D2H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 211	DSPR211	1D3H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 212	DSPR212	1D4H	SEG53	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 213	DSPR213	1D5H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 214	DSPR214	1D6H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 215	DSPR215	1D7H		COM16	COM15	COM14	COM13	R/W	Undefined			

Table A Special Function Register List (continued)

Register name	Symbol	Address	Segment	bit 3	bit 2	bit 1	bit 0	R/W	Initial value at system reset	ML 63187	ML 63189B	ML 63193
Display register 216	DSPR216	1D8H	SEG54	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 217	DSPR217	1D9H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 218	DSPR218	1DAH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 219	DSPR219	1DBH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 220	DSPR220	1DCH	SEG55	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 221	DSPR221	1DDH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 222	DSPR222	1DEH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 223	DSPR223	1DFH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 224	DSPR224	1E0H	SEG56	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 225	DSPR225	1E1H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 226	DSPR226	1E2H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 227	DSPR227	1E3H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 228	DSPR228	1E4H	SEG57	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 229	DSPR229	1E5H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 230	DSPR230	1E6H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 231	DSPR231	1E7H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 232	DSPR232	1E8H	SEG58	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 233	DSPR233	1E9H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 234	DSPR234	1EAH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 235	DSPR235	1EBH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 236	DSPR236	1ECH	SEG59	COM4	COM3	COM2	COM1	R/W	Undefined	●	●	●
Display register 237	DSPR237	1EDH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 238	DSPR238	1EEH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 239	DSPR239	1EFH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 240	DSPR240	1F0H	SEG60	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 241	DSPR241	1F1H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 242	DSPR242	1F2H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 243	DSPR243	1F3H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 244	DSPR244	1F4H	SEG61	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 245	DSPR245	1F5H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 246	DSPR246	1F6H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 247	DSPR247	1F7H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 248	DSPR248	1F8H	SEG62	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 249	DSPR249	1F9H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 250	DSPR250	1FAH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 251	DSPR251	1FBH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 252	DSPR252	1FCH	SEG63	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 253	DSPR253	1FDH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 254	DSPR254	1FEH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 255	DSPR255	1FFH		COM16	COM15	COM14	COM13	R/W	Undefined			

Appendix B Package Dimensions

ML63187-xxxGA
ML63189B-xxxGA

(Unit : mm)

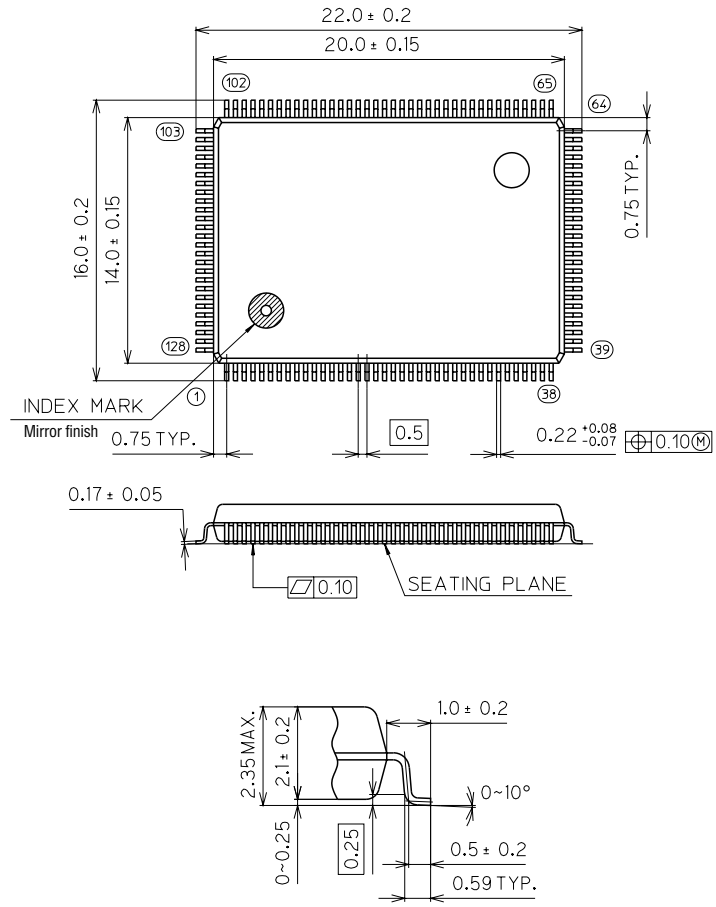


Figure B-1 128-Pin QFP (QFP128-P-1420-0.50-K)

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature, and times).

ML63193-xxxTC

(Unit : mm)

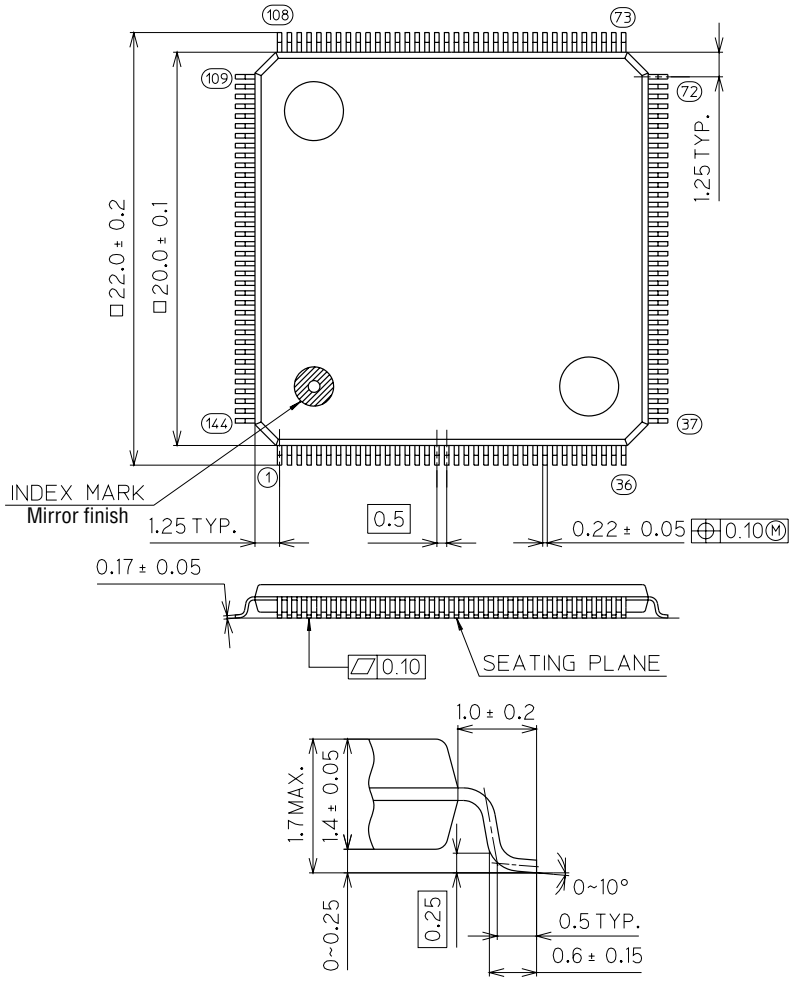


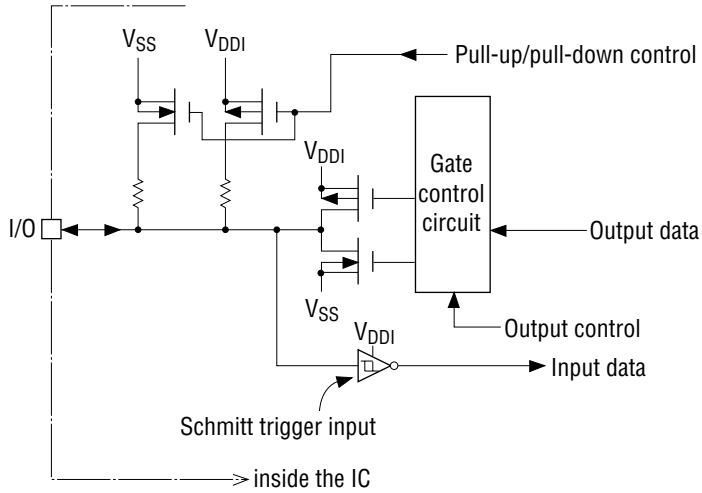
Figure B-2 144-Pin LQFP (LQFP144-P-2020-0.50-K)

Notes for Mounting the Surface Mount Type Package

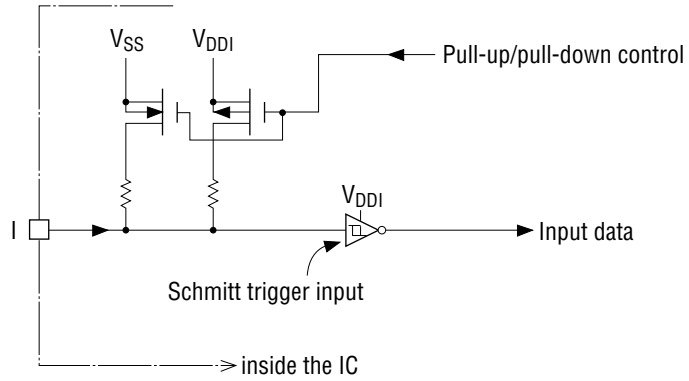
The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature, and times).

Appendix C Input/Output Circuit Configuration

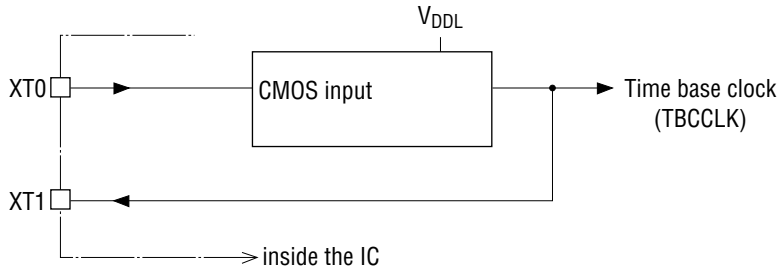
(1) I/O Port (P9.0–P9.3, PA.0–PA.3, PB.0–PB.3, PC.0–PC.3, PE.0–PE.3)



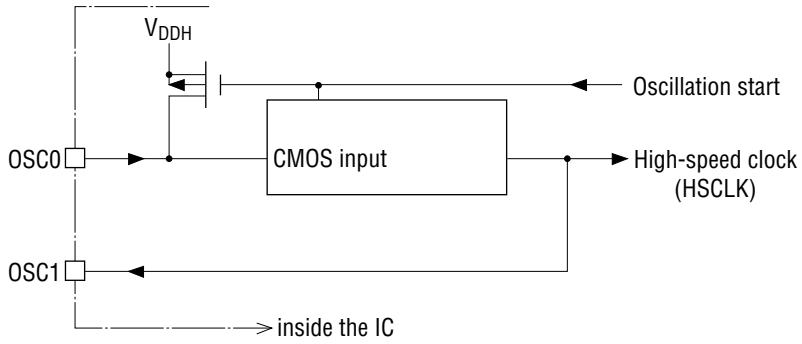
(2) Input Port (P0.0–P0.3)



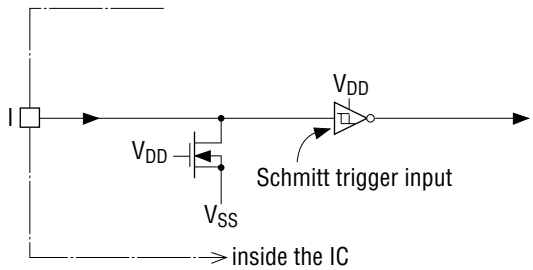
(3) Low-Speed Oscillation Circuit



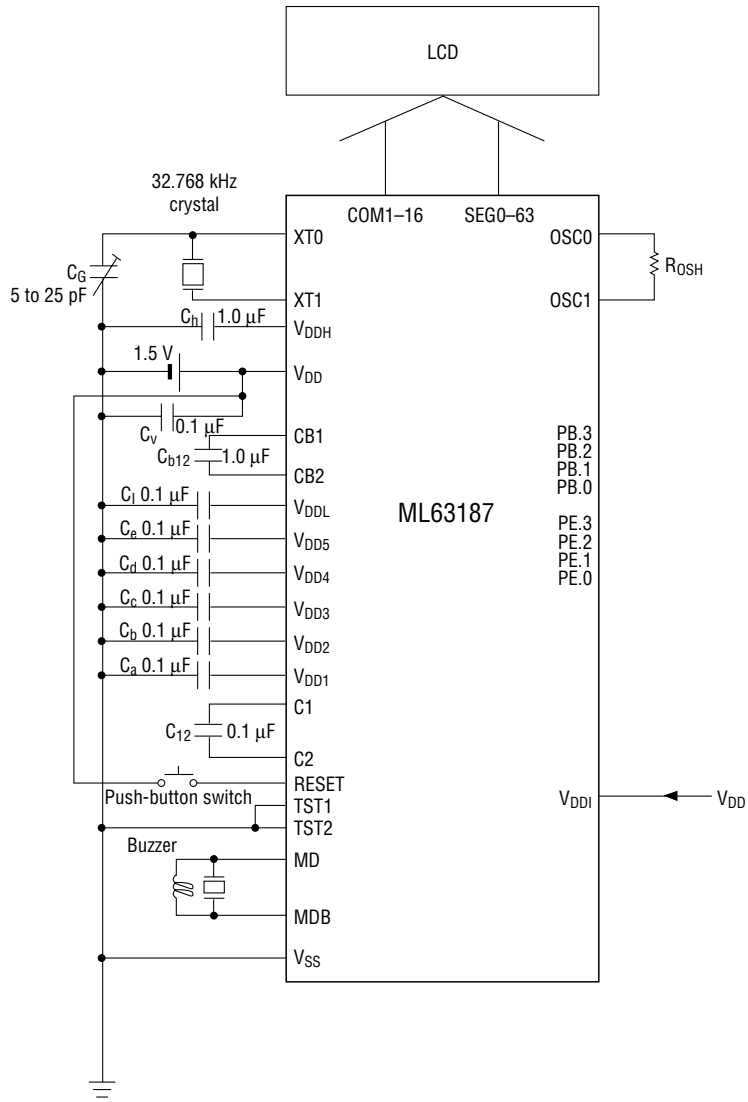
(4) High-Speed Oscillation Circuit



(5) RESET, TST1, and TST2 Inputs



Appendix D Peripheral Circuit Examples

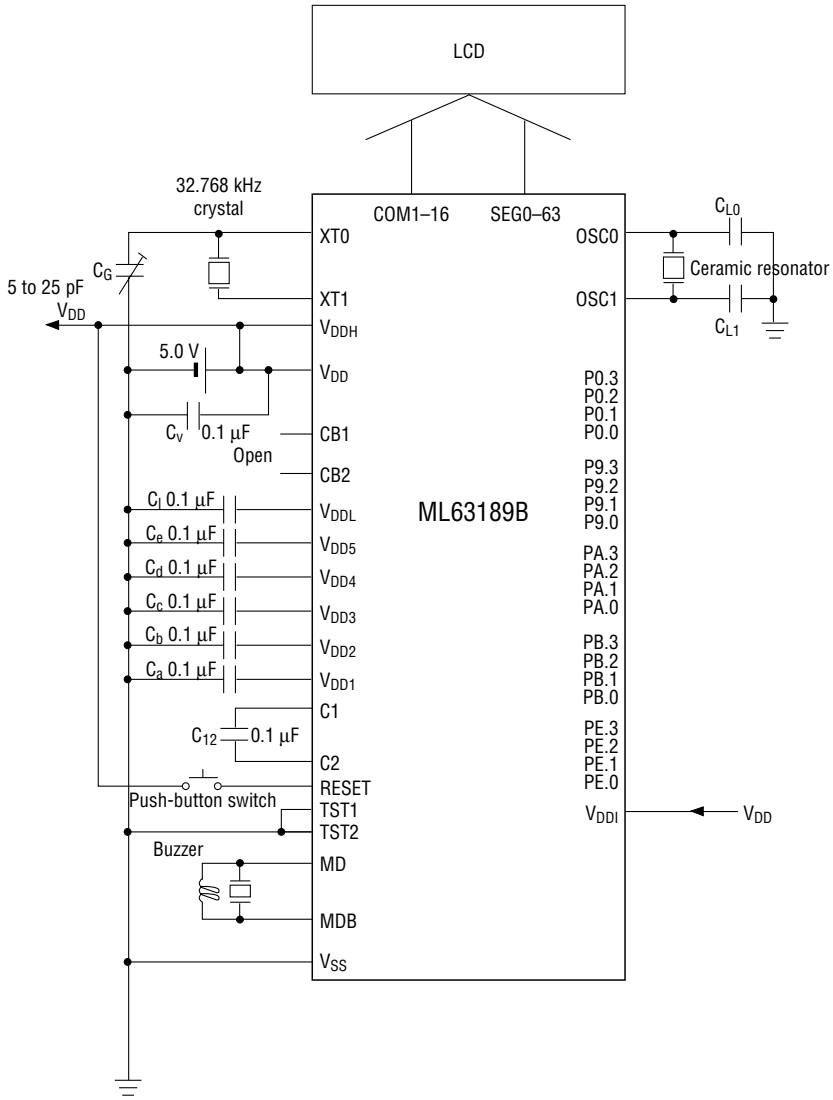


- Crystal oscillation is selected by mask option for low-speed oscillation.
- RC oscillation is selected for high-speed oscillation.
- The power supply for the ports is shared with V_{DD}.
- C_V is an IC power supply bypass capacitor.
- Capacitance values for C_a, C_b, C_c, C_d, C_e, C_l, C_{b12}, C_{12}, C_h, and C_G are only for reference.

Figure D-1 Peripheral Circuit Example with Power Supply Backup

Note:

V_{DDI} is the power supply pin for input and I/O ports.
V_{DDI} must be connected to the positive power supply pin (V_{DD}) of the chip or the power supply pin of the external equipment.

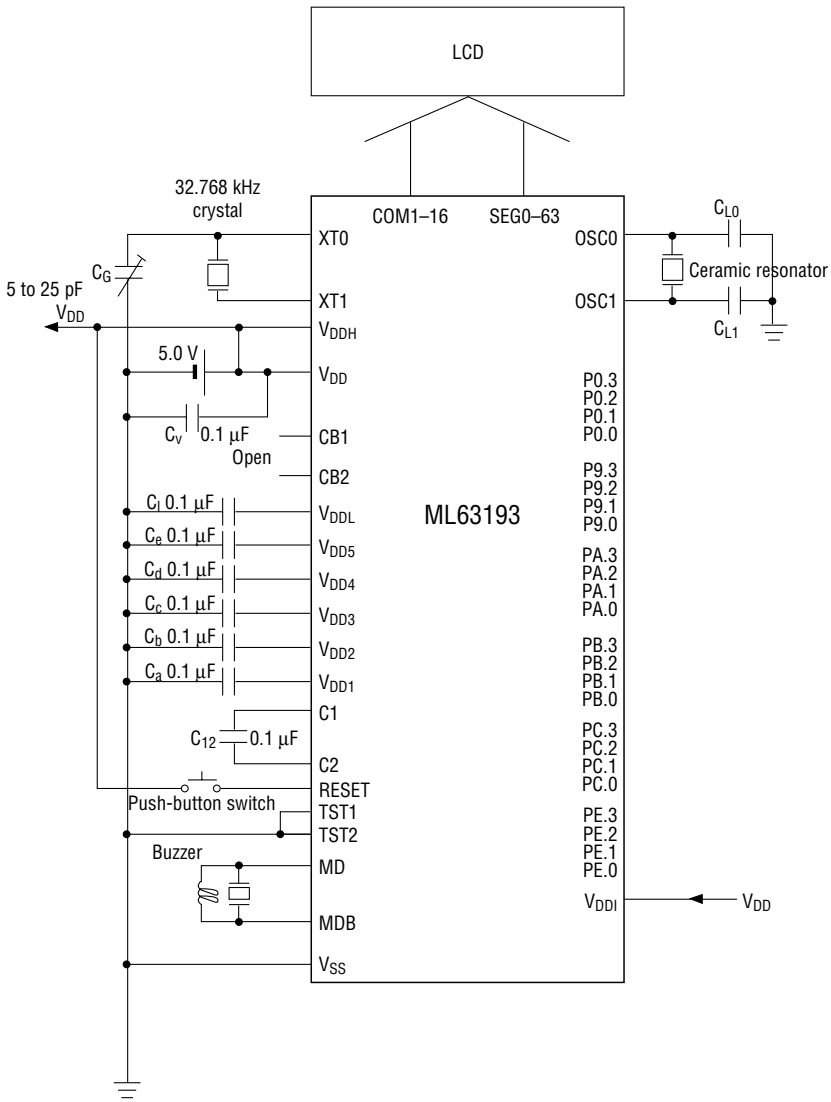


- Crystal oscillation is selected by mask option for low-speed oscillation.
- Ceramic oscillation is selected for high-speed oscillation.
- The power supply for the ports is shared with V_{DD}.
- C_V is an IC power supply bypass capacitor.
- Capacitance values for C_a, C_b, C_c, C_d, C_e, C_l, C_{b12}, C_{12}, and C_G are only for reference.

Figure D-2 Peripheral Circuit Example with No Backup

Note:

V_{DDI} is the power supply pin for input and I/O ports.
V_{DDI} must be connected to the positive power supply pin (V_{DD}) of the chip or the power supply pin of the external equipment.



- Crystal oscillation is selected by mask option for low-speed oscillation.
- Ceramic oscillation is selected for high-speed oscillation.
- The power supply for the ports is shared with V_{DD}.
- C_V is an IC power supply bypass capacitor.
- Capacitance values for C_a, C_b, C_c, C_d, C_e, C_l, C_{b12}, C_{12}, and C_G are only for reference.

Figure D-3 Peripheral Circuit Example with No Backup

Note:

V_{DDI} is the power supply pin for input and I/O ports.
V_{DDI} must be connected to the positive power supply pin (V_{DD}) of the chip or the power supply pin of the external equipment.

Appendix E Electrical Characteristics

Absolute Maximum Ratings

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage 1	V_{DD1}	Ta = 25°C	–0.3 to +1.6	V
Power Supply Voltage 2	V_{DD2}	Ta = 25°C	–0.3 to +2.9	V
Power Supply Voltage 3	V_{DD3}	Ta = 25°C	–0.3 to +4.2	V
Power Supply Voltage 4	V_{DD4}	Ta = 25°C	–0.3 to +5.5	V
Power Supply Voltage 5	V_{DD5}	Ta = 25°C	–0.3 to +6.8	V
Power Supply Voltage 6	V_{DD}	Ta = 25°C	–0.3 to +6.0	V
Power Supply Voltage 7	V_{DDI}	Ta = 25°C	–0.3 to +6.0	V
Power Supply Voltage 8	V_{DDH}	Ta = 25°C	–0.3 to +6.0	V
Power Supply Voltage 9	V_{DDL}	Ta = 25°C	–0.3 to +6.0	V
Input Voltage 1	V_{IN1}	V_{DD} Input, Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Input Voltage 2	V_{IN2}	V_{DDI} Input, Ta = 25°C	–0.3 to V_{DDI} + 0.3	V
Output Voltage 1	V_{OUT1}	V_{DD1} Output, Ta = 25°C	–0.3 to V_{DD1} + 0.3	V
Output Voltage 2	V_{OUT2}	V_{DD2} Output, Ta = 25°C	–0.3 to V_{DD2} + 0.3	V
Output Voltage 3	V_{OUT3}	V_{DD3} Output, Ta = 25°C	–0.3 to V_{DD3} + 0.3	V
Output Voltage 4	V_{OUT4}	V_{DD4} Output, Ta = 25°C	–0.3 to V_{DD4} + 0.3	V
Output Voltage 5	V_{OUT5}	V_{DD5} Output, Ta = 25°C	–0.3 to V_{DD5} + 0.3	V
Output Voltage 6	V_{OUT6}	V_{DD} Output, Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Output Voltage 7	V_{OUT7}	V_{DDI} Output, Ta = 25°C	–0.3 to V_{DDI} + 0.3	V
Output Voltage 8	V_{OUT8}	V_{DDH} Output, Ta = 25°C	–0.3 to V_{DDH} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

Recommended Operating Conditions

• When backup is used

(V_{SS} = 0 V)

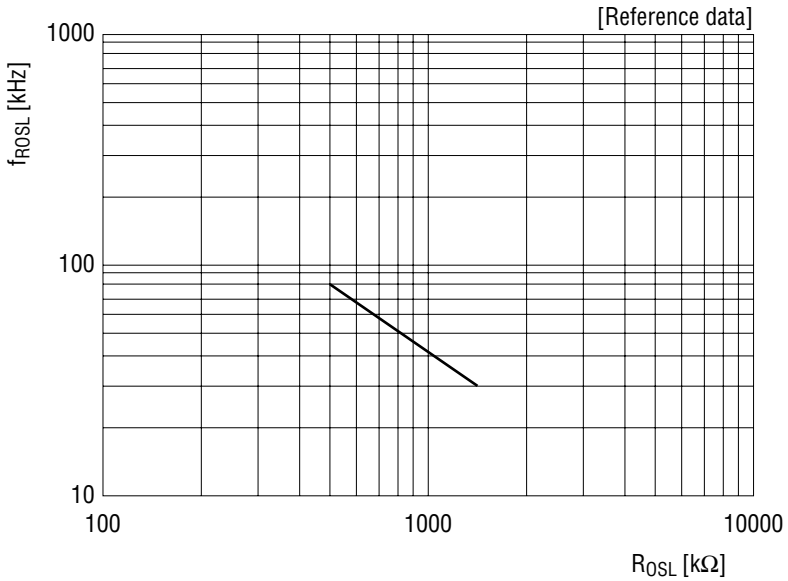
Parameter	Symbol	Condition		Range	Unit
Operating Temperature	T_{op}	—		–20 to +70	°C
Operating Voltage	V_{DD}	—		0.9 to 2.7	V
	V_{DDI}	—		0.9 to 5.5	V
Crystal Oscillation Frequency	f_{XT}	C_G = 5 to 25 pF		32.768 to 76.8	kHz
Low-speed RC Oscillation Frequency	f_{ROSL}	R_{OSL} = 1.5 MΩ		32 ±30%	kHz
		R_{OSL} = 700 kΩ		60 ±30%	
		R_{OSL} = 500 kΩ		80 ±30%	
Ceramic Oscillation Frequency	f_{CM}	V_{DD} = 0.9 to 1.2 V		Not applied	Hz
		V_{DD} = 1.2 to 2.7 V		300k to 500k	
		V_{DD} = 1.5 to 2.7 V		200k to 1M	
High-speed RC Oscillation Frequency	f_{ROSH}	V_{DD} = 0.9 to 1.2 V		Not applied	Hz
		V_{DD} = 1.2 to 2.7 V	R_{OSH} = 400 kΩ	200k ±30%	
			R_{OSH} = 100 kΩ	700k ±30%	
			R_{OSH} = 75 kΩ	1M ±30%	

• When backup is not used

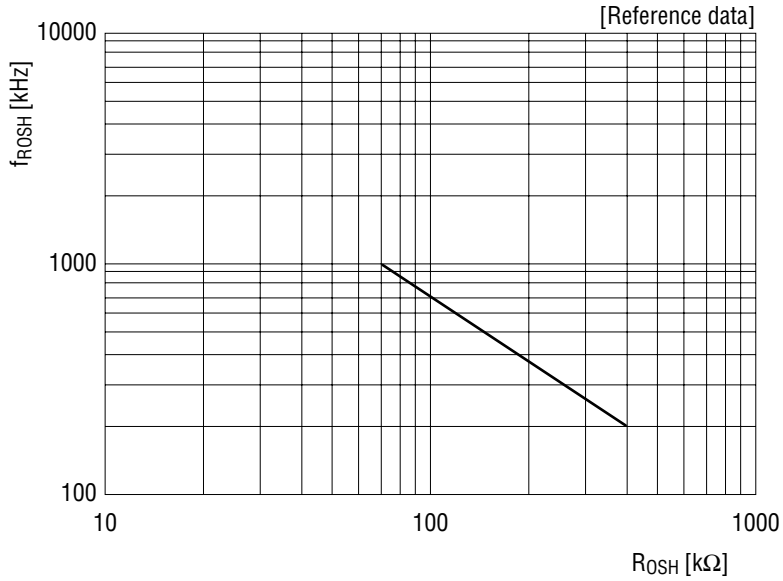
(V_{SS} = 0 V)

Parameter	Symbol	Condition		Range	Unit
Operating Temperature	T_{op}	—		–20 to +70	°C
Operating Voltage	V_{DD}	—		1.8 to 5.5	V
	V_{DDI}	—		1.8 to 5.5	V
Crystal Oscillation Frequency	f_{XT}	C_G = 5 to 25 pF		32.768 to 76.8	kHz
Low-speed RC Oscillation Frequency	f_{ROSL}	R_{OSL} = 1.5 MΩ		32 ±30%	kHz
		R_{OSL} = 700 kΩ		60 ±30%	
		R_{OSL} = 500 kΩ		80 ±30%	
Ceramic Oscillation Frequency	f_{CM}	V_{DD} = 1.8 to 5.5 V		200k to 2M	Hz
High-speed RC Oscillation Frequency	f_{ROSH}	V_{DD} = 1.8 to 5.5 V	R_{OSH} = 100 kΩ	700k ±30%	Hz
			R_{OSH} = 75 kΩ	1M ±30%	
			R_{OSH} = 51 kΩ	1.35M ±30%	
		V_{DD} = 1.8 to 3.5 V, R_{OSH} = 30 kΩ		2M ±30%	

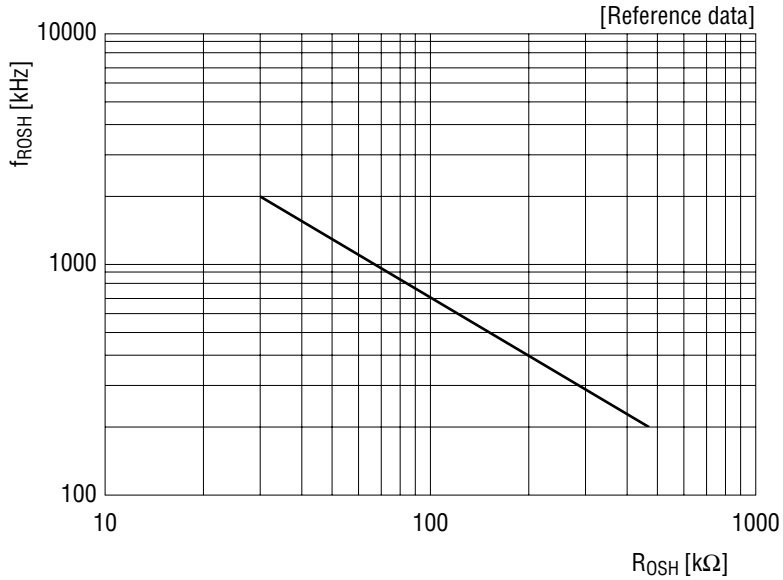
• Typical characteristics of low-speed RC oscillation
When backup is used (V_{DD} = V_{DDI} = 1.5 V)/backup is not used (V_{DD} = V_{DDI} = 3.0 V)



• Typical characteristics of high-speed RC oscillation
When backup is used (V_{DD} = V_{DDI} = 1.5 V)



• Typical characteristics of high-speed RC oscillation
When backup is not used (V_{DD} = V_{DDI} = 3.0 V)



DC Characteristics

(V_{DD} = V_{DDI} = 0.9 to 5.5 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V_{DD2} Voltage	V_{DD2}	1/5 bias, 1/4 bias (Ta = 25°C)	1.7	1.8	1.9	V	
V_{DD2} Voltage Temperature Deviation	ΔV_{DD2}	—	—	–4	—	mV/°C	
V_{DD1} Voltage	V_{DD1}	1/5 bias, 1/4 bias	Typ.– 0.1	1/2 × V_{DD2}	Typ.+ 0.1	V	
V_{DD3} Voltage	V_{DD3}	1/5 bias	Typ.– 0.3	3/2 × V_{DD2}	Typ.+ 0.3	V	
		1/4 bias (connect V_{DD3} and V_{DD2})	Typ.– 0.2	V_{DD2}	Typ.+ 0.2		
V_{DD4} Voltage	V_{DD4}	1/5 bias	Typ.– 0.4	2 × V_{DD2}	Typ.+ 0.4	V	
		1/4 bias	Typ.– 0.3	3/2 × V_{DD2}	Typ.+ 0.3		
V_{DD5} Voltage	V_{DD5}	1/5 bias	Typ.– 0.5	5/2 × V_{DD2}	Typ.+ 0.5	V	
		1/4 bias	Typ.– 0.4	2 × V_{DD2}	Typ.+ 0.4		
V_{DDH} Voltage (Backup used)	V_{DDH}	High-speed clock oscillation stopped V_{DD} = 1.5 V	2.8	—	3.0	V	1
		High-speed clock oscillation (Ceramic oscillation, 1 MHz) V_{DD} = 1.5 V	2.0	—	2.7	V	
V_{DDL} Voltage	V_{DDL}	High-speed clock oscillation stopped	1.0	1.5	2.0	V	
		High-speed clock oscillation (V_{DD} = 1.2 to 5.5 V)	1.2	—	5.5	V	
Crystal Oscillation Start Voltage	V_{STA}	Oscillation start time: within 5 seconds	1.2	—	—	V	
Crystal Oscillation Hold Voltage	V_{HOLD}	Backup used	0.9	—	—	V	
		Backup not used	1.7	—	—	V	
Crystal Oscillation Stop Detect Time	T_{STOP}	—	0.1	—	5.0	ms	
External Crystal Oscillator Capacitance	C_G	—	5	—	25	pF	
Internal Crystal Oscillator Capacitance	C_D	—	20	25	30	pF	
External Ceramic Oscillator Capacitance	$C_{L0, 1}$	CSA2.00MG (Murata MFG.-make) used V_{DD} = 3.0 V	—	30	—	pF	
Internal RC Oscillator Capacitance	C_{OS}	—	8	12	16	pF	
POR Voltage	V_{POR1}	V_{DD} = 1.5 V	0.0	—	0.4	V	
		V_{DD} = 3.0 V	0.0	—	0.7	V	
Non-POR Voltage	V_{POR2}	V_{DD} = 1.5 V	1.2	—	1.5	V	
		V_{DD} = 3.0 V	2.0	—	3.0	V	
BLD Judgment Voltage	V_{BLDC}	LD1 = 1, LD0 = 1, Ta = 25°C	2.30	2.40	2.50	V	—
		LD1 = 1, LD0 = 0, Ta = 25°C	1.70	1.80	1.90		
		LD1 = 0, LD0 = 1, Ta = 25°C	1.10	1.20	1.30		
		LD1 = 0, LD0 = 0, Ta = 25°C	0.95	1.05	1.15		
BLD Judgment Voltage Temperature Deviation	ΔV_{BLDC}	V_{BLDC} = 2.40 V (LD1 = 1, LD0 = 1)	—	–3.5	—	mV/°C	
		V_{BLDC} = 1.80 V (LD1 = 1, LD0 = 0)	—	–2.3	—		
		V_{BLDC} = 1.20 V (LD1 = 0, LD0 = 1)	—	–1.6	—		
		V_{BLDC} = 1.05 V (LD1 = 0, LD0 = 0)	—	–1.2	—		

Notes: 1. "V_{DD2}" voltage varies from 1.8 to 2.4 V depending on the value of the display contrast register (DSPCNT).
2. "T_{STOP}" indicates that if the crystal oscillator stops over the value of T_{STOP}, the system reset occurs.
3. "POR" denotes Power On Reset.
4. "V_{POR1}" indicates that POR occurs when V_{DD} falls from V_{DD} to V_{POR1} and again rises up to V_{DD}.
5. "V_{POR2}" indicates that POR does not occur when V_{DD} falls from V_{DD} to V_{POR2} and again rises up to V_{DD}.

DC Characteristics (continued)

• When backup is used (ML63187/ML63189B)

(32.768 kHz crystal is used for the low-speed clock, $V_{DD} = V_{DDI} = 1.5$ V, $V_{SS} = 0$ V, 1/5 bias, LCD contrast (DSPCNT) = 0H, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU is in HALT state. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	5	6.5	µA	1
			Ta = –20 to +70°C	—	5	10		
Supply Current 2	I_{DD2}	CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	4	5	µA	
			Ta = –20 to +70°C	—	4	8		
Supply Current 3	I_{DD3}	CPU is in operation at low-speed oscillation. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	16	18	µA	
			Ta = –20 to +70°C	—	16	20	µA	
Supply Current 4	I_{DD4}	CPU is in operation at high-speed oscillation (approx.700 kHz RC oscillation, R_{OSH} = 100 kΩ)		—	800	1000	µA	
Supply Current 5	I_{DD5}	CPU is in operation at high-speed oscillation (Ceramic oscillation, 1 MHz)		—	700	850	µA	

• When backup is not used (ML63187/ML63189B)

(32.768 kHz crystal is used for the low-speed clock, $V_{DD} = V_{DDI} = 3.0$ V, $V_{SS} = 0$ V, 1/5 bias, LCD contrast (DSPCNT) = 0H, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU is in HALT state. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	2.2	3	µA	1
			Ta = –20 to +70°C	—	2.2	5		
Supply Current 2	I_{DD2}	CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	1.8	2.5	µA	
			Ta = –20 to +70°C	—	1.8	4		
Supply Current 3	I_{DD3}	CPU is in operation at low-speed oscillation. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	7.5	9	µA	
			Ta = –20 to +70°C	—	7.5	12		
Supply Current 4	I_{DD4}	CPU is in operation at high-speed oscillation (approx. 700 kHz RC oscillation, R_{OSH} = 100 kΩ)		—	550	700	µA	
Supply Current 5	I_{DD5}	CPU is in operation at high-speed oscillation (Ceramic oscillation, 2 MHz)		—	850	1000	µA	

DC Characteristics (continued)

• When backup is used (ML63193)

(32.768 kHz crystal is used for the low-speed clock, $V_{DD} = V_{DDI} = 1.5$ V, $V_{SS} = 0$ V, 1/5 bias, LCD contrast (DSPCNT) = 0H, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU is in HALT state. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	5.6	6.5	µA	1
			Ta = –20 to +70°C	—	5.6	15.0		
Supply Current 2	I_{DD2}	CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	4.5	5.0	µA	
			Ta = –20 to +70°C	—	4.5	13.0		
Supply Current 3	I_{DD3}	CPU is in operation at low-speed oscillation. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	23	26	µA	
			Ta = –20 to +70°C	—	23	30	µA	
Supply Current 4	I_{DD4}	CPU is in operation at high-speed oscillation (approx. 700 kHz RC oscillation, $R_{OSH} = 100$ kΩ)		—	1100	1500	µA	
Supply Current 5	I_{DD5}	CPU is in operation at high-speed oscillation (Ceramic oscillation, 1 MHz)		—	950	1200	µA	

• When backup is not used (ML63193)

(32.768 kHz crystal is used for the low-speed clock, $V_{DD} = V_{DDI} = 3.0$ V, $V_{SS} = 0$ V, 1/5 bias, LCD contrast (DSPCNT) = 0H, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU is in HALT state. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	2.6	3.5	µA	1
			Ta = –20 to +70°C	—	2.6	7.0		
Supply Current 2	I_{DD2}	CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	2.0	2.8	µA	
			Ta = –20 to +70°C	—	2.0	6.0		
Supply Current 3	I_{DD3}	CPU is in operation at low-speed oscillation. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	12	13	µA	
			Ta = –20 to +70°C	—	12	16		
Supply Current 4	I_{DD4}	CPU is in operation at high-speed oscillation (approx. 700 kHz RC oscillation, $R_{OSH} = 100$ kΩ)		—	1000	1200	µA	
Supply Current 5	I_{DD5}	CPU is in operation at high-speed oscillation (Ceramic oscillation, 2 MHz)		—	1100	1300	µA	

DC Characteristics (continued)

(V_{DD} = V_{DDI} = V_{DDH} = 3.0 V, V_{DD1} = 1.1 V, V_{DD2} = 2.2 V, V_{DD3} = 3.3 V, V_{DD4} = 4.4 V, V_{DD5} = 5.5 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1 (P9.0 to P9.3)*1 (PA.0 to PA.3)*1 (PB.0 to PB.3) (PC.0 to PC.3)*2 (PE.0 to PE.3)	I_{OH1}	V_{OH1} = V_{DDI} – 0.5 V	V_{DDI} = 1.5 V	–2.5	–1.4	–0.4	mA	
			V_{DDI} = 3.0 V	–6.0	–3.5	–1.0	mA	
			V_{DDI} = 5.0 V	–8.5	–5.0	–1.5	mA	
	I_{OL1}	V_{OL1} = 0.5 V	V_{DDI} = 1.5 V	0.4	1.4	2.5	mA	
			V_{DDI} = 3.0 V	1.0	3.0	6.0	mA	
			V_{DDI} = 5.0 V	1.5	3.7	8.5	mA	
Output Current 2 (MD, MDB)	I_{OH2}	V_{OH2} = V_{DD} – 0.7 V	V_{DD} = 1.5 V	–4.0	–2.0	–0.5	mA	
			V_{DD} = 3.0 V	–11.0	–6.0	–2.0	mA	
			V_{DD} = V_{DDH} = 5.0 V	–14.0	–9.0	–4.0	mA	
	I_{OL2}	V_{OL2} = 0.7 V	V_{DD} = 1.5 V	0.5	2.0	4.0	mA	
			V_{DD} = 3.0 V	2.0	5.5	11.0	mA	
			V_{DD} = V_{DDH} = 5.0 V	4.0	7.0	14.0	mA	
Output Current 3 (SEG0 to SEG63) (COM1 to COM16)	I_{OH3}	V_{OH3} = V_{DD5} – 0.2 V (V_{DD5} level)		—	—	–4	µA	
	I_{OHM3}	V_{OHM3} = V_{DD4} + 0.2 V (V_{DD4} level)		4	—	—	µA	
	I_{OHM3S}	V_{OHM3S} = V_{DD4} – 0.2 V (V_{DD4} level)		—	—	–4	µA	
	I_{OMH3}	V_{OMH3} = V_{DD3} + 0.2 V (V_{DD3} level)		4	—	—	µA	
	I_{OMH3S}	V_{OMH3S} = V_{DD3} – 0.2 V (V_{DD3} level)		—	—	–4	µA	
	I_{OML3}	V_{OML3} = V_{DD2} + 0.2 V (V_{DD2} level)		4	—	—	µA	2
	I_{OML3S}	V_{OML3S} = V_{DD2} – 0.2 V (V_{DD2} level)		—	—	–4	µA	
	I_{OLM3}	V_{OLM3} = V_{DD1} + 0.2 V (V_{DD1} level)		4	—	—	µA	
	I_{OLM3S}	V_{OLM3S} = V_{DD1} – 0.2 V (V_{DD1} level)		—	—	–4	µA	
	I_{OL3}	V_{OL3} = V_{SS} + 0.2 V (V_{SS} level)		4	—	—	µA	
Output Current 4 (OSC1)	I_{OH4R}	V_{OH4R} = V_{DDH} – 0.5 V (RC oscillation)	V_{DD} = V_{DDH} = 3.0 V	–2.5	–1.3	–0.25	mA	
			V_{DD} = V_{DDH} = 5.0 V	–3.5	–1.7	–0.5	mA	
	I_{OL4R}	V_{OL4R} = 0.5 V (RC oscillation)	V_{DD} = V_{DDH} = 3.0 V	0.25	1.5	2.5	mA	
			V_{DD} = V_{DDH} = 5.0 V	0.5	1.8	3.5	mA	
	I_{OH4C}	V_{OH4C} = V_{DDH} – 0.5 V (ceramic oscillation)	V_{DD} = V_{DDH} = 3.0 V	–500	–250	–100	µA	
			V_{DD} = V_{DDH} = 5.0 V	–800	–350	–200	µA	
	I_{OL4C}	V_{OL4C} = 0.5 V (ceramic oscillation)	V_{DD} = V_{DDH} = 3.0 V	200	500	800	µA	
			V_{DD} = V_{DDH} = 5.0 V	400	700	1000	µA	
Output Leakage Current (P9.0 to P9.3)*1 (PA.0 to PA.3)*1 (PB.0 to PB.3) (PC.0 to PC.3)*2 (PE.0 to PE.3)	I_{OOH}	V_{OH} = V_{DDI}		—	—	0.3	µA	
	I_{OOL}	V_{OL} = V_{SS}		–0.3	—	—	µA	

*1 Applies to the ML63189B and ML63193.

*2 Applies to the ML63193 only.

DC Characteristics (continued)

($V_{DD} = V_{DDI} = V_{DDH} = 3.0$ V, $V_{DD1} = 1.1$ V, $V_{DD2} = 2.2$ V, $V_{DD3} = 3.3$ V, $V_{DD4} = 4.4$ V, $V_{DD5} = 5.5$ V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Input Current 1 (P0.0 to P0.3)*1 (P9.0 to P9.3)*1 (PA.0 to PA.3)*1 (PB.0 to PB.3) (PC.0 to PC.3)*2 (PE.0 to PE.3)	I_{IH1}	$V_{IH1} = V_{DDI}$ (when pulled down)	V_{DDI} = 1.5 V	2	20	45	µA	3
			V_{DDI} = 3.0 V	30	120	260	µA	
			V_{DDI} = 5.0 V	70	350	650	µA	
	I_{IL1}	$V_{IL1} = V_{SS}$ (when pulled up)	V_{DDI} = 1.5 V	–45	–20	–2	µA	
			V_{DDI} = 3.0 V	–260	–120	–30	µA	
			V_{DDI} = 5.0 V	–650	–350	–70	µA	
	I_{IH1Z}	$V_{IH1} = V_{DDI}$ (in a high impedance state)		0.0	—	1.0	µA	
	I_{IL1Z}	$V_{IL1} = V_{SS}$ (in a high impedance state)		–1.0	—	0.0	µA	
Input Current 2 (OSC0)	I_{IL2}	$V_{IL2} = V_{SS}$ (when pulled up)	$V_{DD} = V_{DDH}$ = 3.0 V	–350	–170	–30	µA	
			$V_{DD} = V_{DDH}$ = 5.0 V	–750	–450	–200	µA	
	I_{IH2R}	$V_{IH2R} = V_{DDH}$ (RC oscillation)		0.0	—	1.0	µA	
	I_{IL2R}	$V_{IL2R} = V_{SS}$ (RC oscillation)		–1.0	—	0.0	µA	
	I_{IH2C}	$V_{IH2C} = V_{DDH}$ (ceramic oscillation)	$V_{DD} = V_{DDH}$ = 3.0 V	0.5	1.8	4.0	µA	
			$V_{DD} = V_{DDH}$ = 5.0 V	3	6	10	µA	
	I_{IL2C}	$V_{IL2C} = V_{SS}$ (ceramic oscillation)	$V_{DD} = V_{DDH}$ = 3.0 V	–4.0	–1.8	–0.5	µA	
			$V_{DD} = V_{DDH}$ = 5.0 V	–10	–6	–3	µA	
Input Current 3 (RESET)	I_{IH3}	$V_{IH3} = V_{DD}$	V_{DD} = 1.5 V	10	180	350	µA	
			V_{DD} = 3.0 V	150	1100	2400	µA	
			$V_{DD} = V_{DDH}$ = 5.0 V	0.5	2.7	5.0	mA	
	I_{IL3}	$V_{IL3} = V_{SS}$		–1.0	—	0.0	µA	
Input Current 4 (TST1, TST2)	I_{IH4}	$V_{IH4} = V_{DD}$	V_{DD} = 1.5 V	50	750	1500	µA	
			V_{DD} = 3.0 V	0.5	3.0	5.5	mA	
			$V_{DD} = V_{DDH}$ = 5.0 V	2.0	6.5	11.0	mA	
	I_{IL4}	$V_{IL4} = V_{SS}$		–1.0	—	0.0	µA	

*1 Applies to the ML63189B and ML63193.

*2 Applies to the ML63193 only.

DC Characteristics (continued)

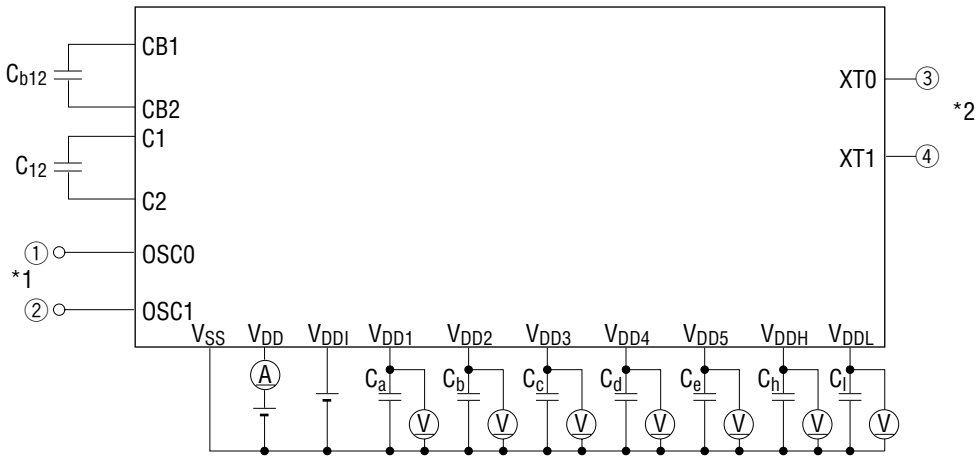
(V_{DD} = V_{DDI} = V_{DDH} = 3.0 V, V_{DD1} = 1.1 V, V_{DD2} = 2.2 V, V_{DD3} = 3.3 V, V_{DD4} = 4.4 V, V_{DD5} = 5.5 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Voltage 1 (P0.0 to P0.3)*1 (P9.0 to P9.3)*1 (PA.0 to PA.3)*1 (PB.0 to PB.3) (PC.0 to PC.3)*2 (PE.0 to PE.3)	V_{IH1}	V_{DDI} = 1.5 V	1.2	—	1.5	V	
		V_{DDI} = 3.0 V	2.4	—	3.0	V	
		V_{DDI} = 5.0 V	4.0	—	5.0	V	
	V_{IL1}	V_{DDI} = 1.5 V	0.0	—	0.3	V	
		V_{DDI} = 3.0 V	0.0	—	0.6	V	
		V_{DDI} = 5.0 V	0.0	—	1.0	V	
Input Voltage 2 (OSC0)	V_{IH2}	V_{DD} = V_{DDH} = 3.0 V	2.4	—	3.0	V	
		V_{DD} = V_{DDH} = 5.0 V	4.0	—	5.0	V	
	V_{IL2}	V_{DD} = V_{DDH} = 3.0 V	0.0	—	0.6	V	
		V_{DD} = V_{DDH} = 5.0 V	0.0	—	1.0	V	
Input Voltage 3 (RESET, TST1, TST2)	V_{IH3}	V_{DD} = 1.5 V	1.35	—	1.5	V	
		V_{DD} = 3.0 V	2.4	—	3.0	V	
		V_{DD} = 5.0 V	4.0	—	5.0	V	4
	V_{IL3}	V_{DD} = 1.5 V	0.0	—	0.15	V	
		V_{DD} = 3.0 V	0.0	—	0.6	V	
		V_{DD} = 5.0 V	0.0	—	1.0	V	
Hysteresis Width 1 (P0.0 to P0.3)*1 (P9.0 to P9.3)*1 (PA.0 to PA.3)*1 (PB.0 to PB.3) (PC.0 to PC.3)*2 (PE.0 to PE.3)	ΔV_{T1}	V_{DDI} = 1.5 V	0.05	0.1	0.3	V	
		V_{DDI} = 3.0 V	0.2	0.5	1.0	V	
		V_{DDI} = 5.0 V	0.25	1.0	1.5	V	
Hysteresis Width 2 (RESET, TST1, TST2)	ΔV_{T2}	V_{DD} = 1.5 V	0.05	0.1	0.3	V	
		V_{DD} = 3.0 V	0.2	0.5	1.0	V	
		V_{DD} = 5.0 V	0.25	1.0	1.5	V	
Input Pin Capacitance (P0.0 to P0.3)*1 (P9.0 to P9.3)*1 (PA.0 to PA.3)*1 (PB.0 to PB.3) (PC.0 to PC.3)*2 (PE.0 to PE.3)	C_{IN}	—	—	—	5	pF	1

*1 Applies to the ML63189B and ML63193.

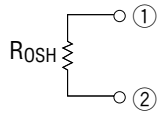
*2 Applies to the ML63193 only.

Measuring circuit 1

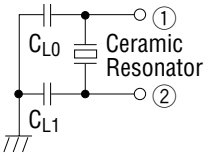


C_a, C_b, C_c, C_d, C_e, C_l, C_{12} : 0.1 µF
C_{b12}, C_h : 1 µF
C_G : 15 pF
C_{L0} : 30 pF
C_{L1} : 30 pF
Ceramic Resonator : CSA2.00MG (2 MHz)
CSB1000J (1 MHz)
(Murata MFG.-make)

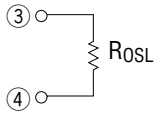
*1 RC Oscillator



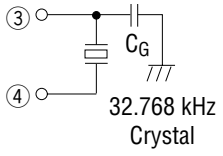
Ceramic Oscillator



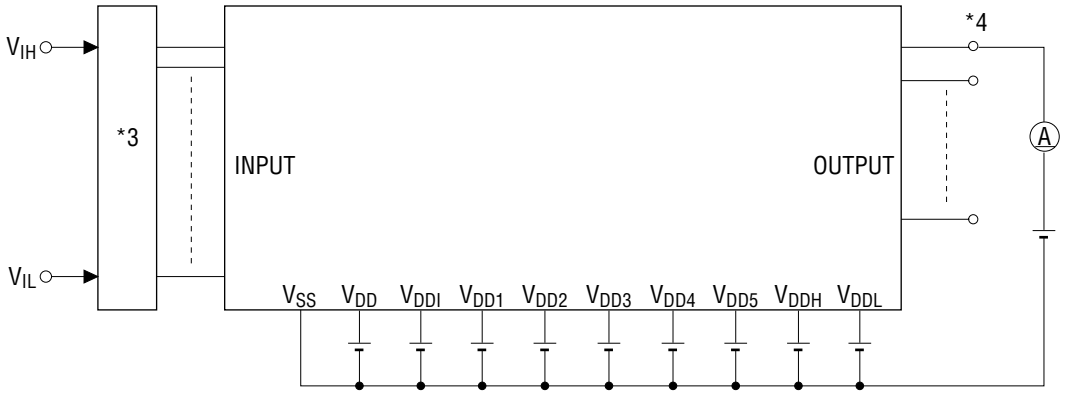
*2 RC Oscillator



Crystal Oscillator

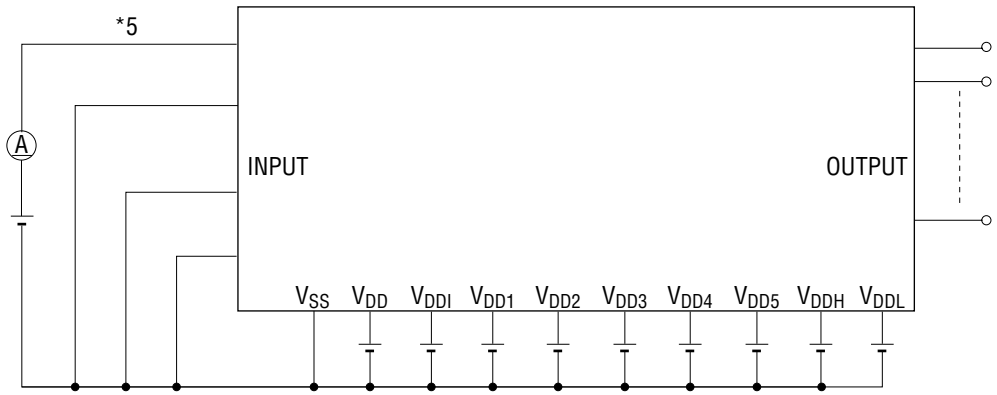


Measuring circuit 2

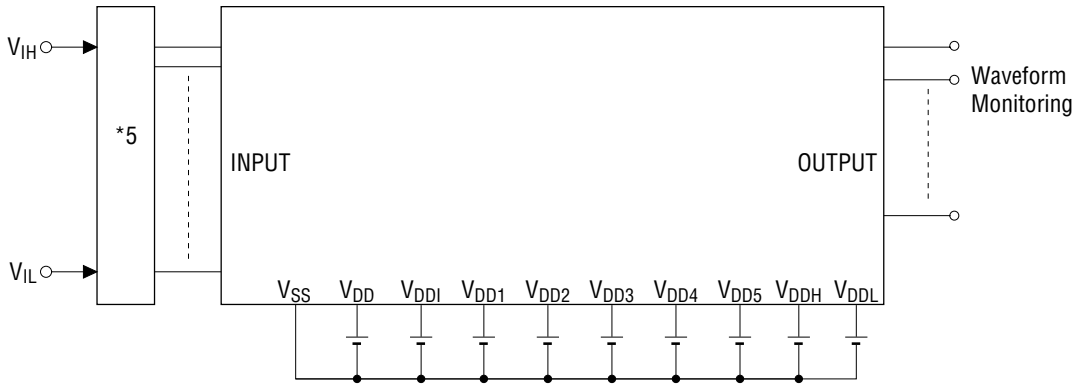


*3 Input logic circuit to determine the specified measuring conditions.
*4 Measured at the specified output pins.

Measuring circuit 3



Measuring circuit 4



*5 Measured at the specified input pins.

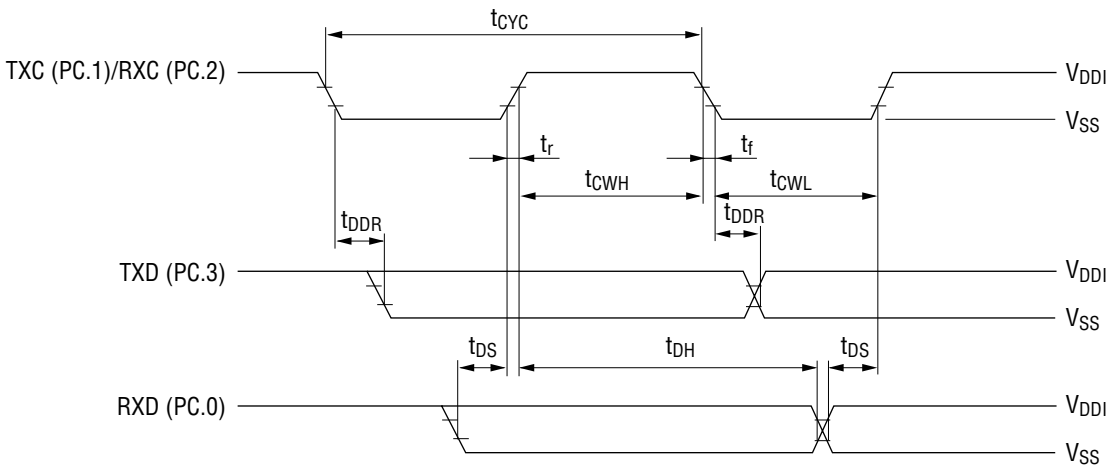
AC Characteristics (Serial Interface, Serial Port) [Only applies to the ML63193]

(V_{DD} = 0.9 to 5.5 V, V_{DDH} = 1.8 to 5.5 V, V_{SS} = 0 V, V_{DDI} = 5.0 V, Ta = –20 to +70°C unless otherwise specified)

(1) Synchronous Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
TXC/RXC Input Fall Time	t_f	—	—	—	1.0	µs
TXC/RXC Input Rise Time	t_r	—	—	—	1.0	µs
TXC/RXC Input "L" Level Pulse Width	t_{CWL}	—	0.8	—	—	µs
TXC/RXC Input "H" Level Pulse Width	t_{CWH}	—	0.8	—	—	µs
TXC/RXC Input Cycle Time	t_{CYC}	—	2.0	—	—	µs
TXC/RXC Output Cycle Time	$t_{CYC(O)}$	CPU in operation state at 32.768 kHz	—	30.5	—	µs
TXD Output Delay Time	t_{DDR}	Output load capacitance 10 pF	—	—	0.4	µs
RXD Input Setup Time	t_{DS}	—	0.5	—	—	µs
RXD Input Hold Time	t_{DH}	—	0.8	—	—	µs

Synchronous Communication Timing Waveforms
("H" level = 4.0 V, "L" level = 1.0 V)

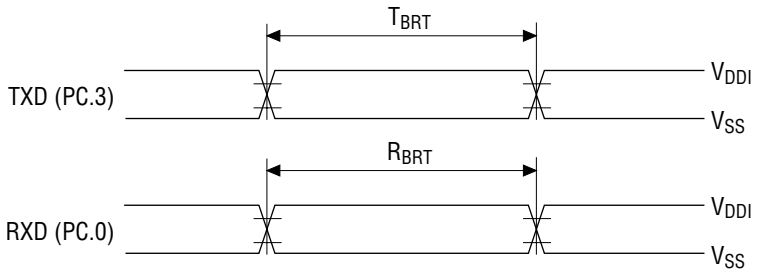


(2) UART Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit Baud Rate	T_{BRT}	$T_{BRT}=1/f_{BRT}$ $T_{CR}=1/f_{OSC}$	$T_{BRT}-T_{CR}$	T_{BRT}	$T_{BRT}+T_{CR}$	s
Receive Baud Rate	R_{BRT}	$R_{BRT}=1/f_{BRT}$	$R_{BRT}\times0.97$	R_{BRT}	$R_{BRT}\times1.03$	s

f_{BRT}: Baud rates (1200, 2400, 4800, 9600 bps)

UART Communication Timing Waveforms
("H" level = 4.0 V, "L" level = 1.0 V)

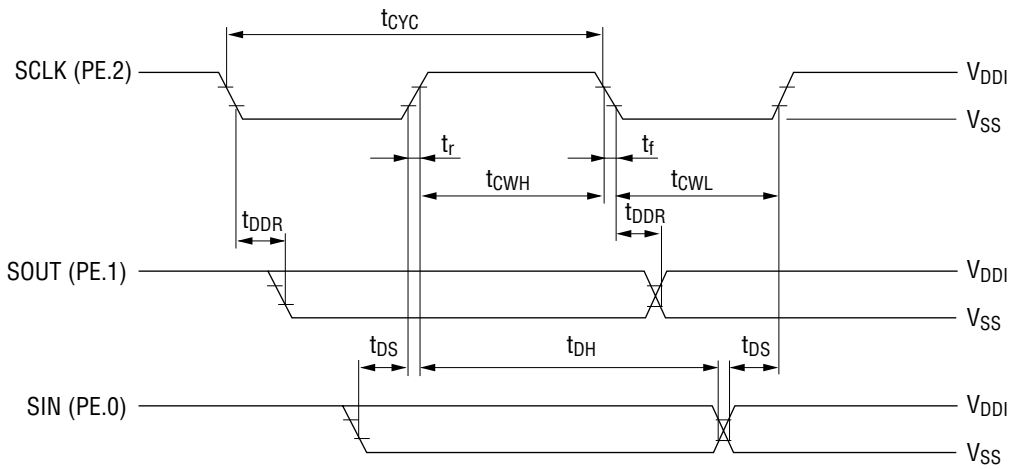


AC Characteristics (Serial Interface, Shift Register)

(V_{DD} = 0.9 to 5.5 V, V_{DDH} = 1.8 to 5.5 V, V_{SS} = 0 V, V_{DDI} = 5.0 V, Ta = –20 to +70°C unless otherwise specified)

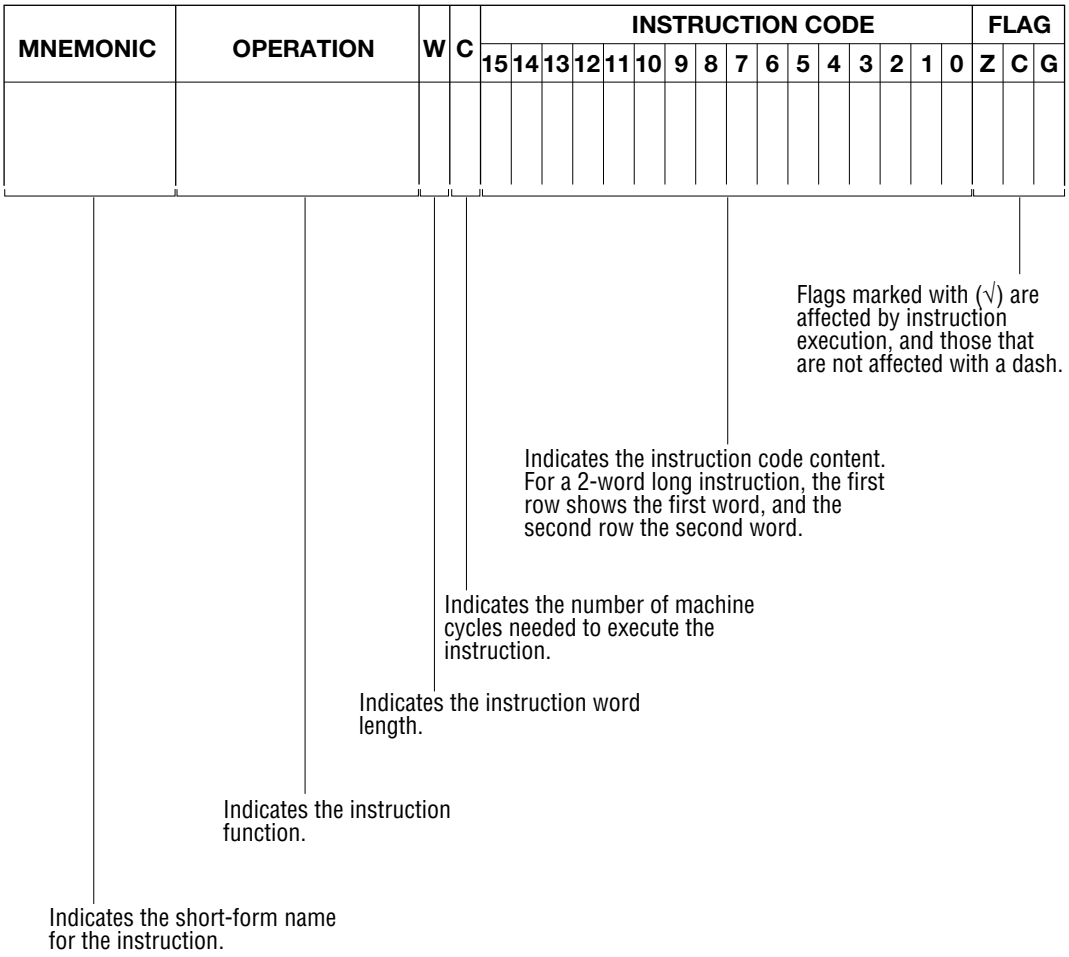
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK Input Fall Time	t_f	—	—	—	1.0	µs
SCLK Input Rise Time	t_r	—	—	—	1.0	µs
SCLK Input "L" Level Pulse Width	t_{CWL}	—	0.8	—	—	µs
SCLK Input "H" Level Pulse Width	t_{CWH}	—	0.8	—	—	µs
SCLK Input Cycle Time	t_{CYC}	V_{DDI} = 5 V to V_{DD}	1.8	—	—	µs
SCLK Output Cycle Time	$t_{CYC1(O)}$	CPU in operation state at 32.768 kHz	—	30.5	—	µs
	$t_{CYC2(O)}$	CPU in operation at 2 MHz V_{DD} = V_{DDH} = 1.8 V to 3.5 V	—	0.5	—	µs
SOUT Output Delay Time	t_{DDR}	C_I = 10 pF	—	—	0.4	µs
SIN Input Setup Time	t_{DS}	—	0.5	—	—	µs
SIN Input Hold Time	t_{DH}	—	0.8	—	—	µs

AC characteristics timing
("H" level = 4.0 V, "L" level = 1.0 V)



Appendix F Instruction List

The format used in the list of instructions is indicated below.



Transfer Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MOV direct,A	direct←A	1	1	1	1	0	0	r_{11}	r_{10}	r_9	r_8	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	—	—	—
MOV [HL],A	[HL]←A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	—	—	—
MOV [XY],A	[XY]←A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	—	—	—
MOV E:[HL],A	E:[HL]←A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	—	—	—
MOV E:[XY],A	E:[XY]←A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	—	—	—
MOV [HL+],A	[HL]←A,HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0	—	—	√
MOV [XY+],A	[XY]←A,XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	—	—	√
MOV E:[HL+],A	E:[HL]←A,HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	—	—	√
MOV E:[XY+],A	E:[XY]←A,XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0	—	—	√
MOV ¥cur,#i4	cur,A←i4	1	1	0	1	0	0	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MOV [HL],#i4	[HL],A←i4	1	1	0	0	0	0	0	1	1	0	0	1	1	0	i_3	i_2	i_1	i_0	√	—	—
MOV [XY],#i4	[XY],A←i4	1	1	0	0	0	0	0	1	1	0	0	1	1	1	i_3	i_2	i_1	i_0	√	—	—
MOV E:[HL],#i4	E:[HL],A←i4	1	1	0	0	0	0	0	1	1	0	0	1	0	0	i_3	i_2	i_1	i_0	√	—	—
MOV E:[XY],#i4	E:[XY],A←i4	1	1	0	0	0	0	0	1	1	0	0	1	0	1	i_3	i_2	i_1	i_0	√	—	—
MOV [HL+],#i4	[HL],A←i4,HL←HL+1	1	1	0	0	0	0	0	1	1	1	0	1	1	0	i_3	i_2	i_1	i_0	√	—	√
MOV [XY+],#i4	[XY],A←i4,XY←XY+1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	i_3	i_2	i_1	i_0	√	—	√
MOV E:[HL+],#i4	E:[HL],A←i4,HL←HL+1	1	1	0	0	0	0	0	1	1	1	0	1	0	0	i_3	i_2	i_1	i_0	√	—	√
MOV E:[XY+],#i4	E:[XY],A←i4,XY←XY+1	1	1	0	0	0	0	0	1	1	1	0	1	0	1	i_3	i_2	i_1	i_0	√	—	√
MOV A,#i4	A←i4	1	1	0	0	0	0	0	0	0	1	1	1	0	0	i_3	i_2	i_1	i_0	√	—	—
MOV A,direct	A←direct	1	1	1	1	0	1	r_{11}	r_{10}	r_9	r_8	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MOV A,[HL]	A←[HL]	1	1	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	√	—	—
MOV A,[XY]	A←[XY]	1	1	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	√	—	—
MOV A,E:[HL]	A←E:[HL]	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	√	—	—
MOV A,E:[XY]	A←E:[XY]	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	√	—	—
MOV A,[HL+]	A←[HL],HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	√	—	√
MOV A,[XY+]	A←[XY],XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	0	1	1	1	0	0	0	√	—	√
MOV A,E:[HL+]	A←E:[HL],HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	0	√	—	√
MOV A,E:[XY+]	A←E:[XY],XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	√	—	√
XCH A,sfr	A↔sfr	1	1	0	0	1	0	1	1	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	—	—	—
XCH A,¥cur	A↔cur	1	1	0	0	1	1	1	1	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	—	—	—
XCH A,[HL]	A↔[HL]	1	1	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	—	—	—
XCH A,[XY]	A↔[XY]	1	1	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	1	—	—	—
XCH A,E:[HL]	A↔E:[HL]	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	—	—	—
XCH A,E:[XY]	A↔E:[XY]	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	1	—	—	—
XCH A,[HL+]	A↔[HL],HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	1	—	—	√
XCH A,[XY+]	A↔[XY],XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	0	1	1	1	0	0	1	—	—	√
XCH A,E:[HL+]	A↔E:[HL],HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	1	—	—	√
XCH A,E:[XY+]	A↔E:[XY],XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	1	—	—	√

Rotate Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
ROL sfr	C←{3sfr0}←C,A←sfr	1	1	0	0	1	0	0	0	1	0	r7	r6	r5	r4	r3	r2	r1	r0	√	√	—
ROL ¥cur	C←{3cur0}←C,A←cur	1	1	0	0	1	1	0	0	1	0	r7	r6	r5	r4	r3	r2	r1	r0	√	√	—
ROL [HL]	C←{3[HL]0}←C,A←[HL]	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	0	√	√	—
ROL [XY]	C←{3[XY]0}←C,A←[XY]	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	0	√	√	—
ROL E:[HL]	C←{3E:[HL]0}←C,A←E:[HL]	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	√	√	—
ROL E:[XY]	C←{3E:[XY]0}←C,A←E:[XY]	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	√	√	—
ROL [HL+]	C←{3[HL]0}←C,A←[HL], HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1	1	0	√	√	√
ROL [XY+]	C←{3[XY]0}←C,A←[XY], XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	0	√	√	√
ROL E:[HL+]	C←{3E:[HL]0}←C, A←E:[HL],HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	√	√	√
ROL E:[XY+]	C←{3E:[XY]0}←C, A←E:[XY],XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	0	√	√	√
ROR sfr	C→{3sfr0}→C,A←sfr	1	1	0	0	1	0	0	0	1	1	r7	r6	r5	r4	r3	r2	r1	r0	√	√	—
ROR ¥cur	C→{3cur0}→C,A←cur	1	1	0	0	1	1	0	0	1	1	r7	r6	r5	r4	r3	r2	r1	r0	√	√	—
ROR [HL]	C→{3[HL]0}→C,A←[HL]	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	1	√	√	—
ROR [XY]	C→{3[XY]0}→C,A←[XY]	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	√	√	—
ROR E:[HL]	C→{3E:[HL]0}→C,A←E:[HL]	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	√	√	—
ROR E:[XY]	C→{3E:[XY]0}→C,A←E:[XY]	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	1	√	√	—
ROR [HL+]	C→{3[HL]0}→C,A←[HL], HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1	1	1	√	√	√
ROR [XY+]	C→{3[XY]0}→C,A←[XY], XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	√	√	√
ROR E:[HL+]	C→{3E:[HL]0}→C, A←E:[HL],HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	√	√	√
ROR E:[XY+]	C→{3E:[XY]0}→C, A←E:[XY],XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	√	√	√

Increment/Decrement Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
INC sfr	sfr,A←sfr+1	1	1	0	0	1	0	0	0	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
INC ¥cur	cur,A←cur+1	1	1	0	0	1	1	0	0	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
INC [HL]	[HL],A←[HL]+1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	0	√	√	—
INC [XY]	[XY],A←[XY]+1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	0	0	√	√	—
INC E:[HL]	E:[HL],A←E:[HL]+1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	√	√	—
INC E:[XY]	E:[XY],A←E:[XY]+1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0	√	√	—
INC [HL+]	[HL],A←[HL]+1, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0	0	0	√	√	√
INC [XY+]	[XY],A←[XY]+1, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	0	0	0	√	√	√
INC E:[HL+]	E:[HL],A←E:[HL]+1, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	√	√	√
INC E:[XY+]	E:[XY],A←E:[XY]+1, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	√	√	√
DEC sfr	sfr,A←sfr–1	1	1	0	0	1	0	0	0	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
DEC ¥cur	cur,A←cur–1	1	1	0	0	1	1	0	0	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
DEC [HL]	[HL],A←[HL]–1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	1	√	√	—
DEC [XY]	[XY],A←[XY]–1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	0	1	√	√	—
DEC E:[HL]	E:[HL],A←E:[HL]–1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	√	√	—
DEC E:[XY]	E:[XY],A←E:[XY]–1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	1	√	√	—
DEC [HL+]	[HL],A←[HL]–1, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0	0	1	√	√	√
DEC [XY+]	[XY],A←[XY]–1, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	0	0	1	√	√	√
DEC E:[HL+]	E:[HL],A←E:[HL]–1, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	1	√	√	√
DEC E:[XY+]	E:[XY],A←E:[XY]–1, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	1	√	√	√

Arithmetic Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
ADD sfr,A	sfr,A←sfr+A	1	1	0	0	1	0	0	1	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADD ¥cur,A	cur,A←cur+A	1	1	0	0	1	1	0	1	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADD [HL],A	[HL],A←[HL]+A	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	0	√	√	—
ADD [XY],A	[XY],A←[XY]+A	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	1	0	√	√	—
ADD E:[HL],A	E:[HL],A←E:[HL]+A	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	√	√	—
ADD E:[XY],A	E:[XY],A←E:[XY]+A	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	√	√	—
ADD [HL+],A	[HL],A←[HL]+A, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0	1	0	√	√	√
ADD [XY+],A	[XY],A←[XY]+A, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	0	1	0	√	√	√
ADD E:[HL+],A	E:[HL],A←E:[HL]+A, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	1	0	√	√	√
ADD E:[XY+],A	E:[XY],A←E:[XY]+A, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	0	1	0	√	√	√
ADD ¥cur,#i4	cur,A←cur+i4	1	1	1	0	0	0	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADD [HL],#i4	[HL],A←[HL]+i4	1	1	0	0	0	0	0	0	0	0	1	0	1	0	i_3	i_2	i_1	i_0	√	√	—
ADD [XY],#i4	[XY],A←[XY]+i4	1	1	0	0	0	0	0	0	0	0	1	0	1	1	i_3	i_2	i_1	i_0	√	√	—
ADD E:[HL],#i4	E:[HL],A←E:[HL]+i4	1	1	0	0	0	0	0	0	0	0	1	0	0	0	i_3	i_2	i_1	i_0	√	√	—
ADD E:[XY],#i4	E:[XY],A←E:[XY]+i4	1	1	0	0	0	0	0	0	0	0	1	0	0	1	i_3	i_2	i_1	i_0	√	√	—
ADD [HL+],#i4	[HL],A←[HL]+i4, HL←HL+1	1	1	0	0	0	0	0	0	0	1	1	0	1	0	i_3	i_2	i_1	i_0	√	√	√
ADD [XY+],#i4	[XY],A←[XY]+i4, XY←XY+1	1	1	0	0	0	0	0	0	0	1	1	0	1	1	i_3	i_2	i_1	i_0	√	√	√
ADD E:[HL+],#i4	E:[HL],A←E:[HL]+i4, HL←HL+1	1	1	0	0	0	0	0	0	0	1	1	0	0	0	i_3	i_2	i_1	i_0	√	√	√
ADD E:[XY+],#i4	E:[XY],A←E:[XY]+i4, XY←XY+1	1	1	0	0	0	0	0	0	0	1	1	0	0	1	i_3	i_2	i_1	i_0	√	√	√
ADC sfr,A	sfr,A←sfr+A+C	1	1	0	0	1	0	0	1	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADC ¥cur,A	cur,A←cur+A+C	1	1	0	0	1	1	0	1	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADC [HL],A	[HL],A←[HL]+A+C	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	1	√	√	—
ADC [XY],A	[XY],A←[XY]+A+C	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	1	1	√	√	—
ADC E:[HL],A	E:[HL],A←E:[HL]+A+C	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	√	√	—
ADC E:[XY],A	E:[XY],A←E:[XY]+A+C	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	1	√	√	—
ADC [HL+],A	[HL],A←[HL]+A+C, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0	1	1	√	√	√
ADC [XY+],A	[XY],A←[XY]+A+C, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	0	1	1	√	√	√
ADC E:[HL+],A	E:[HL],A←E:[HL]+A+C, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	1	1	√	√	√
ADC E:[XY+],A	E:[XY],A←E:[XY]+A+C, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	0	1	1	√	√	√

Arithmetic Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
ADCD sfr,A	sfr,A←decimal adjustment {sfr+A+C}	1	1	0	0	1	0	0	1	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADCD ¥cur,A	cur,A←decimal adjustment {cur+A+C}	1	1	0	0	1	1	0	1	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADCD [HL],A	[HL],A←decimal adjustment {[HL]+A+C}	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	1	0	0	√	√	—
ADCD [XY],A	[XY],A←decimal adjustment {[XY]+A+C}	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	1	0	0	√	√	—
ADCD E:[HL],A	E:[HL],A←decimal adjustment {E:[HL]+A+C}	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	√	√	—
ADCD E:[XY],A	E:[XY],A←decimal adjustment {E:[XY]+A+C}	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	0	√	√	—
ADCD [HL+],A	[HL],A←decimal adjustment {[HL]+A+C}, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	1	0	0	√	√	√
ADCD [XY+],A	[XY],A←decimal adjustment {[XY]+A+C}, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	0	0	√	√	√
ADCD E:[HL+],A	E:[HL],A←decimal adjustment {E:[HL]+A+C}, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	0	√	√	√
ADCD E:[XY+],A	E:[XY],A←decimal adjustment {E:[XY]+A+C}, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	0	√	√	√
ADCJ ¥cur,n	cur,A←n-ary adjustment {cur+C}	1	1	0	0	0	1	0	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADCJ [HL],n	[HL],A←n-ary adjustment {[HL]+C}	1	1	0	0	0	0	0	1	1	0	0	0	1	0	0	n_2	n_1	n_0	√	√	—
ADCJ [XY],n	[XY],A←n-ary adjustment {[XY]+C}	1	1	0	0	0	0	0	1	1	0	0	0	1	1	0	n_2	n_1	n_0	√	√	—
ADCJ E:[HL],n	E:[HL],A←n-ary adjustment {E:[HL]+C}	1	1	0	0	0	0	0	1	1	0	0	0	0	0	0	n_2	n_1	n_0	√	√	—
ADCJ E:[XY],n	E:[XY],A←n-ary adjustment {E:[XY]+C}	1	1	0	0	0	0	0	1	1	0	0	0	0	1	0	n_2	n_1	n_0	√	√	—
ADCJ [HL+],n	[HL],A←n-ary adjustment {[HL]+C},HL←HL+1	1	1	0	0	0	0	0	1	1	1	0	0	1	0	0	n_2	n_1	n_0	√	√	√
ADCJ [XY+],n	[XY],A←n-ary adjustment {[XY]+C},XY←XY+1	1	1	0	0	0	0	0	1	1	1	0	0	1	1	0	n_2	n_1	n_0	√	√	√
ADCJ E:[HL+],n	E:[HL],A←n-ary adjustment {E:[HL]+C},HL←HL+1	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0	n_2	n_1	n_0	√	√	√
ADCJ E:[XY+],n	E:[XY],A←n-ary adjustment {E:[XY]+C},XY←XY+1	1	1	0	0	0	0	0	1	1	1	0	0	0	1	0	n_2	n_1	n_0	√	√	√

Arithmetic Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
SUB sfr,A	sfr,A←sfr–A	1	1	0	0	1	0	0	1	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SUB ¥cur,A	cur,A←cur–A	1	1	0	0	1	1	0	1	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SUB [HL],A	[HL],A←[HL]–A	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	1	0	1	√	√	—
SUB [XY],A	[XY],A←[XY]–A	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	1	0	1	√	√	—
SUB E:[HL],A	E:[HL],A←E:[HL]–A	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	√	√	—
SUB E:[XY],A	E:[XY],A←E:[XY]–A	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	√	√	—
SUB [HL+],A	[HL],A←[HL]–A, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	1	0	1	√	√	√
SUB [XY+],A	[XY],A←[XY]–A, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	0	1	√	√	√
SUB E:[HL+],A	E:[HL],A←E:[HL]–A, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	√	√	√
SUB E:[XY+],A	E:[XY],A←E:[XY]–A, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	1	√	√	√
SUB ¥cur,#i4	cur,A←cur–i4	1	1	1	0	0	1	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SUB [HL],#i4	[HL],A←[HL]–i4	1	1	0	0	0	0	0	0	1	0	1	0	1	0	i_3	i_2	i_1	i_0	√	√	—
SUB [XY],#i4	[XY],A←[XY]–i4	1	1	0	0	0	0	0	0	1	0	1	0	1	1	i_3	i_2	i_1	i_0	√	√	—
SUB E:[HL],#i4	E:[HL],A←E:[HL]–i4	1	1	0	0	0	0	0	0	1	0	1	0	0	0	i_3	i_2	i_1	i_0	√	√	—
SUB E:[XY],#i4	E:[XY],A←E:[XY]–i4	1	1	0	0	0	0	0	0	1	0	1	0	0	1	i_3	i_2	i_1	i_0	√	√	—
SUB [HL+],#i4	[HL],A←[HL]–i4, HL←HL+1	1	1	0	0	0	0	0	0	1	1	1	0	1	0	i_3	i_2	i_1	i_0	√	√	√
SUB [XY+],#i4	[XY],A←[XY]–i4, XY←XY+1	1	1	0	0	0	0	0	0	1	1	1	0	1	1	i_3	i_2	i_1	i_0	√	√	√
SUB E:[HL+],#i4	E:[HL],A←E:[HL]–i4, HL←HL+1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	i_3	i_2	i_1	i_0	√	√	√
SUB E:[XY+],#i4	E:[XY],A←E:[XY]–i4, XY←XY+1	1	1	0	0	0	0	0	0	1	1	1	0	0	1	i_3	i_2	i_1	i_0	√	√	√
SBC sfr,A	sfr,A←sfr–A–C	1	1	0	0	1	0	1	0	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBC ¥cur,A	cur,A←cur–A–C	1	1	0	0	1	1	1	0	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBC [HL],A	[HL],A←[HL]–A–C	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	1	1	0	√	√	—
SBC [XY],A	[XY],A←[XY]–A–C	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	1	1	0	√	√	—
SBC E:[HL],A	E:[HL],A←E:[HL]–A–C	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	0	√	√	—
SBC E:[XY],A	E:[XY],A←E:[XY]–A–C	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	1	1	0	√	√	—
SBC [HL+],A	[HL],A←[HL]–A–C, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	1	1	0	√	√	√
SBC [XY+],A	[XY],A←[XY]–A–C, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	0	√	√	√
SBC E:[HL+],A	E:[HL],A←E:[HL]–A–C, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	1	1	0	√	√	√
SBC E:[XY+],A	E:[XY],A←E:[XY]–A–C, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	1	1	0	√	√	√

Arithmetic Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
SBCD sfr,A	sfr,A←decimal adjustment {sfr–A–C}	1	1	0	0	1	0	1	0	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBCD ¥cur,A	cur,A←decimal adjustment {cur–A–C}	1	1	0	0	1	1	1	0	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBCD [HL],A	[HL],A←decimal adjustment {[HL]–A–C}	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	1	1	1	√	√	—
SBCD [XY],A	[XY],A←decimal adjustment {[XY]–A–C}	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	1	1	1	√	√	—
SBCD E:[HL],A	E:[HL],A←decimal adjustment {E:[HL]–A–C}	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	1	√	√	—
SBCD E:[XY],A	E:[XY],A←decimal adjustment {E:[XY]–A–C}	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	1	1	1	√	√	—
SBCD [HL+],A	[HL],A←decimal adjustment {[HL]–A–C}, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	1	1	1	√	√	√
SBCD [XY+],A	[XY],A←decimal adjustment {[XY]–A–C}, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	1	√	√	√
SBCD E:[HL+],A	E:[HL],A←decimal adjustment {E:[HL]–A–C}, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	1	1	1	√	√	√
SBCD E:[XY+],A	E:[XY],A←decimal adjustment {E:[XY]–A–C}, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	1	1	1	√	√	√
SBCJ ¥cur,n	cur,A←n-ary adjustment {cur–C}	1	1	0	0	0	1	1	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBCJ [HL],n	[HL],A←n-ary adjustment {[HL]–C}	1	1	0	0	0	0	0	1	1	0	0	0	1	0	1	n_2	n_1	n_0	√	√	—
SBCJ [XY],n	[XY],A←n-ary adjustment {[XY]–C}	1	1	0	0	0	0	0	1	1	0	0	0	1	1	1	n_2	n_1	n_0	√	√	—
SBCJ E:[HL],n	E:[HL],A←n-ary adjustment {E:[HL]–C}	1	1	0	0	0	0	0	1	1	0	0	0	0	0	1	n_2	n_1	n_0	√	√	—
SBCJ E:[XY],n	E:[XY],A←n-ary adjustment {E:[XY]–C}	1	1	0	0	0	0	0	1	1	0	0	0	0	1	1	n_2	n_1	n_0	√	√	—
SBCJ [HL+],n	[HL],A←n-ary adjustment {[HL]–C},HL←HL+1	1	1	0	0	0	0	0	1	1	1	0	0	1	0	1	n_2	n_1	n_0	√	√	√
SBCJ [XY+],n	[XY],A←n-ary adjustment {[XY]–C},XY←XY+1	1	1	0	0	0	0	0	1	1	1	0	0	1	1	1	n_2	n_1	n_0	√	√	√
SBCJ E:[HL+],n	E:[HL],A←n-ary adjustment {E:[HL]–C},HL←HL+1	1	1	0	0	0	0	0	1	1	1	0	0	0	0	1	n_2	n_1	n_0	√	√	√
SBCJ E:[XY+],n	E:[XY],A←n-ary adjustment {E:[XY]–C},XY←XY+1	1	1	0	0	0	0	0	1	1	1	0	0	0	1	1	n_2	n_1	n_0	√	√	√

Compare Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
CMP sfr,A	sfr–A	1	1	0	0	1	0	1	0	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
CMP ¥cur,A	cur–A	1	1	0	0	1	1	1	0	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
CMP [HL],A	[HL]–A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	√	√	—
CMP [XY],A	[XY]–A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	1	0	0	√	√	—
CMP E:[HL],A	E:[HL]–A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	√	√	—
CMP E:[XY],A	E:[XY]–A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	√	√	—
CMP [HL+],A	[XY]–A,HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1	0	0	√	√	√
CMP [XY+],A	[XY]–A,XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0	0	√	√	√
CMP E:[HL+],A	E:[HL]–A,HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	√	√	√
CMP E:[XY+],A	E:[XY]–A,XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	0	√	√	√
CMP ¥cur,#i4	cur–i4	1	1	1	0	1	0	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
CMP [HL],#i4	[HL]–i4	1	1	0	0	0	0	0	1	1	0	1	0	1	0	i_3	i_2	i_1	i_0	√	√	—
CMP [XY],#i4	[XY]–i4	1	1	0	0	0	0	0	1	1	0	1	0	1	1	i_3	i_2	i_1	i_0	√	√	—
CMP E:[HL],#i4	E:[HL]–i4	1	1	0	0	0	0	0	1	1	0	1	0	0	0	i_3	i_2	i_1	i_0	√	√	—
CMP E:[XY],#i4	E:[XY]–i4	1	1	0	0	0	0	0	1	1	0	1	0	0	1	i_3	i_2	i_1	i_0	√	√	—
CMP [HL+],#i4	[HL]–i4,HL←HL+1	1	1	0	0	0	0	0	1	1	1	1	0	1	0	i_3	i_2	i_1	i_0	√	√	√
CMP [XY+],#i4	[XY]–i4,XY←XY+1	1	1	0	0	0	0	0	1	1	1	1	0	1	1	i_3	i_2	i_1	i_0	√	√	√
CMP E:[HL+],#i4	E:[HL]–i4,HL←HL+1	1	1	0	0	0	0	0	1	1	1	1	0	0	0	i_3	i_2	i_1	i_0	√	√	√
CMP E:[XY+],#i4	E:[XY]–i4,XY←XY+1	1	1	0	0	0	0	0	1	1	1	1	0	0	1	i_3	i_2	i_1	i_0	√	√	√

Logic Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
AND sfr,A	sfr,A←sfr ∧ A	1	1	0	0	1	0	1	0	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
AND ¥cur,A	cur,A←cur ∧ A	1	1	0	0	1	1	1	0	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
AND [HL],A	[HL],A←[HL] ∧ A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	√	—	—
AND [XY],A	[XY],A←[XY] ∧ A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	1	√	—	—
AND E:[HL],A	E:[HL],A←E:[HL] ∧ A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	√	—	—
AND E:[XY],A	E:[XY],A←E:[XY] ∧ A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	√	—	—
AND [HL+],A	[HL],A←[HL] ∧ A, HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	0	0	1	√	—	√
AND [XY+],A	[XY],A←[XY] ∧ A, XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	1	√	—	√
AND E:[HL+],A	E:[HL],A←E:[HL] ∧ A, HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	√	—	√
AND E:[XY+],A	E:[XY],A←E:[XY] ∧ A, XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	1	√	—	√
AND ¥cur,#i4	cur,A←cur ∧ i4	1	1	0	1	0	1	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
AND [HL],#i4	[HL],A←[HL] ∧ i4	1	1	0	0	0	0	0	1	0	0	0	1	1	0	i_3	i_2	i_1	i_0	√	—	—
AND [XY],#i4	[XY],A←[XY] ∧ i4	1	1	0	0	0	0	0	1	0	0	0	1	1	1	i_3	i_2	i_1	i_0	√	—	—
AND E:[HL],#i4	E:[HL],A←E:[HL] ∧ i4	1	1	0	0	0	0	0	1	0	0	0	1	0	0	i_3	i_2	i_1	i_0	√	—	—
AND E:[XY],#i4	E:[XY],A←E:[XY] ∧ i4	1	1	0	0	0	0	0	1	0	0	0	1	0	1	i_3	i_2	i_1	i_0	√	—	—
AND [HL+],#i4	[HL],A←[HL] ∧ i4, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	1	1	0	i_3	i_2	i_1	i_0	√	—	√
AND [XY+],#i4	[XY],A←[XY] ∧ i4, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	1	1	1	i_3	i_2	i_1	i_0	√	—	√
AND E:[HL+],#i4	E:[HL],A←E:[HL] ∧ i4, HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	1	0	0	i_3	i_2	i_1	i_0	√	—	√
AND E:[XY+],#i4	E:[XY],A←E:[XY] ∧ i4, XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	1	0	1	i_3	i_2	i_1	i_0	√	—	√
OR sfr,A	sfr,A←sfr ∨ A	1	1	0	0	1	0	1	1	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
OR ¥cur,A	cur,A←cur ∨ A	1	1	0	0	1	1	1	1	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
OR [HL],A	[HL],A←[HL] ∨ A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	0	√	—	—
OR [XY],A	[XY],A←[XY] ∨ A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1	0	√	—	—
OR E:[HL],A	E:[HL],A←E:[HL] ∨ A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	√	—	—
OR E:[XY],A	E:[XY],A←E:[XY] ∨ A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	√	—	—
OR [HL+],A	[HL],A←[HL] ∨ A, HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	0	1	0	√	—	√
OR [XY+],A	[XY],A←[XY] ∨ A, XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	0	1	0	√	—	√
OR E:[HL+],A	E:[HL],A←E:[HL] ∨ A, HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	√	—	√
OR E:[XY+],A	E:[XY],A←E:[XY] ∨ A, XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	1	0	√	—	√

Logic Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
OR ¥cur,#i4	cur,A←cur ∨ i4	1	1	0	1	1	0	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
OR [HL],#i4	[HL],A←[HL] ∨ i4	1	1	0	0	0	0	0	0	1	0	0	1	1	0	i_3	i_2	i_1	i_0	√	—	—
OR [XY],#i4	[XY],A←[XY] ∨ i4	1	1	0	0	0	0	0	0	1	0	0	1	1	1	i_3	i_2	i_1	i_0	√	—	—
OR E:[HL],#i4	E:[HL],A←E:[HL] ∨ i4	1	1	0	0	0	0	0	0	1	0	0	1	0	0	i_3	i_2	i_1	i_0	√	—	—
OR E:[XY],#i4	E:[XY],A←E:[XY] ∨ i4	1	1	0	0	0	0	0	0	1	0	0	1	0	1	i_3	i_2	i_1	i_0	√	—	—
OR [HL+],#i4	[HL],A←[HL] ∨ i4, HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	i_3	i_2	i_1	i_0	√	—	√
OR [XY+],#i4	[XY],A←[XY] ∨ i4, XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	1	1	1	i_3	i_2	i_1	i_0	√	—	√
OR E:[HL+],#i4	E:[HL],A←E:[HL] ∨ i4, HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	1	0	0	i_3	i_2	i_1	i_0	√	—	√
OR E:[XY+],#i4	E:[XY],A←E:[XY] ∨ i4, XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	1	0	1	i_3	i_2	i_1	i_0	√	—	√
XOR sfr,A	sfr,A←sfr∀A	1	1	0	0	1	0	1	1	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
XOR ¥cur,A	cur,A←cur∀A	1	1	0	0	1	1	1	1	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
XOR [HL],A	[HL],A←[HL]∀A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	1	√	—	—
XOR [XY],A	[XY],A←[XY]∀A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1	1	√	—	—
XOR E:[HL],A	E:[HL],A←E:[HL]∀A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	√	—	—
XOR E:[XY],A	E:[XY],A←E:[XY]∀A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1	√	—	—
XOR [HL+],A	[HL],A←[HL]∀A,HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	0	1	1	√	—	√
XOR [XY+],A	[XY],A←[XY]∀A,XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	0	1	1	√	—	√
XOR E:[HL+],A	E:[HL],A←E:[HL]∀A, HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	1	√	—	√
XOR E:[XY+],A	E:[XY],A←E:[XY]∀A, XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	1	1	√	—	√
XOR ¥cur,#i4	cur,A←cur∀i4	1	1	0	1	1	1	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
XOR [HL],#i4	[HL],A←[HL]∀i4	1	1	0	0	0	0	0	0	0	0	0	1	1	0	i_3	i_2	i_1	i_0	√	—	—
XOR [XY],#i4	[XY],A←[XY]∀i4	1	1	0	0	0	0	0	0	0	0	0	1	1	1	i_3	i_2	i_1	i_0	√	—	—
XOR E:[HL],#i4	E:[HL],A←E:[HL]∀i4	1	1	0	0	0	0	0	0	0	0	0	1	0	0	i_3	i_2	i_1	i_0	√	—	—
XOR E:[XY],#i4	E:[XY],A←E:[XY]∀i4	1	1	0	0	0	0	0	0	0	0	0	1	0	1	i_3	i_2	i_1	i_0	√	—	—
XOR [HL+],#i4	[HL],A←[HL]∀i4, HL←HL+1	1	1	0	0	0	0	0	0	0	1	0	1	1	0	i_3	i_2	i_1	i_0	√	—	√
XOR [XY+],#i4	[XY],A←[XY]∀i4, XY←XY+1	1	1	0	0	0	0	0	0	0	1	0	1	1	1	i_3	i_2	i_1	i_0	√	—	√
XOR E:[HL+],#i4	E:[HL],A←E:[HL]∀i4, HL←HL+1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	i_3	i_2	i_1	i_0	√	—	√
XOR E:[XY+],#i4	E:[XY],A←E:[XY]∀i4, XY←XY+1	1	1	0	0	0	0	0	0	0	1	0	1	0	1	i_3	i_2	i_1	i_0	√	—	√

Mask Operation Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MTST sfr,A	Testing of all bits in sfr not masked by A	1	1	0	0	1	0	1	1	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MTST ¥cur,A	Testing of all bits in cur not masked by A	1	1	0	0	1	1	1	1	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MTST [HL],A	Testing of all bits in [HL] not masked by A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	1	√	—	—
MTST [XY],A	Testing of all bits in [XY] not masked by A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	1	0	1	√	—	—
MTST E:[HL],A	Testing of all bits in E:[HL]not masked by A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	√	—	—
MTST E:[XY],A	Testing of all bits in E:[XY]not masked by A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	√	—	—
MTST [HL+],A	Testing of all bits in [HL] not masked by A, HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1	0	1	√	—	√
MTST [XY+],A	Testing of all bits in [XY] not masked by A, XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0	1	√	—	√
MTST E:[HL+],A	Testing of all bits in E:[HL] not masked by A, HL←HL+1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	√	—	√
MTST E:[XY+],A	Testing of all bits in E:[XY] not masked by A, XY←XY+1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	1	√	—	√
MTST ¥cur,#m	Testing of bits in cur not masked by #m	1	1	1	0	1	1	m_3	m_2	m_1	m_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MTST [HL],#m	Testing of all bits in [HL] not masked by #m	1	1	0	0	0	0	0	1	0	0	1	0	1	0	m_3	m_2	m_1	m_0	√	—	—
MTST [XY],#m	Testing of all bits in [XY] not masked by #m	1	1	0	0	0	0	0	1	0	0	1	0	1	1	m_3	m_2	m_1	m_0	√	—	—
MTST E:[HL],#m	Testing of all bits in E:[HL] not masked by #m	1	1	0	0	0	0	0	1	0	0	1	0	0	0	m_3	m_2	m_1	m_0	√	—	—
MTST E:[XY],#m	Testing of all bits in E:[XY] not masked by #m	1	1	0	0	0	0	0	1	0	0	1	0	0	1	m_3	m_2	m_1	m_0	√	—	—
MTST [HL+],#m	Testing of all bits in [HL] not masked by #m, HL←HL+1	1	1	0	0	0	0	0	1	0	1	1	0	1	0	m_3	m_2	m_1	m_0	√	—	√
MTST [XY+],#m	Testing of all bits in [XY] not masked by #m, XY←XY+1	1	1	0	0	0	0	0	1	0	1	1	0	1	1	m_3	m_2	m_1	m_0	√	—	√
MTST E:[HL+], #m	Testing of all bits in E:[HL] not masked by #m, HL←HL+1	1	1	0	0	0	0	0	1	0	1	1	0	0	0	m_3	m_2	m_1	m_0	√	—	√
MTST E:[XY+], #m	Testing of all bits in E:[XY] not masked by #m, XY←XY+1	1	1	0	0	0	0	0	1	0	1	1	0	0	1	m_3	m_2	m_1	m_0	√	—	√

Mask Operation Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MCLR ¥cur,#m	Clearing of all bits in cur not masked by #m, A←cur	1	1	0	1	0	1	m_3	m_2	m_1	m_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MCLR [HL],#m	Clearing of all bits in [HL] not masked by #m, A←[HL]	1	1	0	0	0	0	0	1	0	0	0	1	1	0	m_3	m_2	m_1	m_0	√	—	—
MCLR [XY],#m	Clearing of all bits in [XY] not masked by #m, A←[XY]	1	1	0	0	0	0	0	1	0	0	0	1	1	1	m_3	m_2	m_1	m_0	√	—	—
MCLR E:[HL],#m	Clearing of all bits in E:[HL] not masked by #m, A←E:[HL]	1	1	0	0	0	0	0	1	0	0	0	1	0	0	m_3	m_2	m_1	m_0	√	—	—
MCLR E:[XY],#m	Clearing of all bits in E:[XY] not masked by #m, A←E:[XY]	1	1	0	0	0	0	0	1	0	0	0	1	0	1	m_3	m_2	m_1	m_0	√	—	—
MCLR [HL+],#m	Clearing of all bits in [HL] not masked by #m,A←[HL],HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	1	1	0	m_3	m_2	m_1	m_0	√	—	√
MCLR [XY+],#m	Clearing of all bits in [XY] not masked by #m,A←[XY],XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	1	1	1	m_3	m_2	m_1	m_0	√	—	√
MCLR E:[HL+], #m	Clearing of all bits in E:[HL] not masked by #m,A←E:[HL],HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	1	0	0	m_3	m_2	m_1	m_0	√	—	√
MCLR E:[XY+], #m	Clearing of all bits in E:[XY] not masked by #m,A←E:[XY],XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	1	0	1	m_3	m_2	m_1	m_0	√	—	√

Mask Operation Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MSET ¥cur,#m	Setting of all bits in cur not masked by #m, A←cur	1	1	0	1	1	0	m_3	m_2	m_1	m_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MSET [HL],#m	Setting of all bits in [HL] not masked by #m, A←[HL]	1	1	0	0	0	0	0	0	1	0	0	1	1	0	m_3	m_2	m_1	m_0	√	—	—
MSET [XY],#m	Setting of all bits in [XY] not masked by #m, A←[XY]	1	1	0	0	0	0	0	0	1	0	0	1	1	1	m_3	m_2	m_1	m_0	√	—	—
MSET E:[HL],#m	Setting of all bits in E: [HL] not masked by #m, A←E:[HL]	1	1	0	0	0	0	0	0	1	0	0	1	0	0	m_3	m_2	m_1	m_0	√	—	—
MSET E:[XY],#m	Setting of all bits in E: [XY] not masked by #m, A←E:[XY]	1	1	0	0	0	0	0	0	1	0	0	1	0	1	m_3	m_2	m_1	m_0	√	—	—
MSET [HL+],#m	Setting of all bits in [HL] not masked by #m, A←[HL],HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	m_3	m_2	m_1	m_0	√	—	√
MSET [XY+],#m	Setting of all bits in [XY] not masked by #m, A←[XY],XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	1	1	1	m_3	m_2	m_1	m_0	√	—	√
MSET E:[HL+], #m	Setting of all bits in E: [HL] not masked by #m, A←E:[HL],HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	1	0	0	m_3	m_2	m_1	m_0	√	—	√
MSET E:[XY+], #m	Setting of all bits in E: [XY] not masked by #m, A←E:[XY],XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	1	0	1	m_3	m_2	m_1	m_0	√	—	√

Mask Operation Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MNOT ¥cur,#m	Inverting of all bits in cur not masked by #m, A←cur	1	1	0	1	1	1	m_3	m_2	m_1	m_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MNOT [HL],#m	Inverting of all bits in [HL] not masked by #m, A←[HL]	1	1	0	0	0	0	0	0	0	0	0	1	1	0	m_3	m_2	m_1	m_0	√	—	—
MNOT [XY],#m	Inverting of all bits in [XY] not masked by #m, A←[XY]	1	1	0	0	0	0	0	0	0	0	0	1	1	1	m_3	m_2	m_1	m_0	√	—	—
MNOT E:[HL],#m	Inverting of all bits in E:[HL] not masked by #m, A←E:[HL]	1	1	0	0	0	0	0	0	0	0	0	1	0	0	m_3	m_2	m_1	m_0	√	—	—
MNOT E:[XY],#m	Inverting of all bits in E:[XY] not masked by #m, A←E:[XY]	1	1	0	0	0	0	0	0	0	0	0	1	0	1	m_3	m_2	m_1	m_0	√	—	—
MNOT [HL+],#m	Inverting of all bits in [HL] not masked by #m, A←[HL],HL←HL+1	1	1	0	0	0	0	0	0	0	1	0	1	1	0	m_3	m_2	m_1	m_0	√	—	√
MNOT [XY+],#m	Inverting of all bits in [XY] not masked by #m, A←[XY],XY←XY+1	1	1	0	0	0	0	0	0	0	1	0	1	1	1	m_3	m_2	m_1	m_0	√	—	√
MNOT E:[HL+], #m	Inverting of all bits in E:[HL] not masked by #m, A←E:[HL],HL←HL+1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	m_3	m_2	m_1	m_0	√	—	√
MNOT E:[XY+], #m	Inverting of all bits in E:[XY] not masked by #m, A←E:[XY],XY←XY+1	1	1	0	0	0	0	0	0	0	1	0	1	0	1	m_3	m_2	m_1	m_0	√	—	√

Bit Operation Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
BTST ¥cur.n	Bit testing of cur.n	1	1	1	0	1	1	n_3	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
BTST [HL].n	Bit testing of [HL].n	1	1	0	0	0	0	0	1	0	0	1	0	1	0	n_3	n_2	n_1	n_0	√	—	—
BTST [XY].n	Bit testing of [XY].n	1	1	0	0	0	0	0	1	0	0	1	0	1	1	n_3	n_2	n_1	n_0	√	—	—
BTST E:[HL].n	Bit testing of E:[HL].n	1	1	0	0	0	0	0	1	0	0	1	0	0	0	n_3	n_2	n_1	n_0	√	—	—
BTST E:[XY].n	Bit testing of E:[XY].n	1	1	0	0	0	0	0	1	0	0	1	0	0	1	n_3	n_2	n_1	n_0	√	—	—
BTST [HL+].n	Bit testing of [HL].n, HL←HL+1	1	1	0	0	0	0	0	1	0	1	1	0	1	0	n_3	n_2	n_1	n_0	√	—	√
BTST [XY+].n	Bit testing of [XY].n, XY←XY+1	1	1	0	0	0	0	0	1	0	1	1	0	1	1	n_3	n_2	n_1	n_0	√	—	√
BTST E:[HL+].n	Bit testing of E:[HL].n, HL←HL+1	1	1	0	0	0	0	0	1	0	1	1	0	0	0	n_3	n_2	n_1	n_0	√	—	√
BTST E:[XY+].n	Bit testing of E:[XY].n, XY←XY+1	1	1	0	0	0	0	0	1	0	1	1	0	0	1	n_3	n_2	n_1	n_0	√	—	√
BCLR ¥cur.n	cur.n←0,A←cur	1	1	0	1	0	1	n_3	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
BCLR [HL].n	[HL].n←0,A←[HL]	1	1	0	0	0	0	0	1	0	0	0	1	1	0	n_3	n_2	n_1	n_0	√	—	—
BCLR [XY].n	[XY].n←0,A←[XY]	1	1	0	0	0	0	0	1	0	0	0	1	1	1	n_3	n_2	n_1	n_0	√	—	—
BCLR E:[HL].n	E:[HL].n←0,A←E:[HL]	1	1	0	0	0	0	0	1	0	0	0	1	0	0	n_3	n_2	n_1	n_0	√	—	—
BCLR E:[XY].n	E:[XY].n←0,A←E:[XY]	1	1	0	0	0	0	0	1	0	0	0	1	0	1	n_3	n_2	n_1	n_0	√	—	—
BCLR [HL+].n	[HL].n←0,A←[HL], HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	1	1	0	n_3	n_2	n_1	n_0	√	—	√
BCLR [XY+].n	[XY].n←0,A←[XY], XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	1	1	1	n_3	n_2	n_1	n_0	√	—	√
BCLR E:[HL+].n	E:[HL].n←0,A←E:[HL], HL←HL+1	1	1	0	0	0	0	0	1	0	1	0	1	0	0	n_3	n_2	n_1	n_0	√	—	√
BCLR E:[XY+].n	E:[XY].n←0,A←E:[XY], XY←XY+1	1	1	0	0	0	0	0	1	0	1	0	1	0	1	n_3	n_2	n_1	n_0	√	—	√
BSET ¥cur.n	cur.n←1,A←cur	1	1	0	1	1	0	n_3	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
BSET [HL].n	[HL].n←1,A←[HL]	1	1	0	0	0	0	0	0	1	0	0	1	1	0	n_3	n_2	n_1	n_0	√	—	—
BSET [XY].n	[XY].n←1,A←[XY]	1	1	0	0	0	0	0	0	1	0	0	1	1	1	n_3	n_2	n_1	n_0	√	—	—
BSET E:[HL].n	E:[HL].n←1,A←E:[HL]	1	1	0	0	0	0	0	0	1	0	0	1	0	0	n_3	n_2	n_1	n_0	√	—	—
BSET E:[XY].n	E:[XY].n←1,A←E:[XY]	1	1	0	0	0	0	0	0	1	0	0	1	0	1	n_3	n_2	n_1	n_0	√	—	—
BSET [HL+].n	[HL].n←1,A←[HL], HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	n_3	n_2	n_1	n_0	√	—	√
BSET [XY+].n	[XY].n←1,A←[XY], XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	1	1	1	n_3	n_2	n_1	n_0	√	—	√
BSET E:[HL+].n	E:[HL].n←1,A←E:[HL], HL←HL+1	1	1	0	0	0	0	0	0	1	1	0	1	0	0	n_3	n_2	n_1	n_0	√	—	√
BSET E:[XY+].n	E:[XY].n←1,A←E:[XY], XY←XY+1	1	1	0	0	0	0	0	0	1	1	0	1	0	1	n_3	n_2	n_1	n_0	√	—	√

Bit Operation Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
BNOT ¥cur.n	cur.n←$\overline{\text{cur.n}}$,A←cur	1	1	0	1	1	1	n_3	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
BNOT [HL].n	[HL].n←$\overline{\text{[HL].n}}$,A←[HL]	1	1	0	0	0	0	0	0	0	0	0	1	1	0	n_3	n_2	n_1	n_0	√	—	—
BNOT [XY].n	[XY].n←$\overline{\text{[XY].n}}$,A←[XY]	1	1	0	0	0	0	0	0	0	0	0	1	1	1	n_3	n_2	n_1	n_0	√	—	—
BNOT E:[HL].n	E:[HL].n←$\overline{\text{E:[HL].n}}$,A←E:[HL]	1	1	0	0	0	0	0	0	0	0	0	1	0	0	n_3	n_2	n_1	n_0	√	—	—
BNOT E:[XY].n	E:[XY].n←$\overline{\text{E:[XY].n}}$,A←E:[XY]	1	1	0	0	0	0	0	0	0	0	0	1	0	1	n_3	n_2	n_1	n_0	√	—	—
BNOT [HL+].n	[HL].n←$\overline{\text{[HL].n}}$,A←[HL], HL←HL+1	1	1	0	0	0	0	0	0	0	1	0	1	1	0	n_3	n_2	n_1	n_0	√	—	√
BNOT [XY+].n	[XY].n←$\overline{\text{[XY].n}}$,A←[XY], XY←XY+1	1	1	0	0	0	0	0	0	0	1	0	1	1	1	n_3	n_2	n_1	n_0	√	—	√
BNOT E:[HL+].n	E:[HL].n←$\overline{\text{E:[HL].n}}$,A←E:[HL],HL←HL+1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	n_3	n_2	n_1	n_0	√	—	√
BNOT E:[XY+].n	E:[XY].n←$\overline{\text{E:[XY].n}}$,A←E:[XY],XY←XY+1	1	1	0	0	0	0	0	0	0	1	0	1	0	1	n_3	n_2	n_1	n_0	√	—	√

ROM Table Reference Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MOVHB [HL], [RA]	[HL],[HL+1]←$(RA)_{15-8}$	1	2	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	0	—	—	—
MOVHB [XY], [RA]	[XY],[XY+1]←$(RA)_{15-8}$	1	2	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	0	—	—	—
MOVHB E:[HL], [RA]	E:[HL],E:[HL+1]←$(RA)_{15-8}$	1	2	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	—	—	—
MOVHB E:[XY], [RA]	E:[XY],E:[XY+1]←$(RA)_{15-8}$	1	2	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	0	—	—	—
MOVHB [HL+], [RA]	[HL],[HL+1]←$(RA)_{15-8}$, HL←HL+2	1	2	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1	0	—	—	√
MOVHB [XY+], [RA]	[XY],[XY+1]←$(RA)_{15-8}$, XY←XY+2	1	2	0	0	0	0	0	0	1	1	0	0	1	1	1	0	1	0	—	—	√
MOVHB E:[HL+], [RA]	E:[HL],E:[HL+1]←$(RA)_{15-8}$,HL←HL+2	1	2	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	—	—	√
MOVHB E:[XY+], [RA]	E:[XY],E:[XY+1]←$(RA)_{15-8}$,XY←XY+2	1	2	0	0	0	0	0	0	1	1	0	0	0	1	1	0	1	0	—	—	√
MOVHB [HL], cadr16	[HL],[HL+1]←$(cadr16)_{15-8}$	2	3	0	0	0	0	0	0	1	1	0	0	1	0	0	1	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB [XY], cadr16	[XY],[XY+1]←$(cadr16)_{15-8}$	2	3	0	0	0	0	0	0	1	1	0	0	1	1	0	1	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB E:[HL], cadr16	E:[HL],E:[HL+1]←$(cadr16)_{15-8}$	2	3	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB E:[XY], cadr16	E:[XY],E:[XY+1]←$(cadr16)_{15-8}$	2	3	0	0	0	0	0	0	1	1	0	0	0	1	0	1	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB [HL+], cadr16	[HL],[HL+1]←$(cadr16)_{15-8}$,HL←HL+2	2	3	0	0	0	0	0	0	1	1	0	0	1	0	1	1	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB [XY+], cadr16	[XY],[XY+1]←$(cadr16)_{15-8}$,XY←XY+2	2	3	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB E:[HL+], cadr16	E:[HL],E:[HL+1]←$(cadr16)_{15-8}$,HL←HL+2	2	3	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB E:[XY+], cadr16	E:[XY],E:[XY+1]←$(cadr16)_{15-8}$,XY←XY+2	2	3	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			

ROM Table Reference Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MOVLB [HL], [RA]	[HL],[HL+1]←$(RA)_{7-0}$	1	2	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	1	—	—	—
MOVLB [XY], [RA]	[XY],[XY+1]←$(RA)_{7-0}$	1	2	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	—	—	—
MOVLB E:[HL], [RA]	E:[HL],E:[HL+1]←$(RA)_{7-0}$	1	2	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	—	—	—
MOVLB E:[XY], [RA]	E:[XY],E:[XY+1]←$(RA)_{7-0}$	1	2	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	1	—	—	—
MOVLB [HL+], [RA]	[HL],[HL+1]←$(RA)_{7-0}$, HL←HL+2	1	2	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1	1	—	—	√
MOVLB [XY+], [RA]	[XY],[XY+1]←$(RA)_{7-0}$, XY←XY+2	1	2	0	0	0	0	0	0	1	1	0	0	1	1	1	0	1	1	—	—	√
MOVLB E:[HL+], [RA]	E:[HL],E:[HL+1]←$(RA)_{7-0}$,HL←HL+2	1	2	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	1	—	—	√
MOVLB E:[XY+], [RA]	E:[XY],E:[XY+1]←$(RA)_{7-0}$,XY←XY+2	1	2	0	0	0	0	0	0	1	1	0	0	0	1	1	0	1	1	—	—	√
MOVLB [HL], cadr16	[HL],[HL+1]←$(cadr16)_{7-0}$	2	3	0	0	0	0	0	0	1	1	0	0	1	0	0	1	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB [XY], cadr16	[XY],[XY+1]←$(cadr16)_{7-0}$	2	3	0	0	0	0	0	0	1	1	0	0	1	1	0	1	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB E:[HL], cadr16	E:[HL],E:[HL+1]←$(cadr16)_{7-0}$	2	3	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB E:[XY], cadr16	E:[XY],E:[XY+1]←$(cadr16)_{7-0}$	2	3	0	0	0	0	0	0	1	1	0	0	0	1	0	1	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB [HL+], cadr16	[HL],[HL+1]←$(cadr16)_{7-0}$,HL←HL+2	2	3	0	0	0	0	0	0	1	1	0	0	1	0	1	1	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB [XY+], cadr16	[XY],[XY+1]←$(cadr16)_{7-0}$,XY←XY+2	2	3	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB E:[HL+], cadr16	E:[HL],E:[HL+1]←$(cadr16)_{7-0}$,HL←HL+2	2	3	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB E:[XY+], cadr16	E:[XY],E:[XY+1]←$(cadr16)_{7-0}$,XY←XY+2	2	3	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			

Stack Operation Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
PUSH HL	(RSP)←{FLAG,A,HL}, RSP←RSP+1	1	2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	—	—	—
PUSH XY	(RSP)←{CBR,EBR,XY}, RSP←RSP+1	1	2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	—	—	—
POP HL	RSP←RSP−1, {FLAG,A,HL}←(RSP)	1	2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	√	√	√
POP XY	RSP←RSP−1, {CBR,EBR,XY}←(RSP)	1	2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	—	—	—

Flag Operation Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
FCLR G	G←0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	—	—	√
FCLR C	C←0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	—	√	—
FCLR Z	Z←0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	√	—	—
FSET G	G←1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	—	—	√
FSET C	C←1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	—	√	—
FSET Z	Z←1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	√	—	—

Jump Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
LJMP cadr15	PC←cadr15	2	2	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	—	—	—
				0	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
JMP cadr12	$PC_{11\sim0}$←cadr12	1	1	1	1	1	0	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
SJMP radr8	PC←Next PC+radr8	1	1	0	0	0	0	1	0	0	a_7	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
JMP PC+A	PC←PC+A+1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	—	—	—

Conditional Branch Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
BC radr8 BLT radr8	if C=1 then PC←Next PC+radr8(<)	1	1	0	0	0	0	1	0	1	a_7	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BNC radr8 BGE radr8	if C=0 then PC←Next PC+radr8(≧)	1	1	0	0	0	0	1	0	1	a_7	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BZ radr8 BEQ radr8	if Z=1 then PC←Next PC+radr8(=)	1	1	0	0	0	0	1	1	0	a_7	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BNZ radr8 BNE radr8	if Z=0 then PC←Next PC+radr8(≠)	1	1	0	0	0	0	1	1	0	a_7	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BLE radr8	if (C=1) ∨ (Z=1) then PC←Next PC+radr8(≦)	1	1	0	0	0	0	1	1	1	a_7	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BGT radr8	if (C=0) ∧ (Z=0) then PC←Next PC+radr8(>)	1	1	0	0	0	0	1	1	1	a_7	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BNG radr8	if G=0 then PC←Next PC+radr8	1	1	0	0	0	0	1	0	0	a_7	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—

Call/Return Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
LCAL cadr15	(SP)←PC,PC←cadr15, SP←SP+1	2	2	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	—	—	—
				0	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
CAL cadr12	(SP)←PC,PC_{11-0}←cadr12,SP←SP+1	1	1	1	1	1	1	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
RT	PC←(SP)+1,SP←SP–1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	—	—	—
RTI	PC←(SP)+1,SP←SP–1, MIE←1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	—	—	—
RTNMI	PC←(SP)+1,SP←SP–1 MIE←status of MIE before an interrupt occurs	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	—	—	—

Control Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
NOP	NO OPERATION	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—
HALT	HALT CPU	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	—	—	—
EI	MIE←1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	—	—	—
DI	MIE←0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	—	—	—
INCB HL	HL←HL+1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	—	—	√
INCB XY	XY←XY+1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	—	—	√
INCW RA	RA←RA+1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	—	—	√
MOV CBR,#i4	CBR←i4	1	1	0	0	0	0	0	0	0	0	0	0	1	1	i_3	i_2	i_1	i_0	—	—	—
MOV EBR,#i4	EBR←i4	1	1	0	0	0	0	0	0	0	0	0	0	1	0	i_3	i_2	i_1	i_0	—	—	—
MOV RA0,#i4	RA0←i4	1	1	0	0	0	0	0	0	1	0	0	0	0	0	i_3	i_2	i_1	i_0	—	—	—
MOV RA1,#i4	RA1←i4	1	1	0	0	0	0	0	0	1	0	0	0	0	1	i_3	i_2	i_1	i_0	—	—	—
MOV RA2,#i4	RA2←i4	1	1	0	0	0	0	0	0	1	0	0	0	1	0	i_3	i_2	i_1	i_0	—	—	—
MOV RA3,#i4	RA3←i4	1	1	0	0	0	0	0	0	1	0	0	0	1	1	i_3	i_2	i_1	i_0	—	—	—
MOV H,#i4	H←i4	1	1	0	0	0	0	0	0	0	1	0	0	1	1	i_3	i_2	i_1	i_0	—	—	—
MOV L,#i4	L←i4	1	1	0	0	0	0	0	0	0	1	0	0	1	0	i_3	i_2	i_1	i_0	—	—	—
MOV X,#i4	X←i4	1	1	0	0	0	0	0	0	0	1	0	0	0	1	i_3	i_2	i_1	i_0	—	—	—
MOV Y,#i4	Y←i4	1	1	0	0	0	0	0	0	0	1	0	0	0	0	i_3	i_2	i_1	i_0	—	—	—
MSA cadr15	Melody output starts	2	3	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	—	—	—
				0	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			

Appendix G Mask Option

In the ML63187, ML63189B, and ML63193, use the mask option to specify the following functions:

- Low-speed clock oscillation circuit
  Specify the crystal oscillation circuit or the RC oscillation circuit for the low-speed clock oscillation circuit.
- Reset signal sampling
  Specify whether or not the reset signal will be sampled at 2 kHz.
  When specifying "will carry out 2 kHz sampling," hold the RESET pin at a "H" level for 1 ms or more.

To use the mask option, assign mask option data in the application program in accordance with the formats below. The mask option area for each device is an application program execution disabled area.

- Mask option area for ML63187: 3FE0H
- Mask option area for ML63189B: 7FE0H
- Mask option area for ML63193: 0FFE0H

Mask option data assignment format

The mask option is set with the two bits (bits 0 and 1) addressed in the mask option area that is assigned to each model.

Table G-1 shows the mask option data assignment format.

Table G-1 Mask Option Data Assignment Format

Function	Mask option area	bit	data	Option to be selected
Low-speed clock oscillation circuit (crystal oscillation circuit/RC oscillation circuit)	ML63187: 3FE0H ML63189B: 7FE0H ML63193: 0FFE0H	bit 0	0	Crystal oscillation circuit
			1	RC oscillation circuit
Reset signal sampling (will/will not carry out 2 kHz sampling)		bit 1	0	Will carry out 2 kHz sampling
			1	Will not carry out 2 kHz sampling

Example of mask option data generation

• When the crystal oscillation circuit is specified for the low-speed clock oscillation circuit and not carrying out reset signal sampling is specified in the ML63187

```
ORG   3FE0H   ← Use an assembler pseudo-instruction to set the address of option data
                 to 3FE0H.
DW    0002H   :  Crystal oscillation circuit, 2 kHz sampling will not be carried out
```

• When the RC oscillation circuit is specified for the low-speed clock oscillation circuit and carrying out reset signal sampling is specified in the ML63189B

```
ORG   7FE0H   ← Use an assembler pseudo-instruction to set the address of option data
                 to 7FE0H.
DW    0001H   :  RC oscillation circuit, 2 kHz sampling will be carried out
```

• When the crystal oscillation circuit is specified for the low-speed clock oscillation circuit and carrying out reset signal sampling is specified in the ML63193

```
ORG   0FFE0H   ← Use an assembler pseudo-instruction to set the address of option data
                  to 0FFE0H.
DW    0000H    :  Crystal oscillation circuit, 2 kHz sampling will be carried out
```

[Additional note: Handling of mask option area when the Development Support System (EASE63180) is used]

The Development Support System (EASE63180) allows the user to execute application programs in the mask option area as well as reading and writing data there. What this means is that there is no equivalent to the test data N area break for detecting when execution strays into this area. The developer must, therefore, define breakpoints for the mask option area when using the EASE63180. These breakpoints then prevent program execution in this area in a manner similar to the test data N area break.

ML63187/189B/193

User's Manual

First Edition: March 2000

FEUL63193-01