OKI Semiconductor

This version: Aug. 1998
Previous version: Nov. 1996

Single Supply PCM CODEC Application Notes

CONTENTS

DESCRIPTION

1. Table of Difference in Electrical Characteristics Between the Dual Supply CODEC and the Single Supply CODEC

		Dual Supply CODEC Ex. MSM6997H	5 V Single Supply CODEC Ex. MSM7543	3 V Single Supply CODEC Ex. MSM7702	5 V Single Supply Malti-ch CODEC Ex. MSM7533
Power Supply Voltage		+5 V ±5% –5 V ±5%	+5 V ±5%	2.7 V to 3.8 V	+5 V ±5%
Power Consumption		68 mW typ. 110 mW max.	20 mW typ. 32 mW max.	15 mW typ.	35 mW typ. 74 mW spec
Signal Level (0 dBm0)		1.227 Vrms (+4 dBm)	0.6007 Vrms (–2.2 dBm)	Transmit 0.35 Vrms Receive 0.50 Vrms	0.85 Vrms (0.80 dBm)
Signal Ground		0 V	$V_{DD}/2$	$V_{DD}/2$	$V_{DD}/2$
Idle Channel Noise	Transmit	–79 dBm0p typ. –75 dBm0p spec.	–74 dBm0p typ. –70 dBm0p spec.	–72 dBm0p typ. –68 dBm0p spec.	–73.5 dBm0p typ. –70 dBm0p spec.
	Receive	–84 dBm0p typ. –75 dBm0p spec.	–78 dBm0p typ. –75 dBm0p spec.	–76.5 dBm0p typ. –74 dBm0p spec.	–78 dBm0p typ. –75 dBm0p spec.
Transmit/Receive Asynchronous Operation		Enable Both BCLOCK and SYNC can be separated in transmit and receive.	Disable BCLOCK is used for both transmit and receive.	Disable BCLOCK is used for both transmit and receive.	Disable BCLOCK is used for both transmit and receive.
Usable BCLOCK Frequency		64 kHz to 2048 kHz	Value specified in catalog	Value specified in catalog	Value specified in catalog
Names of the Products Families		MSM6932B/6933B MSM6962/6963 MSM6982/6983 MSM6996 MSM6998/6999 MSM6810/6811 MSM6812/6813 MSM6814/6815	MSM7508B/7509B MSM7578/7579 MSM7543/7544 MSM7507 MSM7502 MSM6895/6896 MSM7503 ML7000 ML7001	MSM7566/7567 MSM7541/7542 MSM7704 MSM7717 MSM7716 MSM7728	MSM7534 MSM7705

Note: There is no difference in other characteristics between the three types of CODEC listed above.

2. Dynamic Range of Single Supply CODEC

(1) Absolute level

Conventional CODEC (±5 V power supplies in the MSM6997 series)
0 dBm0 = +4.0 dBm = 1.227 Vrms

5 V single supply CODEC (in the MSM7508B, MSM7543)
0 dBm0 = –2.2 dBm = 0.6007 Vrms

3 V single supply CODEC (in the MSM7541)
0 dBm0 = –6.9 dBm = 0.35 Vrms (transmit)
0 dBm0 = –3.8 dBm = 0.5 Vrms (receive)

5 V single supply multi-ch CODEC (MSM7533 etc.)
0 dBm0 = 0.8 dBm = 0.85 Vrms

(2) Maximum output amplitude

Conventional dual supply CODEC (MSM6997/6998)
Vmax = $2 \times \sqrt{2} \times \sqrt{2} \times 1.227 = 4.9\ V_{PP}$
Maximum amplitude : Vmax = $4.9\ V_{PP}$

5 V single supply CODEC (MSM7543/7544, MSM7508B/7509B)
Vmax = $2 \times \sqrt{2} \times \sqrt{2} \times 0.6007 = 2.4\ V_{PP}$
Maximum amplitude : Vmax = $2.4\ V_{PP}$

As described above, the output amplitude of 5 V single supply CODEC series is approximately half the level of the dual supply CODEC.

3 V single supply CODEC (MSM7541/7542, MSM7566/7567, MSM7702, MSM7717, MSM7704)

(Transmit side)
Vmax = $2 \times \sqrt{2} \times \sqrt{2} \times 0.35 = 1.4\ V_{PP}$
Maximum amplitude : Vmax = $1.4\ V_{PP}$

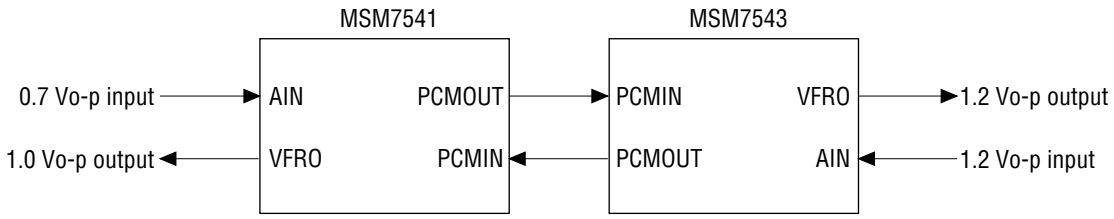
(Receive side)
Vmax = $2 \times \sqrt{2} \times \sqrt{2} \times 0.5 = 2.0\ V_{PP}$
Maximum amplitude : Vmax = $2.0\ V_{PP}$

5 V single supply multi-ch CODEC (MSM7533/7534, MSM7705)
Vmax = $2 \times \sqrt{2} \times \sqrt{2} \times 0.85 = 3.4\ V_{PP}$
Maximum amplitude : Vmax = $3.4\ V_{PP}$

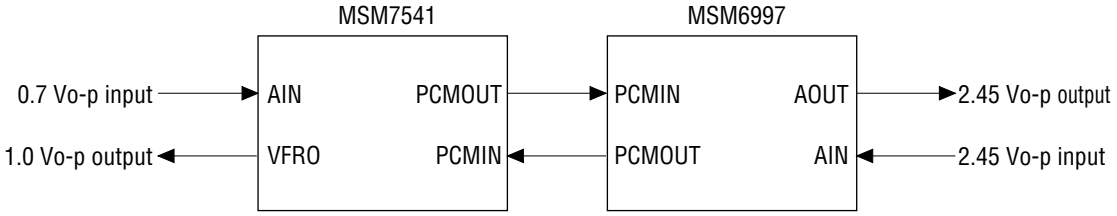
Note: As described above, the dynamic range of a 3 V single supply CODEC is different between the transmit side and the receive side.

3. Output Amplitude of CODEC Connected to Another CODEC with a Different Dynamic Range

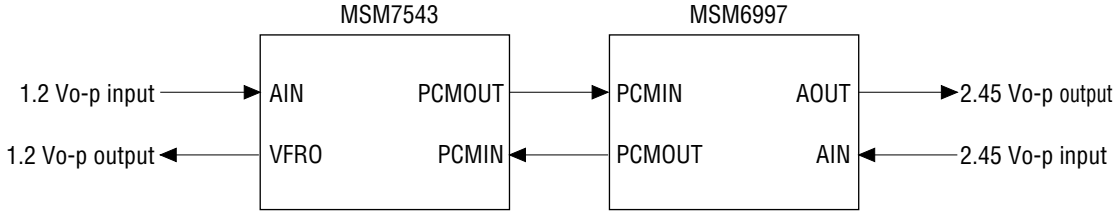
Example 1. When the 3 V single supply CODEC is interfaced with the 5 V single supply CODEC.



Example 2. When the 3 V single supply CODEC is interfaced with the dual supply CODEC.



Example 3. When the 5 V single supply CODEC is interfaced with the dual supply CODEC.



Note: In the above figures, the input gain is assumed to be one.

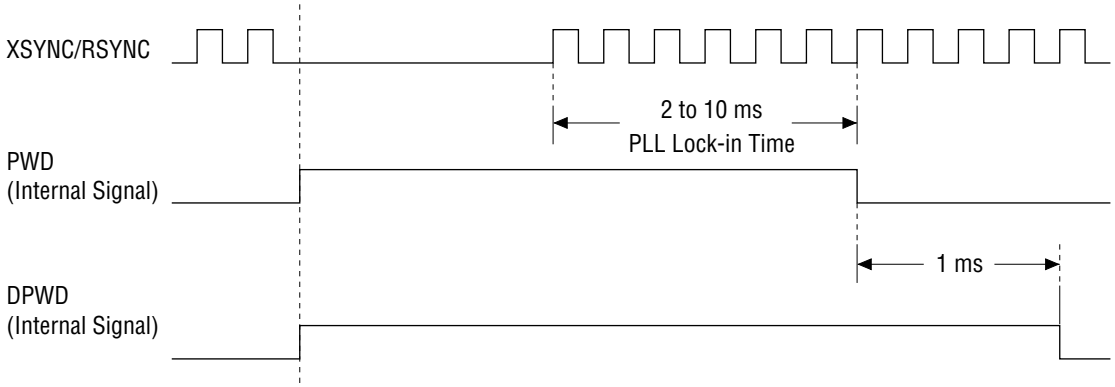
4. Power Save Mode

The single supply CODEC automatically enters power save mode based on the following conditions.

Case 1. When the XSYNC, RSYNC or BCLOCK signal is set to digital "1" or digital "0".

Case 2. When the XSYNC or RSYNC signal has a lot of jitter.

In case 1 and case 2, the internal PLL and the analog circuit with the exception of the reference voltage source go in to a power down state.
This state is called Power save mode.



PWD : Internal circuit signal which sets the PLL and analog circuit with the exception of the reference voltage circuit to the power down state.

DPWD : Delayed PWD. The states of PCMOUT and the analog output do not become stable soon after the entire device goes in to the power on state.

To avoid an unstable state, the DPWD signal inside the device is fixed at digital "1" for about 1 ms after locking of PLL, and the states of PCMOUT and the analog output are fixed.

This description applies to MSM7508B/7509B.

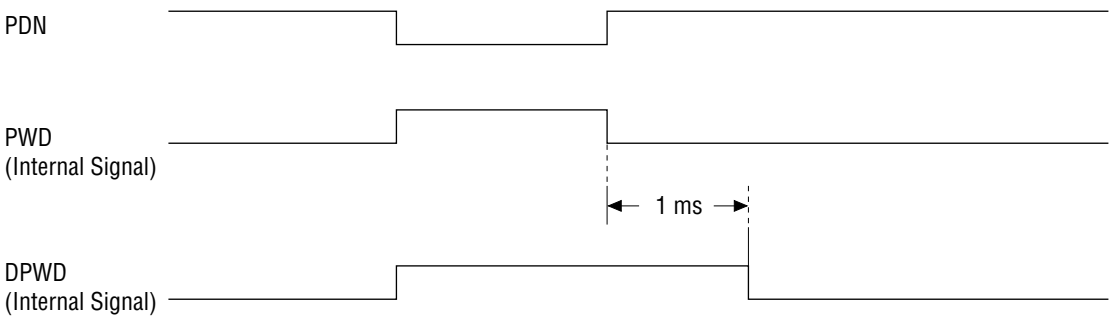
In the case of MSM7541/7542/7543/7544/7566/7567/7533H/7533V/7534/7507/7717/7705/7702/7704/7578/7579/7705/7717, the RSYNC signal is not monitored and only the BCLOCK, and XSYNC signals are monitored.

Note : If the power source contains noise pulses, and the amplitude of the noise is great, the PLL may go in to an asynchronous state and the device may go to power save mode.

5. Power Down Mode

Common to all 3 V single supply and 5 V single supply CODEC.

When digital "0" is input to the power down signal input pin (PDN), all of the analog circuits including the PLL and the reference voltage circuit go in to a power down state.

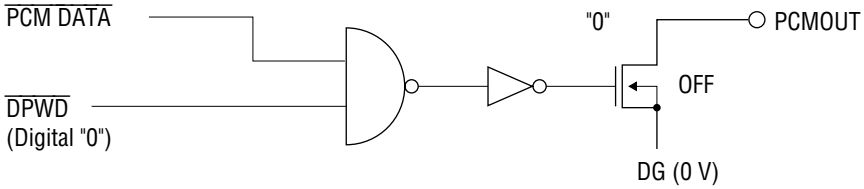


5.1 Setup time from power down mode to operation mode.

The locking of the internal PLL circuit takes a long time to setup. It usually takes 2 ms to 10 ms, depending on device variations. The device starts within a maximum of 10 ms.

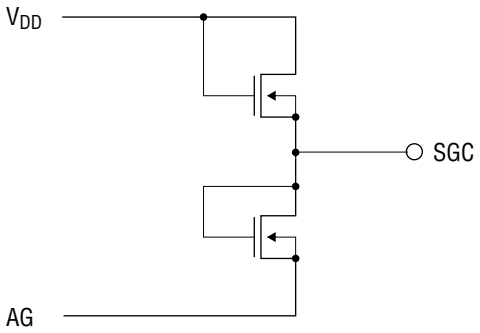
6. The State of the Output Pin in Power Save Mode and Power Down Mode

PCMOUT, PCM data output pins (applicable to all types of device)
These pins are open.



SG (applicable to all types of device)
The pin is undefined when in high impedance.

SGC (applicable to all types of device)
The output voltage is 1/2 V_{DD}. The output resistance is approximately 500 kΩ.



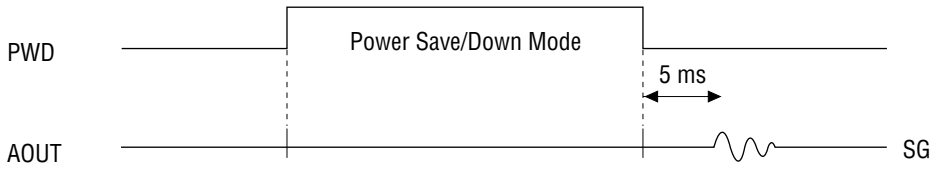
The state of each analog output pin differs depending on the type of device, as shown below.

Product Name	Power Save Mode				Power Down Mode			
	GSX	VFRO	AOUT	AOUT–/AOUT+	GSX	VFRO	AOUT	AOUT–/AOUT+
MSM7508B/7509B	Hz	—	HR SG	—	Hz	—	HR SG	—
MSM7578/7579	HR AG	—	SG	—	HR AG	—	HR SG	—
MSM7543/7544	Hz	HR AG	—	Hz	Hz	HR AG	—	Hz
MSM7507	HR AG	SG	—	SG	HR AG	HR SG	—	Hz
MSM7541/7542	HR AG	HR AG	—	Hz	HR AG	HR AG	—	Hz
MSM7566/7567	HR AG	Hz	—	SG	HR AG	Hz	—	HR SG
MSM7533/7534	HR AG	—	SG	—	HR AG	—	HR SG	—
MSM7702	Hz	—	SG	—	Hz	—	HR SG	—
MSM7704	Hz	—	SG	—	Hz	—	HR SG	—
MSM7717	HR AG	Hz	—	OP	HR AG	SG	—	Hz
MSM7705	HR AG	—	SG	—	HR AG	—	SG	—
MSM7717	HR AG	Hz	—	OP	HR AG	SG	—	Hz
MSM7716	—	—	—	OP	—	HR SG	—	Hz
MSM7000	AG	SG	—	Hz	AG	SG	—	Hz
MSM7001	AG	SG	—	Hz	AG	SG	—	Hz

Hz : High impedance
HR AG : Connected to AG with several 10 kΩ
HR SG : Connected to SGC with several 10 kΩ
SG : Output the SG voltage with 100 Ω or less
OP : Operating

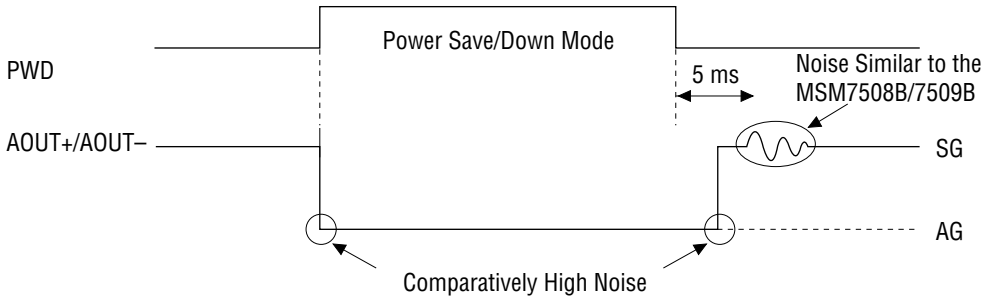
7. Analog Noise Dependent Upon the Power Down/Power Save States

AOUT (MSM7508B/7509B)



Noise is output 5 ms after the rising edge of DPWD signal.
Noise level : –30 dBm0 to –40 dBm0
Noise frequency : 1 kHz to 2 kHz
This noise level is lower than those of the MSM7541/7542/7543/7544 product families. The noise level in MSM7566/7567/7533/7534/7507/7702/7578/7579 is lower still.

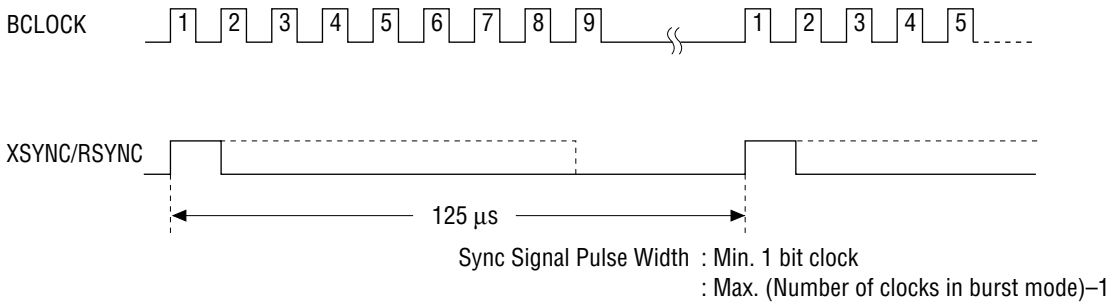
AOUT+/AOUT– (MSM7541/7542/7543/7544)



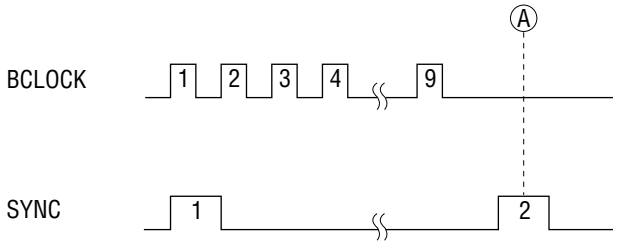
Jitter noise is likely to be generated at the syncronizing signal in the wireless system in particular, but when jitter noises continue for 500 ns or more, even if communication is in progress, the device may enter power save mode. At that time, AOUT outputs noise. Generally in a device like the CODEC, it is difficult to design a device free from a noise. With the MSM7541/7542/7543/7544 series, the noise generated is higher than in the MSM7508B and MSM7509B. With the MSM7541/7542/7543/7544 series, the control of power saving by the RSYNC is not provided because noise is easily generated at RSYNC.

8. The Burst Mode Clock

In the single supply series CODEC, the device can be operated by a burst mode clock.



Bit clocks 1 to 8 are used for PCM data transfer, bit clock 9 is used for starting the internal operation of the CODEC, so that at least 9 bits are needed (except an operation at 64 kHz). When the bit clock frequency is 64 kbps, 8 bit clocks are required, for the device to operate, but this is not a burst mode clock operation. In this case the maximum cycle time of a synchronizing signal is 100 µs (exactly 109.375 µs). When the bit clock signal BCLOCK stops, the device goes to power save mode.



Whether or not the bit clock and the SYNC signal exist at the same time is monitored at each SYNC signal timing at the rising edge of the bit clocks. In the above figure, the BCLOCK signal does not exist at the point "A", so the device is operating in power save mode. Practically, the device goes to power save mode after a certain time elapses from the point "A".

9. Interfaces Between the Device Input and a Microphone Output

According to the analog input specified for MSM7543, the maximum input level of the MSM7543 GSX pin is 1.2 Vo-p and the +3 dBm0 digital pattern is output from the PCMOUT pin. Normally the gain of the average speed level is set to –15 dBm0 for voice devices, which is equivalent to the signal level of 0.15 Vo-p for the MSM7543 GSX pin (0.088 Vo-p at the MSM7541).
If the average signal level from a microphone unit is X Vo-p, the gain required for the analog input of the MSM7543 is as shown below.

$$G = 20 \log 0.151/X \text{ dB}$$

Since the maximum input amplifier gain can be set to +20 dB, if the above value of gain G is lower than +20 dB, only the gain setting of the input amplifier is required. But if the value of G is higher than +20 dB, a microphone preamplifier must be added. Fig. 1 shows an example of a circuit with a preamplifier added.

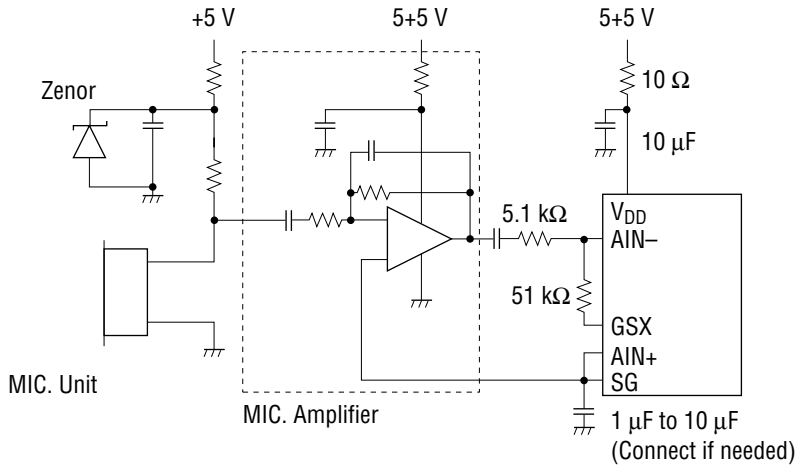


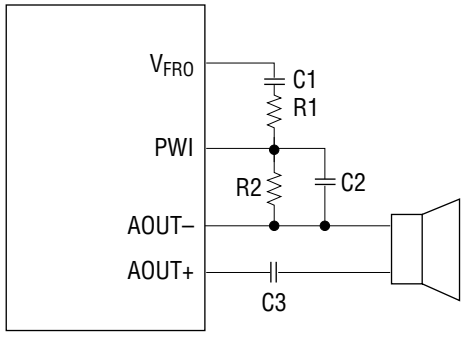
Figure 1

Note : In Fig. 1, the amplifier gain of the MSM7543 analog input is assumed to be +20 dB, and a resistance of 10 Ω and a capacitance of 10 µF should be connected to the power supply for decoupling use if needed.

10. Interface Between the Device Output and a Speaker Input

The MSM7543 analog output has the minimum differential output load resistance of 1.2 kΩ. This value is defined to assure an output amplitude of AOUT+/AOUT– and the total distortion at the level of the catalog. If the requirements usage are satisfied, the value of the load resistance may be less than 1.2 kΩ. The direct driving of a dynamic type speaker having an impedance of less than 1.2 kΩ should be tested by the user.

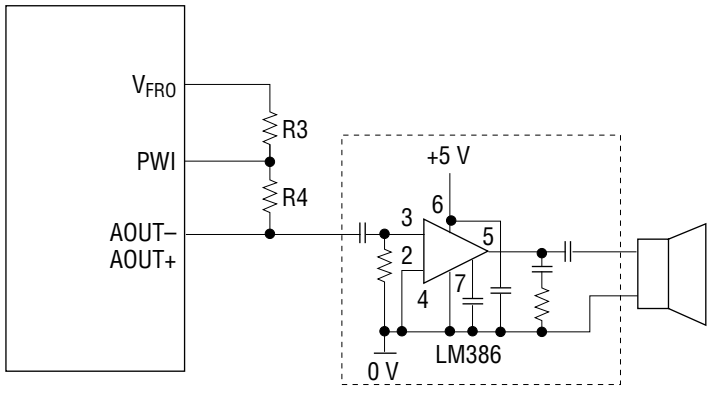
An example of a peripheral circuit when using the device to drive a speaker directly is shown in Fig. 2.
An example of a peripheral circuit when adding a preamplifier to the device is shown in Fig. 3.



Maximum output amplitude at V_{FRO}
: 1.2 Vo-p
R1 : 51 kΩ
R2 : 51 kΩ
C1 and C2 are for adjustment of frequency characteristics.
When the f-characteristic is flat,
C1 : 0.1 μF
C2 : Not used
C3 is used for preventing the DC-current between AOUT+ and AOUT–.
C3 : 47 μF

Figure 2

In Fig. 2 the gain setting is defined at 0 dB, but if an output level of a speaker is higher in this state, a resistor should be connected in series with the capacitor C3. The characteristics of output amplitude and harmonic distortion are improved, as a consequence of converting this resistance.

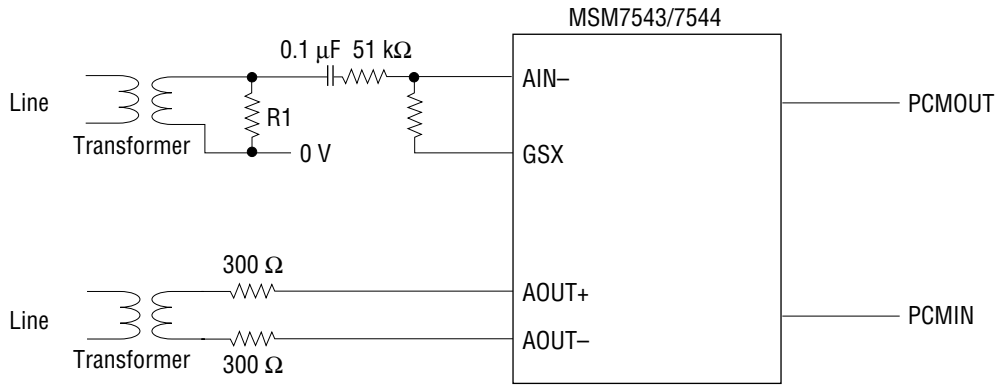


R3 : 51 kΩ
R4 : Should be adjusted.

Refer to the data sheet prepared by the National Semiconductor Co., for the peripheral circuit of LM386.

Figure 3

11. An Example of a Circuit Connected to a Telephone Line



Note : The value of R1 in the above diagram is 600 Ω, but a resistor between 550 Ω and 600 Ω is used for a transformer coil resistance.