CHAPTER 11

Technology introduction

Technology introduction

1. Semiconductor process technology

1-1 Silicon process technology

HAMAMATSU uses various types of silicon process technology to develop a wide variety of optical devices [Table 1-1].

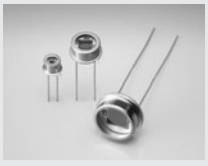
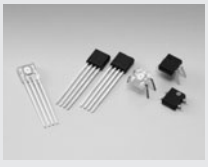
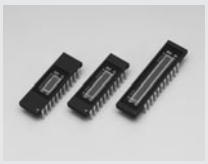
By the photodiode process we fabricate Si photodiodes with low dark current and high UV sensitivity. The photo IC process is suitable for high-speed response photo ICs that integrate a photodiode together with a signal processing circuit. To fabricate high-speed photo ICs, a PIN bipolar process is utilized, which is for integrating a PIN photodiode and bipolar high-speed signal processing circuit onto the same chip.

The image sensor process includes a CMOS process and CCD process. In the CMOS process, HAMAMATSU utilizes its advanced analog and digital circuits to fabricate sophisticated photosensors used in a wide range of fields including measurement, medical diagnosis, and security. In the CCD process, HAMAMATSU takes advantage of its own unique process control technology to fabricate image sensors having a high S/N suitable for low-light-level detection.

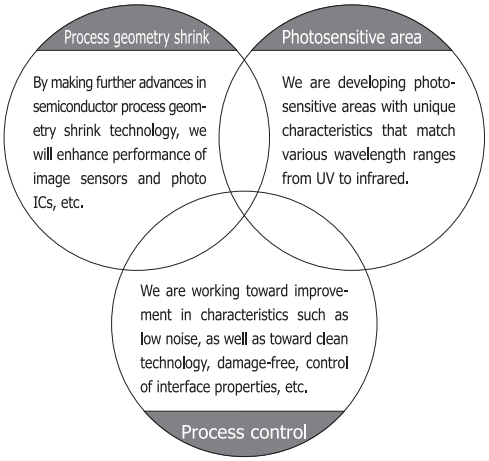
Future approaches to silicon process technology

Technology development is progressing along three major themes (process geometry shrink, photosensitive area, and process control). By merging these three technologies, HAMAMATSU aims to produce opto-semiconductors with even higher sensitivity, higher speed, and higher device integration.

[Table 1-1] HAMAMATSU silicon process technologies

Product example	Type of process	Features
	Photodiode process	● Wide spectral response range from UV to infrared ● Low dark current ● High UV sensitivity ● Various types of products (Si photodiodes, Si PIN photodiodes, Si photodiode arrays, Si APDs, PSDs)
	Photo IC process	● Integrated with photodiode and signal processing circuit ● Digital output or analog output ● Supports bipolar process, PIN bipolar process, and CMOS photo IC process
	CMOS process	● Delivers low power consumption and high device integration ● Suitable for image sensors with a wide spectral response range from UV to infrared
	CCD process	● Front-illuminated CCD image sensors: high S/N and wide dynamic range ● Back-thinned CCD image sensors: high quantum efficiency in the UV region

[Figure 1-1] Future directions in silicon process technologies



1-2 Compound semiconductor process technology

Generally crystal defects are a frequent concern in compound semiconductors, unlike in silicon which is a single element. This makes epitaxial growth technology essential for obtaining good crystals. At HAMAMATSU we use technologies such as MBE/MOCVD to form good quality crystalline growth layers. We are also amassing a great deal of technical knowledge on the wet etching process.

HAMAMATSU is working to develop high-performance optical devices using the compound semiconductor process technology capable of precision processing that includes dry etching process as well as the wet etching process [Table 1-2].

Compound semiconductors such as GaAs and InP allow making semi-insulating substrates with resistance over 10000 times larger than the resistance of silicon. This kind of performance is not possible to obtain from the silicon process technology. The compound semiconductor process technology allows making electrical insulation without forming a junction, so parasitic capacitance can be held to extremely low levels. Devices with response speeds exceeding 100 GHz, which is determined by the CR time constant, can even be fabricated.

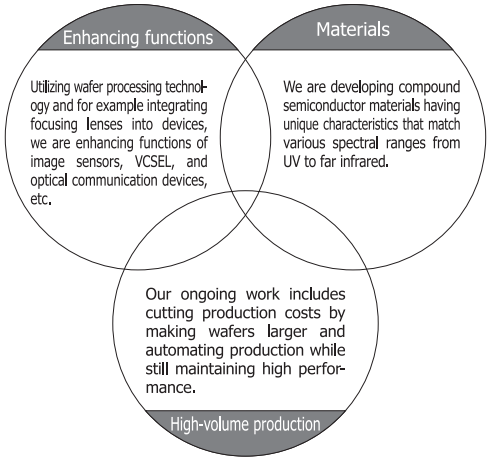
Future approaches to compound semiconductor process technology

The development of this technology is progressing along three major themes (enhancing functions, materials, and high-volume production). These technical areas are essential for developing and manufacturing high-performance compound semiconductor devices that provide high sensitivity and high speed. As to the materials, in particular, we are developing infrared detectors using InAsSb-based materials that do not contain Hg, Cd, or Pb which falls under environmental management substances.

[Table 1-2] HAMAMATSU compound semiconductor process technologies

Product example	Type of process	Features
	Compound photodiode process	● Covers UV to short-wavelength infrared regions by changing combination of In/Ga/As/P used for active layer (GaP, GaAsP: UV to visible region, GaAs: visible to near infrared region, InGaAs: near infrared, InAs: near to mid infrared) ● Available in various sizes from large active area for analytical use to small diameter of active area for high-speed optical communication ● Suitable for array, can be used for infrared imaging when utilized as image sensor active area
	Photoconductive detector process	● Near to mid infrared detection (PbS, PbSe, MCT, InSb) ● Resistance changes with incident light. ● High sensitivity
	LED process	● Red to near infrared light emitters ● Small emission spot diameter ● High reliability
	VCSEL process	● Red to near infrared VCSEL ● Ultra-high speed, high output ● Suitable for array

[Figure 1-2] Future directions in compound semiconductor process technology



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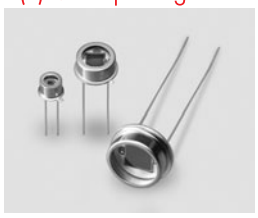
2. Mounting/package technology

2 - 1 Packages for diverse needs

HAMAMATSU offers a diverse lineup of packages to meet a wide range of market needs [Figure 2-1]. Metal packages are widely used in applications requiring high reliability. Ceramic packages are utilized for general-purpose applications, while plastic packages are used in applications where low cost is essential. Special type packages include square metal packages used in thermoelectrically cooled CCD area image sensors, etc. A wide lineup of packages is also available for surface mounting. For applications where small and thin devices are particularly required, we supply COB (chip on board) and thin plastic packages like those shown in Figure 2-2.

[Figure 2-1] Package examples

(a) Metal package



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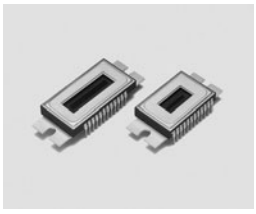
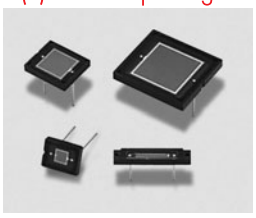


Square metal

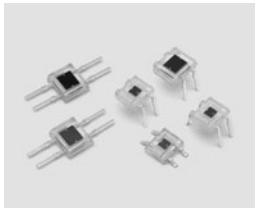
(b) Ceramic package



Standard type

Surface mount type

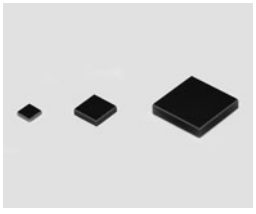
(c) Plastic package



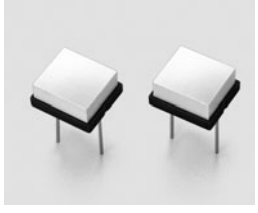
Standard type

COB (chip on board)

(d) Chip size package

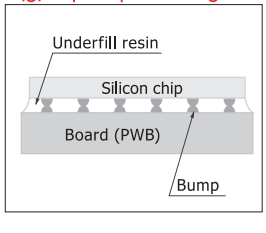


(e) Coupled to scintillator



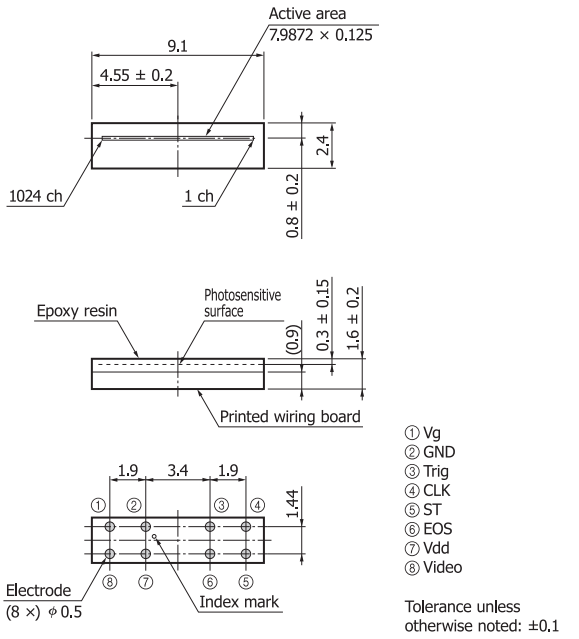
(f) Long, narrow type

(g) Flip-chip bonding



Flip-chip bonding is a mounting technology where an inverted chip is directly connected to a board, etc. by using solder bumps. The flip-chip bonding saves a great deal of space and also upgrades device performance.

[Figure 2-2] COB example (S10226, unit: mm)



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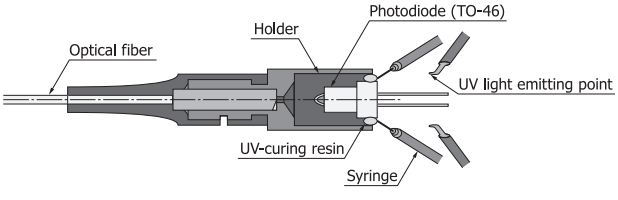
2 - 2 High-precision alignment technology

In optical communications devices, the optical loss at the coupling point between the optical fiber and photodiode has to be reduced. Therefore, high-precision alignment on the submicron level is essential. HAMAMATSU uses the following procedure for this alignment task.

① Set the photodiode and holder in the alignment system.
② Move the photodiode toward the holder.
③ Move the photodiode a little at a time, and search for the position where sensitivity is highest.
④ Apply UV-curing resin to the coupling point.
⑤ Cure (harden) the resin using a UV light source.

[Figure 2-3] Optical fiber and photodiode alignment



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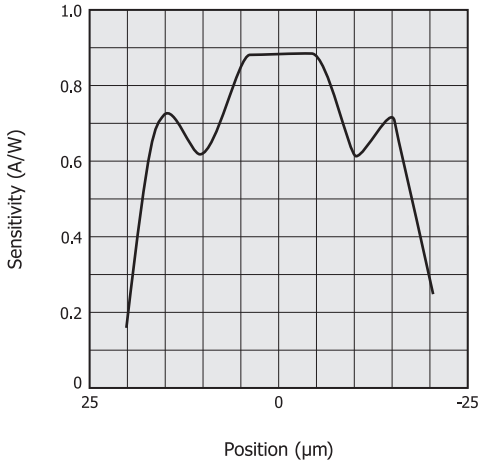
[Figure 2-4] Photodiode alignment profile example



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3. MEMS technology

Silicon MEMS (micro-electro-mechanical systems) technology is drawing much attention as a technology capable of innovating opto-semiconductor functions. Here we introduce some of our MEMS technology.

3 - 1 Etching technology

In addition to isotropic etching (same amount of etching in all directions) used in fabricating conventional semiconductors, MEMS technology utilizes anisotropic etching and sacrificial layer etching.

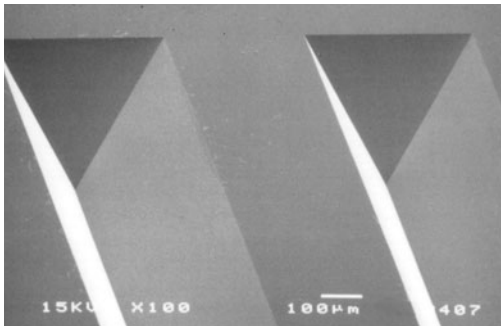
Anisotropic etching

Unlike isotropic etching, anisotropic etching is a technique for etching material in specified directions.

(1) Alkaline etching

This technique uses potassium hydroxide and TMAH (tetra methyl ammonium hydroxide) solutions to perform anisotropic etching by utilizing the difference in etching speed on the crystalline surface of the silicon wafer. A silicon wafer having a (100) crystal plane is generally used, and etching is performed on square aperture patterns formed along lines where a (111) crystal plane and the wafer surface intersect. This makes a (111) crystal plane with approx. 55 degree angles appear. Because of single-crystal processing, alkaline etching offers highly precise etching and so is used for fabricating thin active areas, forming V-grooves for passive alignment, and for MEMS packages, etc.

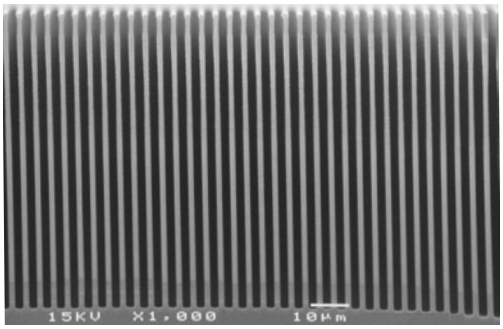
[Figure 3-1] V-grooves formed by alkaline etching



(2) Deep etching

Deep etching is a technique for isolating elements and forming actuators, etc. by dry etching in the perpendicular direction. Etching depth can extend from a few dozen to several hundred micrometers. The Bosch process is used to carry out deep etching. The Bosch process is a method for etching by switching between an etching gas (such as SF_6) and a film protection gas (such as C_4F_8) for etching groove side walls.

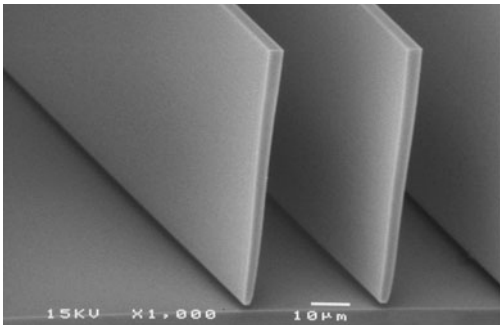
[Figure 3-2] Trenches made by deep etching



Sacrificial layer etching

Sacrificial layer etching is a technique for fabricating hollow structures by etching only specified layers. This etching technique is utilized for forming special thin-film active areas and for actuator moving parts. Figure 3-3 shows movable comb-teeth formed using an SOI (silicon on insulator) wafer. The buried oxide film exposed after the deep etching is then formed by sacrificial layer etching. In a microbolometer, a hollow thin-film active area is formed by sacrificial layer etching after patterning the active area.

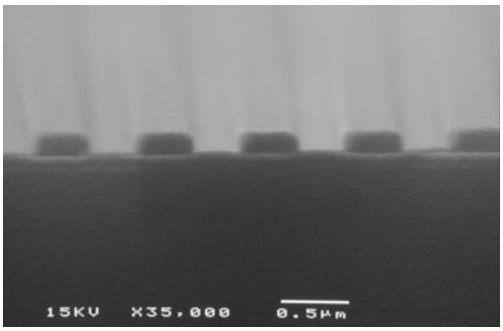
[Figure 3-3] Hollow movable comb-teeth formed by sacrificial layer etching



3 - 2 Nanoimprint

Nanoimprint is a new technique applicable for forming nanometer-scale structures and for nanolithography. In this method, UV-curing resin is coated onto a substrate, a quartz pattern (mold or template) formed with fine structures is pressed onto that substrate, and UV light is then irradiated to transfer the fine structures to the resin. Nanoimprint allows fabricating fine optical components with highly detailed patterns.

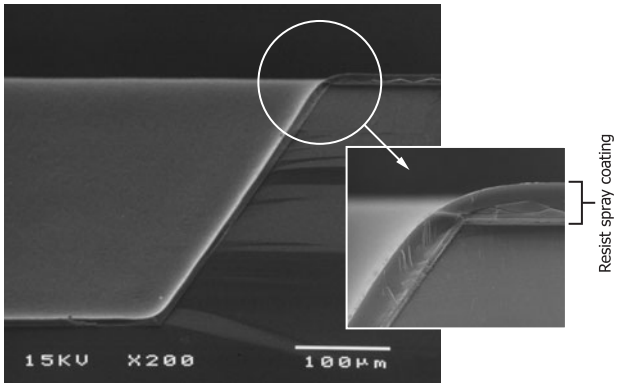
[Figure 3-4] Nanoimprint example



3 - 3 Resist spray coating

Metal wiring layers and insulator films sometimes need to be etched after cavities and grooves are formed by alkaline etching, etc. Conventional spin coating cannot apply resist uniformly to those grooves and surrounding areas. Therefore, in those cases, a resist diluted into a solution is sprayed onto the grooves by a spray nozzle. This method allows forming patterns on structures with grooves.

[Figure 3-5] Resist spray coating example



3 - 4 Bonding technology

Wafer bonding and chip-to-chip bonding are indispensable techniques for WLP (wafer level packages) and for achieving even higher integration in devices in the future.

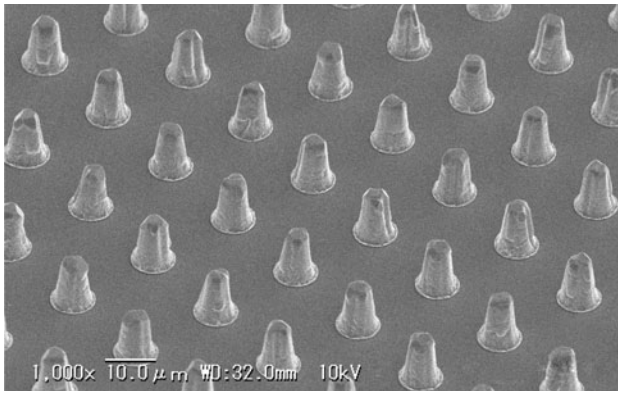
Wafer direct bonding

Wafer direct bonding is a technique for bonding wafers with a high degree of sealing without using adhesives.
Wafer direct bonding includes anodic bonding and room-temperature bonding. Anodic bonding is a technique for covalently bonding a silicon wafer to alkaline glass at their interface by applying an electrical field at a high temperature. Room-temperature bonding is a technique for bonding wafers together by performing surface processing between the wafers and applying pressure to them in a vacuum.

Fine pitch bump bonding

When forming a photosensor and a circuit together monolithically is difficult, as in compound opto-semiconductors, a compound opto-semiconductor chip must be electrically connected to a silicon readout IC. For example, in the case of an infrared two-dimensional image sensor (640 × 512 pixels), 327680 indium bump electrodes per chip are formed at an approx. 20 μm pitch, and the sensor chip is then jointed to the readout IC chip by high-precision flip-chip bonding.

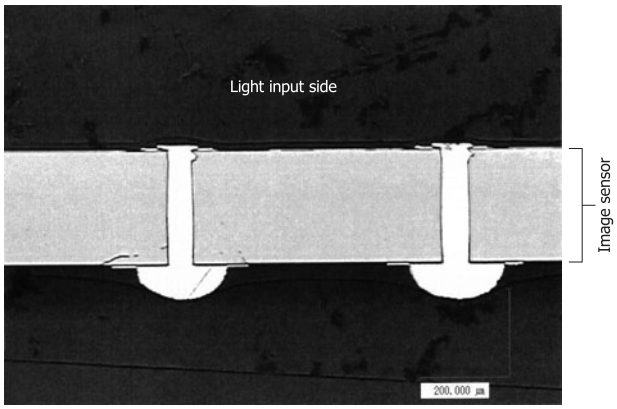
[Figure 3-6] 20 μm pitch indium bump electrodes



3 - 5 Through-hole electrode

A through-hole electrode is an electrical connection passing through the silicon wafer, which allows the electrode of an optical device formed on the silicon wafer surface to extend to the backside of the wafer. This through-hole electrode is formed by deep etching and insulating, and by forming electrodes.
Through-hole electrode connections and bonding technology are indispensable techniques in order to achieve higher integration of optical sensors, component mounting on active areas, and WLP.

[Figure 3-7] Image sensor through-hole electrode example



4. Hybrid technology

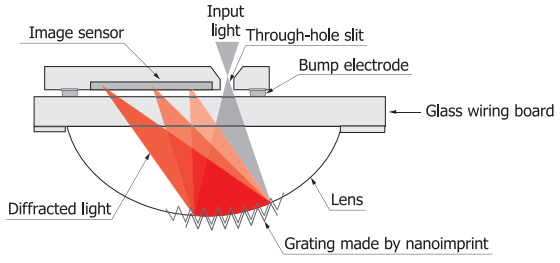
4 - 1 Ultra-compact mini-spectrometers

Conventional spectrometers are large and rather high in cost. We have provided mini-spectrometers that are handy and easy to use. Now we offer an even smaller mini-spectrometer. It is an ultra-compact mini-spectrometer reduced to nearly thumb size. This ultra-compact mini-spectrometer will expand spectrometer applications to include tasks such as color management in color printers and LCD monitors.

Figure 4-1 shows the internal structure of the ultra-compact mini-spectrometer. Elemental technologies for fabricating ultra-compact mini-spectrometers include technologies for replicating a grating and for fabricating an entrance slit in the image sensor chip. The technology for replicating a grating makes use of nanoimprint, which transfers an engraved grating pattern onto a glass body. UV-curing resin (replica resin) is attached near the top of a condenser lens, and the grating is replicated on the lens by pressing the grating pattern against the resin while simultaneously irradiating it with UV light [Figure 4-2].

The technique for fabricating an entrance slit in the image sensor chip involves etching that forms an entrance slit precisely aligned using the same photomask as the image sensor. This ultra-compact mini-spectrometer has an internal CMOS linear image sensor made by HAMAMATSU with functions and characteristics suitable for spectrometers.

[Figure 4-1] Structure of ultra-compact mini-spectrometer



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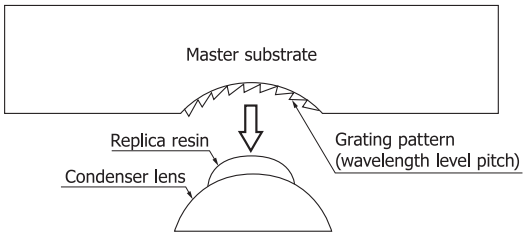
[Figure 4-2] Replication of grating



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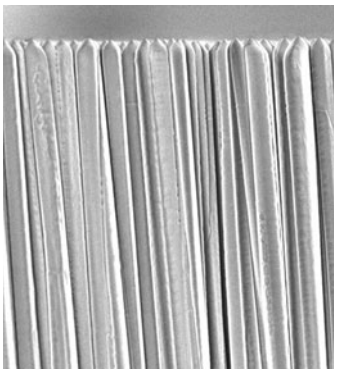
4 - 2 CsI(Tl) direct-deposition type flat panel sensors

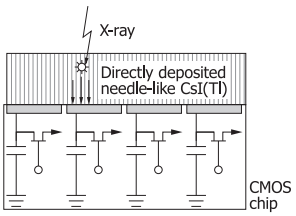
CsI(Tl) direct-deposition type flat panel sensors are highly sensitive digital X-ray image sensors in which CsI(Tl) is directly deposited on the large area CMOS image sensor.

Directly depositing a scintillator material comprised of CsI(Tl) needle-like crystal, which converts X-rays into light, onto the sensor chip helps reduce effects from light scattering and coupling loss occurring between the chip and the scintillator, thereby improving the image resolution and sensitivity.

[Figure 4-3] Needle-like crystal of CsI(Tl)



[Figure 4-4] Cross section of CsI(Tl) direct-deposition type flat panel sensor



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