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LF – 2.7 GHz 60 dB TruPwr™ Detector

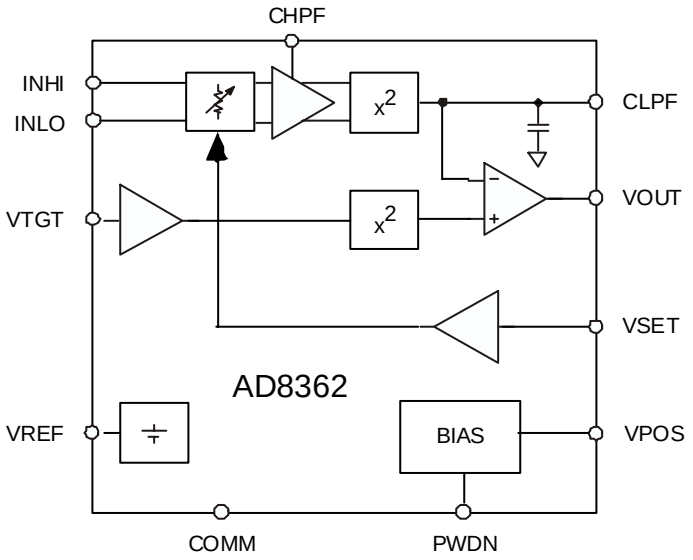
Preliminary Technical Data AD8362

FEATURES

True-Power (Root-Mean-Square) Measurement
Temperature-Stable Linear-in-dB Response
Input Dynamic Range 60 dB
-45 to +15 dBm CW Input re: 50 Ω
Flat Response from LF to 2.7 GHz, useful to 3 GHz
High Accuracy and Linearity
Laser-trimmed Slope of 50 mV/dB
Modulation Independent (GSM/W-CDMA/TDMA, etc.)
Operation from –40 to +85 °C at V_S of 4.5 to 5.5 V
Powers Down to <100 µW

APPLICATIONS

Power Amplifier Linearization/Control Loops
Multi-Carrier Transmitter Power Control
Rx or Tx Signal Strength Indication (RSSI, TSSI)
Instrumentation at LF, HF, VHF, UHF, L- and S-bands



PRODUCT DESCRIPTION

The AD8362 is a true-RMS-responding power detector having a 60 dB measurement range, intended for use in a variety of high-frequency communication and instrumentation systems where an accurate response to signal power is required, regardless of signal waveform. It is fully specified for use at frequencies up to 2.7 GHz. Signal inputs having RMS values from 1.26 mV to 1.26 V (–45 to +15 dBm in a 50 Ω system) can be accepted. Large crest factors, exceeding the requirements for accurate measurement of CDMA signals, do not degrade accuracy. The AD8362 is easy to use, requiring only a single supply of 5 V plus signal-coupling capacitors (or, in some cases, a balun) and simple decoupling.

The input signal is first applied to a resistive ladder attenuator, having twelve tap-points at about 5 dB intervals. These are smoothly interpolated using a proprietary technique to implement an accurate and continuously-variable attenuator, whose setting is controlled by a voltage applied to pin **VSET**. The resulting signal is applied to a high-performance broadband amplifier, the output of which is measured by a wideband square-law detector cell. The resulting fluctuating output is then filtered and compared with the output of an identical squarer, whose input is a fixed DC voltage imported via pin **VTGT**, which will usually be tied to the accurate reference of 1.25 V provided at pin **VREF**. In some applications, the target voltage (and thus the log intercept) may be altered. The resulting difference in the output of the two squaring cells is then applied to a high-gain error amplifier (an integrator) generating a voltage at pin **VOUT** which can run from rail to rail.

When used in a power measurement mode, pin **VOUT** is simply tied to **VSET**, and the output is then proportional to the logarithm of the RMS value of the input. Thus, the reading is scaled directly in decibels, and is conveniently scaled 1 V per decade (50 mV per dB); other slopes are easily arranged. The output can run from ground to a maximum of about 0.1 V below the supply voltage, V_S. High load currents can be provided.

In controller modes, this low noise signal is used to vary the gain of the host system's RF amplifier, to restore a balance between the set-point demand, determined by the voltage applied to the **VSET** pin, and a sample of the actual RF power. The set-point voltage may optionally be a baseband replica of the amplitude modulation, in which case the effect is to remove the modulation component prior to detection and low-pass filtering.
For general instrumentation applications, the corner frequency of the averaging filter may be lowered without limit by the addition of an external capacitor at pin **CLPF**. In this way, the AD8362 can be used to determine the RMS value of a low-frequency signal having a complex modulation envelope. The high-pass corner of the broadband amplifier may also need to be lowered by a capacitor added at pin **CHPF**.

The AD8362 may be powered down by a logic voltage applied to the **PWDN** pin, when the current consumption is reduced to under 2 µA. The chip powers up to its normal operating current of 18 mA at 25ºC within less than 1 µs.

The AD8362 is supplied in a 16-pin TSSOP package for operation over the temperature range of -40°C to +85°C.

Multiple patents pending

Rev. PrN 02/14/02

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AD8362-SPECIFICATIONS

(Unless otherwise noted, V_S = 5 V, T=25°C, Z_o = 50 Ω, differential input drive, 0 dBV = 1 Vrms)

Parameters	Conditions	Min	Typ	Max	Units
OVERALL FUNCTION					
Maximum Input Frequency			2.7		GHz
Input Voltage Range	CW sine wave input	0.00126		1.26	Vrms
		-58		+2	dBV
	Equivalent input power re: 50 Ω (see note 1)	-45		+15	dBm
Input Voltage Range	Single-ended drive, CW sine wave input	1.26		400	mVrms
		-58		-8	dBV
	Equivalent input power re: 50 Ω (see note 1)	-45		+5	dBm
Measurement Linearity[2]	Over central 50 dB range, 30 MHz ≤ f ≤ 2.7 GHz		±0.5		dB
	Over central 60 dB range, 30 MHz ≤ f ≤ 2.7 GHz		±1		dB
RF INPUT INTERFACE	Pins **INHI**, **INLO**, ac coupled				
Input Resistance	Single-ended drive, wrt **DECL**		100		Ω
	Differential drive		200		Ω
Input Impedance	(see performance curves)		TBD		Ω
OUTPUT INTERFACE	Pin **VOUT**				
Voltage Range	R_L ≥ 200 Ω	0.5		4.95	V
Source/Sink Current	**VOUT** held at V_S/2		TBD		mA
Small-signal Bandwidth	C_L ≤ 300 pF		TBD		MHz
Full-scale Slew Rate	C_L ≤ 300 pF		TBD		V/µs
Wideband Noise	**CLPF** = xxx pF, f_{SPOT} ≤ 20 MHz		TBD		nV/√Hz
SET-POINT INPUT	Pin **VSET**				
Voltage Range	Corresponding to 1.126 mV – 1.26 Vrms input signal	0.5		3.5	V
Input Resistance			70		kΩ
Logarithmic Scale Factor	f = 100 MHz, -40°C ≤ T_A ≤ 85°C		50		mV/dB
Logarithmic Intercept	f = 100 MHz, -40°C ≤ T_A ≤ 85°C, re: 1 Vrms		-66		dBV
	re: 50 Ω		-53		dBm
Temperature Sensitivity	P_{IN} = -10 dBm, slope and intercept errors combined		TBD		dB/°C
RMS TARGET SET[3]	Pin **VTGT**				
Input Voltage Range	Measurement range = TBD dB	TBD		TBD	V
Input Bias Current	**VTGT** = 1.25 V		-28		uA
	VTGT = 0 V		-52		uA
Incremental Input Resistance			52		kΩ
Bandwidth of Target Channel	To –3 dB point		260		MHz
VOLTAGE REFERENCE	Pin **VREF**				
Output Voltage	-40°C ≤ T_A ≤ 85°C		1.25		V
Current Limit	Into a grounded load		TBD		mA
Power Supply Rejection Ratio			TBD		V/V
POWER DOWN INTERFACE	Pin **PWDN**				
Logic Level to Enable	Logic LO enables			TBD	V
Logic Level to Disable	Logic HI disables	TBD			V
Input Current	Logic HI		TBD		uA
	Logic LO		TBD		uA
Enable Time	From **PWDN** Low to **VOUT** within 10% of final value		TBD	TBD	us
Disable Time	From **PWDN** High to **VOUT** within 10% of final value		TBD	TBD	us

Parameters	Conditions	Min	Typ	Max	Units
POWER INTERFACE	Pin **VPOS**				
Supply Voltage		4.5	5	5.5	V
Quiescent Current			19	TBD	mA
vs. Temperature	-40°C ≤ T_A ≤ 85°C		19		mA
Supply Voltage Sensitivity		TBD	TBD	TBD	mA/V
Supply Current	**PWDN** enabled		TBD		µA

Notes

1. Using an external 100 Ω resistor connected between **INHI** and **INLO** to produce a net 50 Ω input resistance.
2. Determined by linear regression.
3. The voltage required at this pin is 10x the rms value of the steady-state output of the amplifier section.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage V_{POS}…….…..…..…… .5.5V
Input Power (re: 50 Ω)…….……..……TBD
Equivalent Voltage ……TBD mVrms
Internal Power Dissipation ….……...……..500 mW
θ_{JA} ……..…125 °C/W
Maximum Junction Temperature ……..…+125 °C
Operating Temperature Range …..-40 °C to +85 °C
Storage Temperature Range …….-65 °C to +150 °C
Lead Temperature Range (Soldering 60 sec)..+300 °C

***Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**

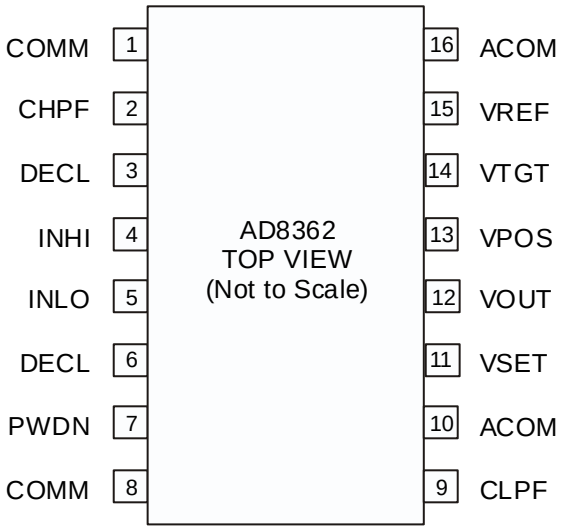
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8362 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy [>250 V HBM] electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temp. Range	Package Description
AD8362ARU	-40 °C to +85 °C	Tube, 16-Lead TSSOP
AD8362ARU-REEL7		7" Tape and Reel
AD8362ARU-REEL		13" Tape and Reel
AD8362-EVAL		Evaluation Board

PIN CONFIGURATION



Pin Function Descriptions

Pin	Name	Description	Equivalent Circuit
1, 8	**COMM**	Common connection. Connect via low impedance to system common.	
2	**CHPF**	Input HPF. Connect to common via a capacitor to determine 3 dB point of input signal high-pass filter.	
3, 6	**DECL**	Decoupling terminals for **INHI** and **INLO**. Connect to common via a large capacitance to complete input circuit.	
4	**INHI**	"High" signal input terminal. Part of a differential input port with **INLO**.	
5	**INLO**	"Low" signal input terminal. Part of a differential input port with **INHI**.	
7	**PWDN**	Disable/Enable control input. Apply logic high voltage to shut AD8362 down.	
9	**CLPF**	Connection for loop filter integration (averaging) capacitor, the other pin of which is usually grounded via a resistor to improve loop stability and response time.	
10, 16	**ACOM**	Analog common connection for output amplifier.	
11	**VSET**	The voltage applied to this pin sets the decibel value of the required RF input voltage that results in zero current out of pin **CLPF** and thus the loop integrating capacitor.	
12	**VOUT**	Output of error amplifier. In measurement mode, normally connected directly to **VSET**.	
13	**VPOS**	Connect to +5 V power supply.	
14	**VTGT**	The logarithmic intercept voltage is proportional to the voltage applied to this pin. The use of a lower target voltage increases the crest factor capacity.	
15	**VREF**	General-purpose reference voltage output of 1.25V (usually connected only to **VTGT**).	

Evaluation Board

Figure XX shows the schematic of the AD8362 evaluation board. It supports operation of the AD8362 in Measurement Modes or Controller Modes, and allows for the use of the internally-generated reference voltage to be used as the target voltage.

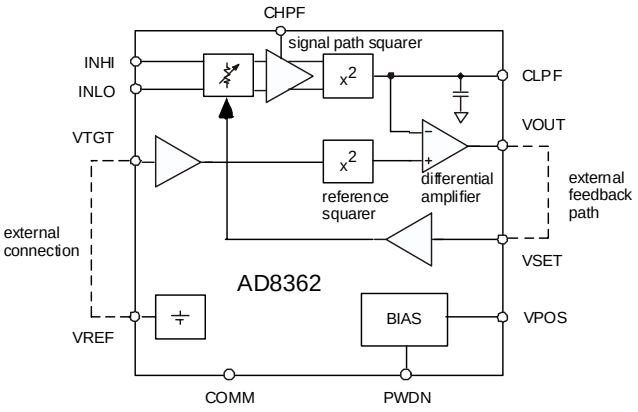


Figure X4 Simplified Block Diagram in Measurement Mode

Figure X4 shows the AD8362 as it could be configured for measurement mode operation. The AD8362 compares an amplified, squared, averaged version of the input signal to a target voltage which has been applied to an identical squaring cell. These voltages are applied to a differential amplifier, the output of which is fed back in Measurement Mode to the gain control of the input variable attenuator. This forces the output of the signal-path squaring cell to be equal to the output of the reference squaring cell. In this mode, the output voltage of the differential amplifier is a linear-in-dB representation of the input signal rms voltage.

Input Circuit

The input to the AD8362 is differential in order to optimize the input measurement range, among other things. A balun can transform a single-ended RF signal to differential form. The ETC1.6-4-2-3, 500 MHz – 2.5 GHz, 4:1 balun is installed on the evaluation board. Note that the RF input impedance at the RFIN connector may not be 50 Ω unless a balun having the correct ratio is used. If the AD8362 is to be evaluated at frequencies higher than 2.5 GHz or lower than 500 MHz, better performance will be obtained if this balun is replaced with one that is designed for those frequencies.

It is important to note that the balun transformer steps up the signal voltage by the square root of its turns ratio. Thus, the signal voltage at the output of T1 is 6 dB larger than at its input. This is effectively the input signal magnitude which the AD8362 measures.

The AD8362 eval board has been designed to accommodate other single-ended interfaces. If either of the configurations described below are used, balun T1 may be eliminated, at the expense of a 6 dB reduction in measurement range at the high end and reduced sensitivity to very small signals.

Balun T1 may be removed and replaced with two resistors which will match a 50 Ω source to the input impedance of the AD8362. In this case, RA should be 25 Ω and RB should be 33 Ω, as shown in Figure X2. Note that the unused input to the AD8362 must be ac-coupled to ground, via capacitor C5 and the 0 Ω resistor RC. In this configuration, R16 is open.

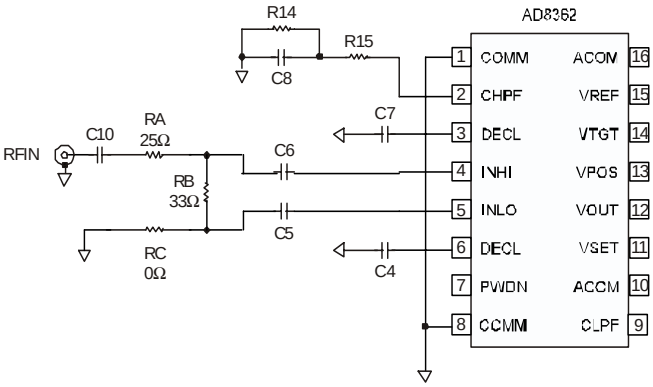


Figure X2 Single-ended Drive Without a Balun – Option A

Alternatively, T1 may be removed, a 0 Ω resistor installed at positions RA and RC and a 100 Ω resistor installed at R16, as shown in Figure X3.

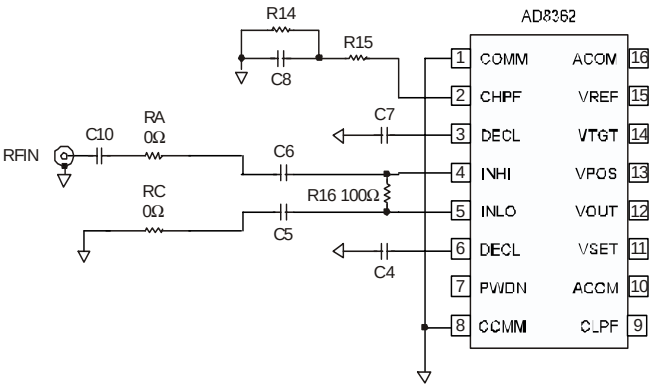


Figure X3 Single ended Drive without a Balun – Option B

Target Voltage

The target voltage can be used to adjust the intercept of the AD8362 transfer function. Nominally, the voltage applied to **VTGT** is the stable, 1.25 V reference voltage produced by a band gap cell on the AD8362, which is available at **VREF**. This is the case when SW1 is in the position shown in Figure XX.

If the voltage at **VTGT** is lowered the intercept is increased, which allows the AD8362 to accurately measure signals with larger crest factors, at the expense of reduced sensitivity to very small input signals. This can be accomplished by installing the appropriate resistor values for R4 and R5, and switching SW1 to connect **VTGT** to LK1. The input incremental resistance at pin VTGT is nominally 52 kΩ, so the value of R5 should be calculated with this in mind.

An external voltage may be applied to connector VTGT. In this case, LK1 should be removed. The external voltage may be a dc voltage higher than that available from **VREF**, which would improve the sensitivity of the AD8362 to small input signals, at the expense of reduced ability to measure large input signals.

Measurement Mode

The AD8362 can be configured in Measurement Mode by externally completing a feedback path from **VOUT** to **VSET**. The slope of the transfer function can be altered by controlling the portion of the voltage present at **VOUT** that is applied to **VSET**. If the entire signal from **VOUT** is applied to **VSET**, as is the case when SW2 is in the position shown in Figure XX, the slope of the transfer function is nominally 50 mV per dB.

The transfer function slope can be increased by adding an external resistor between **VOUT** to **VSET**, which is R17 on the eval board. If this configuration is used, then SW2 should be switched from the position shown in Figure XX or the 0 Ω resistor at R8 should be removed. R9 should be removed from the evaluation board.

$$R_{17} = R_{IN} * \left(\frac{NS}{OS} - 1 \right)$$

R17 forms a voltage divider with the input resistance of VSET, as shown is Figure X4. The formula for R17, in terms of the desired slope (NS), original slope (OS) and input resistance of VSET (RIN) is

Since the value of RIN is not tightly controlled or guaranteed, it may be helpful to add an external shunt resistor, in position R9, whose resistance is smaller than the nominal value of RIN, thereby decreasing the sensitivity of the new slope to process variations that might cause the value of RIN to change. In this case, the equation that defines the value of R17 is

$$R_{17} = \left(\frac{R_{IN} * R_9}{R_{IN} + R_9} \right) * \left(\frac{NS}{OS} - 1 \right)$$

If this configuration is used, it is important to provide sufficient load impedance to pin **VOUT** to ensure that it will not be called upon to source more than its specified source /sink current.

Controller Mode

The AD8362 can be configured to operate as a controller, the operation of which is analogous to a comparator. In this configuration, there is no feedback path between pins **VOUT** and **VSET**, so SW2 should be switch from the position shown in Figure XX and R17 should be open.

A set-point voltage is applied to pin **VSET**. If the input signal magnitude is lower than that which corresponds to the set-point voltage, the voltage at pin **VOUT** is a logic low. If the input signal magnitude is increased to a value larger than that which corresponds to the set-point voltage, the voltage at pin **VOUT** will go to logic high.

The set-point voltage that will cause the AD8362 to toggle at a given input signal level is simply the voltage would be produced at **VOUT** if the AD8362 were configured in Measurement Mode.

Power Down

Switch SW3 allows the **PWDN** pin to be connected either to the supply line voltage, V_{POS}, in order to disable the AD8362, or to a pull-down resistor to which an externally-generated logic level may be applied. The AD8362 is enabled by a low logic level applied to the **PWDN** pin, which may also be directly grounded.

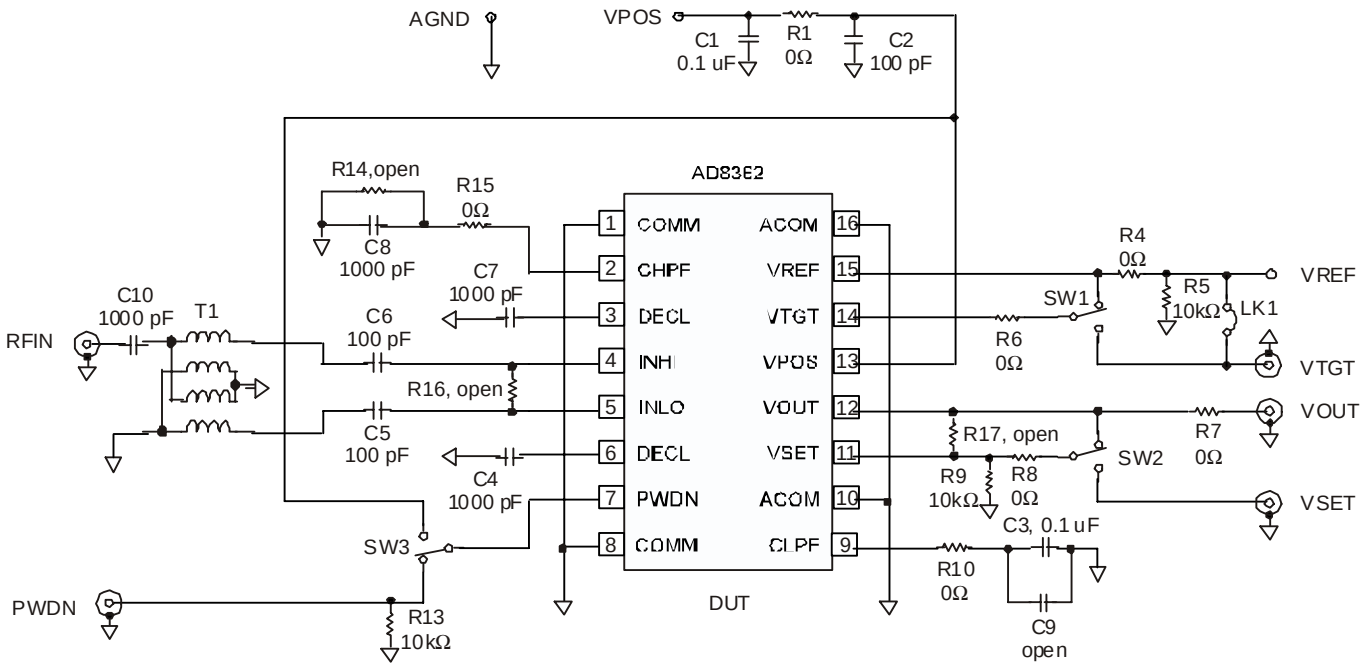


Figure XX. Evaluation Board Schematic

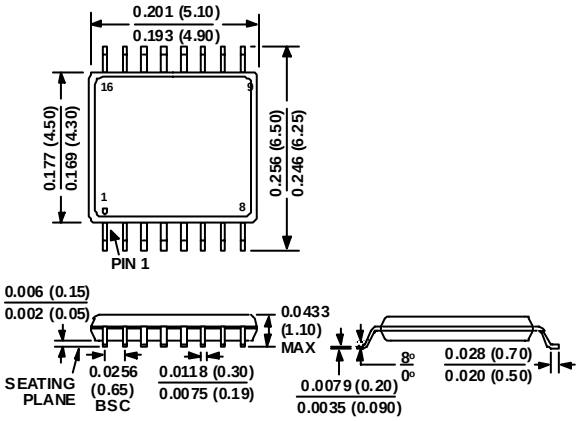
Table II Evaluation Board Configuration Options

Component	Function	Part Number	Default Value
T1		ETC1.6-4-2-3	
C1	Supply filtering/decoupling capacitor		0.1 µF
C2	Supply filtering/decoupling capacitor		100 pF
C3	Output low pass filter capacitor		0.1 µF
C9	Output low pass filter capacitor (normally omitted, not installed)		
C4, C7, C10	Input bias-point decoupling capacitors		1000 pF
C5, C6	Input signal coupling capacitors		100 pF
C8	Input high pass filter capacitor		1000 pF
DUT	AD8362	AD8362ARU	
R1, R4, R6, R7, R8, R10, R15			0 Ω
R5, R9, R13	Optional pull-down resistors		10k Ω
R16	(not installed, see text)		100 Ω
R17	Slope adjustment (not installed, see text)		(See text)
RA	(Not installed, see text)		25 Ω or 0 Ω
RB	(Not installed, see text)		33 Ω
RC	(Not installed, see text)		0 Ω
SW1	Internal/external target voltage selector		
SW2	Measurement mode/controller mode selector		
SW3	Powerdown/enable or external power down selector		

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead TSSOP
(RU-16)



Rev. PrN 02/07/02

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