OKI Semiconductor

This version: Jan. 1998
Previous version: Nov. 1996

MSM7557

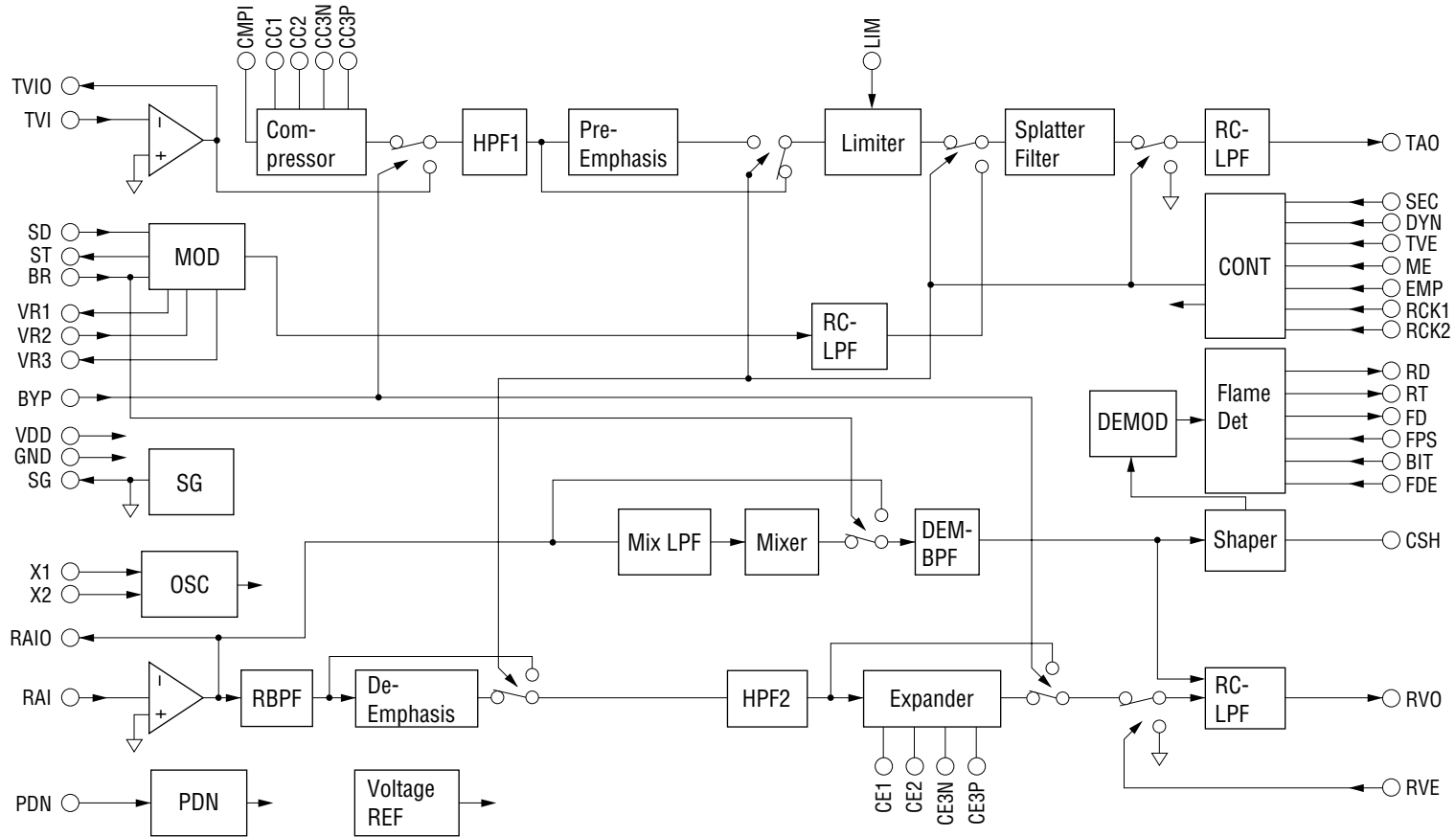## Single Chip MSK Modem with Compandor for Cordless Telephone

GENERAL DESCRIPTION

The MSM7557 is a single chip MSK modem with base band voice processor for cordless telephone.
The MSM7557 voice transmit block consists of high pass filter, compressor, pre-emphasis, limiter and splatter filter.
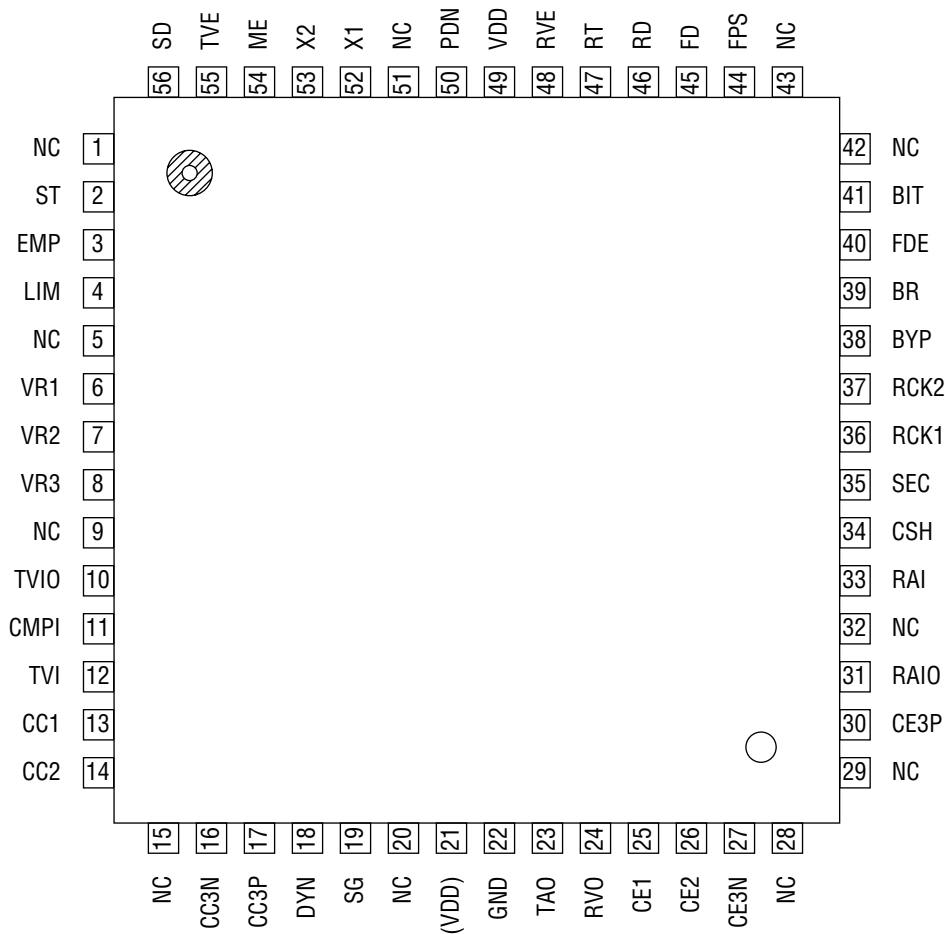Voice receive block consists of Band pass filter, De-emphasis and Expander.

FEATURES

- Available to transmit modem signal and also transmit base band voice signal through wireless transmission path (0.3 kHz to 3.4 kHz)
- Built-in compandor circuit
- Upper limit of voice band (3306 Hz/3400 Hz/3500 Hz) is selectable
- Modem bit rate (2400/1200 bps) is selectable
- Transmit function and receive function operate separately
- Emphasis mode selectable
- Built-in bit synchronous detector and frame synchronous detector
- Built-in limiter level generator and external limit voltage input
- Dynamic range selectable
- Built-in crystal oscillator circuit
- Wide range power supply voltage (2.7V ~ 5.5V)
- Package :
  56-pin plastic QFP   (QFP56-P-910-0.65-2K) (Product name : MSM7557GS-2K)

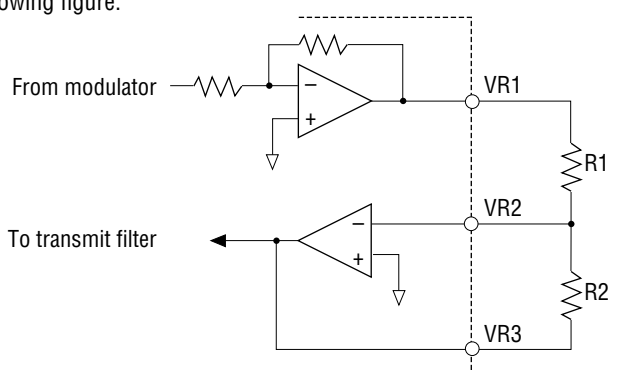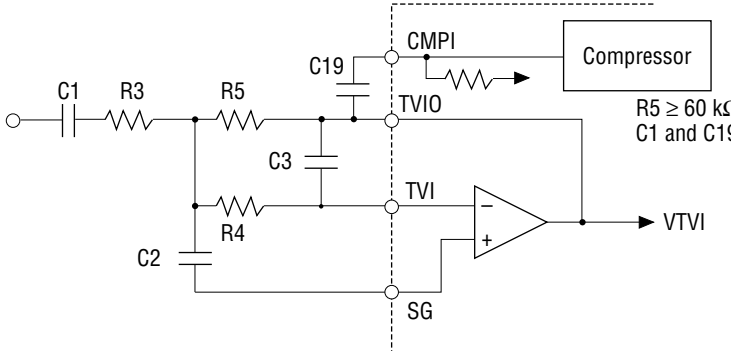**OKI** Semiconductor   **MSM7557**

PIN CONFIGURATION (TOP VIEW)

Top pins (left to right, 56–43): SD(56), TVE(55), ME(54), X2(53), X1(52), NC(51), PDN(50), VDD(49), RVE(48), RT(47), RD(46), FD(45), FPS(44), NC(43)

Left pins (top to bottom, 1–14):
1	NC
2	ST
3	EMP
4	LIM
5	NC
6	VR1
7	VR2
8	VR3
9	NC
10	TVIO
11	CMPI
12	TVI
13	CC1
14	CC2

Right pins (top to bottom, 42–29):
42	NC
41	BIT
40	FDE
39	BR
38	BYP
37	RCK2
36	RCK1
35	SEC
34	CSH
33	RAI
32	NC
31	RAIO
30	CE3P
29	NC

Bottom pins (left to right, 15–28): NC(15), CC3N(16), CC3P(17), DYN(18), SG(19), NC(20), (VDD)(21), GND(22), TAO(23), RVO(24), CE1(25), CE2(26), CE3N(27), NC(28)

Notes: The pin 49 should be used for V_{DD}.
The pin 21 should be connected to V_{DD} or opened.
NC : No connect pin

PIN DESCRIPTION

Name	Description
SD	Transmit data input. The data on SD pin are took into MSK modulator and the data are available on the positive edge of ST. In order to synchronize a receive modem, more than 18bits bit-synchronous signal should be transmitted before data transmission. If S/N ratio of the receive signal is always good, more than 11bits bit-synchronous signal synchronizes the receiver.
ST	Transmit data timing clock output. When digital "0" is put on ME pin, ST is fixed to digital "1" level.

Emphasis path selection.

	EMP	Transmit side	Receive side
EMP	0	Pre-emphasis circuit is bypassed to the path	De-emphasis circuit is bypassed to the path
	1	Pre-emphasis circuit is connected to the path	De-emphasis circuit is connected to the path

Deviation limiter control.

Voice signal maximum Rf modulation level is controlled by connecting external reference voltage to this pin.

Input impedance of this pin is about 200 kΩ.

When this pin is left open, internal reference voltage is used as the clamp level.

Internal clamp level is as follows.

	DYN	Internal clamp level	Limiter level
LIM	0	0.50 V	−9 dBV
	1	1.26 V	−1 dBV

This internal clamp level is made by internal reference voltage which is unrelated with V_{DD}.

Negative clamp level is made by internal operational amplifier and the voltage is reversed at VSG.

OKI Semiconductor | **MSM7557**

(Continued)

Name	Description
VR1 VR2 VR3	Modulator output level control. Refer to the following figure. $R1 \geq 40\ k\Omega$ $R2 \geq 40\ k\Omega$ $R1 \geq R2$ $V_{TAO} = 20 \times \log (R2/R1) - 9\ dBV$ (DYN = "0") $V_{TAO} = 20 \times \log (R2/R1) - 1\ dBV$ (DYN = "1") This level is made from internal voltage reference, so this level doesn't depend on power supply voltage.
TVIO TVI	Transmit side RC active filter input (TVI) and output (TVIO). If over 50 kHz frequency element is in the input signal, folding noise is generated from internal SCF circuit, so second order RC-active filter is needed. (fc = 10 kHz) $R5 \geq 60\ k\Omega$ C1 and C19 are used for DC cut. Example of fc = 10 kHz and 0 dB gain R3 = R4 = R5 = 68 kΩ C1 = 0.22 μF, C2 = 510 pF, C3 = 110 pF When digital "1" is applied to TVE pin, transmit voice signal comes out to TAO.
CC1 CC2	Capacitor connection pins to remove for DC offset of the compressor. A 1 μF capacitor between SG pin and each pin should be connected.
CC3N CC3P	Capacitor connection pins for the compressor attack and recovery time. When DYN is digital "0" level, a 0.22 μF capacitor should be connected between CC3N and CC3P. And when DYN is digital "1" level, a 0.47 μF capacitor should be connected between them.

OKI Semiconductor   **MSM7557**

(Continued)

Name	Description
CMPI	Compressor circuit input. A 0.47 μF capacitor should be connected between CMPI and TVIO.
DYN	Dynamic range control input. For an application of which V_{DD} is always higher than 4.5 V (Base station), by setting DYN = "1", modem transmit carrier level, typical input signal level, limiter clamp level and compandor standard input level are up about 8dB to improve S/N ratio. For an application of which V_{DD} is lower than 4.5 V (Hand-set) DYN shall be digital "0". To make easier interface with the RF part, one solution is to put digital "0" on DYN pin for both Base station and Handset.
SG	Built-in analog signal ground. The DC voltage is half of V_{DD}. To make this voltage source impedance lower and to ensure the device performance, it is necessary to put a bypass capacitor of more than 1μF between SG and V_{DD} in close physical proximity to the device.
GND	Ground pin, (0V).
TAO	Transmit analog signal output. According to control data on ME and TVE, TAO is set as follows. TABLE_TAO
RVO	Receive voice signal output. RVO pin state is defined by RVE control. TABLE_RVO
CE1 CE2	Capacitor connection pins to remove DC offset of the expander. A 1 μF capacitor between SG pin and each pin should be connected.
CE3N CE3P	Capacitor connection pins for the expander attack time and recovery time. When DYN is digital "0" level, a 0.22 μF capacitor should be connected between CE3N and CE3P. And when DYN is digital "1" level, a 0.47 μF capacitor should be connected between them.
RAIO RAI	Receive side amplifier input (RAI) and output (RAIO). Second order RC-active filter is needed like TVIO and TVI. Refer to TVIO and TVI pin description.
CSH	Capacitor connection pin to remove DC offset of the modem shaper circuit. A 1 μF capacitor should be connected between GND pin and CSH.

TABLE_TAO:

ME	TVE	TAO
0	0	No signal output (potential = SG)
0	1	Voice signal output
1	X	MSK modulator output

X : Don't care

TABLE_RVO:

RVE	RVO
0	Output disable (potential = SG)
1	Output enable

(Continued)

Name	Function
SEC	Device test input. SEC shall be connected to GND.
RCK1 RCK2	Voice band select. | RCK1	RCK2	Upper Limit of Voice Band | |------|------|---------------------------| | 0 | 1 | 3306 Hz | | X | 0 | 3400 Hz | | 1 | 1 | 3500 Hz |
BYP	Compandor path selection. | BYP	Transmit side	Receive side | |-----|---------------|--------------| | 0 | Compressor is connected to the path. | Expander is connected to the path. | | 1 | Compressor is bypassed to the path. | Expander is bypassed to the path. |
BR	Modem data signaling rate select pin. | BR	Date signaling rate | |----|---------------------| | 0 | 1200 bps | | 1 | 2400 bps |

OKI Semiconductor   **MSM7557**

(Continued)

Name	Function
FDE	Frame synchronous signal detector control. When digital "0" is applied to this pin, FD pin is fixed to "0" level. RT and RD always work. When digital "1" is applied to this pin, frame synchronous detector works, and RT and RD pins are fixed to "1" level untill synchronous signal detector detects frame synchronous signal and FD becomes "1" level. Refer to Fig.3 (receive signal timing).
BIT	Bit synchronous signal detector control. When BIT and FDE pins are digital "1" level and when bit synchronous signal and frame synchronous signal are detected continously, FD becomes digital "1". When BIT pin is digital "0" level and FDE pin is digital "1" level and when 16-bit frame synchronous signal is detected, FD pin becomes digital "1" level. Refer to FPS pin detection.
FPS	Frame synchronous pattern control. <table><tr><th>BIT</th><th>FPS</th><th>Detect pattern</th><th>Receiver</th></tr><tr><td>0</td><td>0</td><td>1001 0011 0011 0110 (=9336H)</td><td>Handset side</td></tr><tr><td>0</td><td>1</td><td>1100 0100 1101 0110 (=C4D6H)</td><td>Base station</td></tr><tr><td>1</td><td>0</td><td>1010 1001 0011 0011 0110 (=A9336H)</td><td>Handset side</td></tr><tr><td>1</td><td>1</td><td>1010 1100 0100 1101 0110(=AC4D6H)</td><td>Base station</td></tr></table>(Note : This pattern is for Japanese Cordless Telephone.)
FD	Frame synchronous detector output. When receive data correspond to detection pattern, FD pin is held to digital "1" level. When FDE is applied to digital "0" level, FD pin is reset to digital "0" level. And at the full power down state (PDN = "1", RVE = "0"), FD pin is reset to digital "0" level.
RD	Demodulator serial data output. The data are synchronized with the re-generated timing clock of RT. When FDE is digital "1" level and also FD is digital "0" level, RD is fixed to digital "1" level.
RT	Receive data timing clock output. This signal is re-generated by internal digital PLL. The falling edge of this clock output is coincident with the transitions of RD. The rising edge of RT can be used to latch the valid receive data. When FDE pin is applied to digital "1" level and also FD pin output digital "0" level, RT pin is fixed to digital "1" level. Refer to Fig.3.
RVE	Receive voice signal control. Refer to RVO pin description.
V_{DD}	Power supply. This device is sensitive to power supply noises as switched capacitor tequniques are utilized. A bypass capacitor of more than 10 μF between V_{DD} and GND pin should be connected to ensure the performance.

OKI Semiconductor   **MSM7557**

(Continued)

Name	Function
PDN	Power down control. Power down state is controlled by PDN, ME, RVE, and TVE. (table below) At the mode 4, all functions are powered on. At the full power down mode(PDN = "1" and RVE = "0"), the demodulator circuit and FD pin are reset. When V_{DD} is turned ON, the demodulator circuit and FD pin should be reset by setting Mode1.

	PDN	ME	RVE	TVE	Voice control path	Transmit side modem	Receive side modem
Mode1	1	X	0	X	OFF	OFF	OFF
Mode2	1	X	1	X	OFF	OFF	ON
Mode3	0	1	0	0	OFF	ON	ON
Mode4	others				ON	ON	ON

X : Don't care

Name	Function
X1 X2	Crystal connection. 3.6864 MHz crystal shall be connected. When an external master clock is applied, the clock should be supplied to X2 pin via a 200 pF capacitor for AC coupling and X1 should be opened.
ME	MSK moudulator output. When digital "1" is applied to this pin, MSK modulator is connected to the splatter filter. Refer to TAO pin description.
TVE	Transmit side voice signal contorol. Refer to TAO pin description.

OKI Semiconductor   **MSM7557**

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C Refer to GND	−0.3 to +7.0	V
Analog Input Voltage *1	V_{IA}		−0.3 to V_{DD} + 0.3	
Digital Input Voltage *2	V_{ID}			
Storage Temperature	T_{STG}	—	−55 to +150	°C

*1 : LIM, VR2, TVI, RAI, CMPI
*2 : SD, EMP, DYN, SEC, RCK1, RCK2, BYP, BR, FDE, BIT, FPS, RVE, PDN, X2, ME, TVE

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	from GND level	DYN = "0"	2.7	3.6	5.5	V
			DYN= "1"	4.5	5.0	5.5	
Operating Temperature	T_{op}	V_{DD} = 2.7 V to 5.5 V		−30	+25	+70	°C
Crystal Oscillating Freq.	$f_{X'TAL}$	—		3.6860	3.6864	3.6868	MHz
Data Signaling Rate	T_S	BR = 0"		—	1200	—	bit/sec
		BR = "1"		—	2400	—	
C4, C5, C11, C12, C15	—	—		—	1.0	—	μF
C6, C13	—	DYN = "0"		—	0.22	—	
	—	DYN = "1"		—	0.47	—	
C7, C8	—	—		—	1.0	—	
C9, C10	—	RL ≥ 40kΩ		—	0.22	—	
C14	—	—		—	10	—	
C19	—	—		—	0.47	—	
C20, C21	—	—		—	20	—	pF

OKI Semiconductor   **MSM7557**

ELECTRICAL CHARACTERISTICS

DC Characteristics

$\left(\begin{array}{l} \text{DYN = "0" : } V_{DD} = 2.7 \text{ V to } 5.5 \text{ V, Ta} = -30°C \text{ to } 70°C \\ \text{DYN = "1" : } V_{DD} = 4.5 \text{ V to } 5.5 \text{ V, Ta} = -30°C \text{ to } 70°C \end{array} \right)$

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Power Supply Current *1	I_{DD}	Normal mode (mode 4)	3.6 V	—	9.0	18	mA
			5.5 V	—	14.0	24	
	I_{DDS1}	Power down mode 1	5.5 V	—	1.0	20	μA
	I_{DDS2}	Power down mode 2	3.6 V	—	3.8	7.0	mA
	I_{DDS3}	Power down mode 3		—	4.6	9.0	
Input Leakage Current *2	I_{IL}	$V_{IN} = 0$ V		−10	—	+10	μA
	I_{IH}	$V_{IN} = V_{DD}$					
Input Voltege *2	I_{IL}	—		0	—	$0.2V_{DD}$	V
	I_{IH}			$0.7V_{DD}$	—	V_{DD}	
Output Voltege *3	V_{OL}	$I_{OL} = -20$ μA		0	—	$0.1V_{DD}$	
	V_{OH}	$I_{OH} = 20$ μA		$0.8V_{DD}$	—	V_{DD}	

*1 Refer to PDN pin description
*2 SD, EMP, DYN, SEC, RCK1, RCK2, BYP, BR, FDE, BIT, FPS, RVE, PDN, ME, TVE
*3 ST, FD, RD, RT

OKI Semiconductor

AC Characteristics

$$\left(\begin{array}{l} \text{DYN = "0" : } V_{DD} = 2.7 \text{ V to } 5.5 \text{ V, Ta} = -30°C \text{ to } 70°C \\ \text{DYN = "1" : } V_{DD} = 4.5 \text{ V to } 5.5 \text{ V, Ta} = -30°C \text{ to } 70°C \end{array} \right)$$

Parameter		Symbol	Condition		Min.	Typ.	Max.	Unit
Transmit Carrier Frequency		f_{M1}	SD = "1"	BR = "0"	1199	1200	1201	Hz
		f_{S1}	SD= "0"	ME= "1"	1799	1800	1801	
		f_{M2}	SD = "1"	BR = "1"	1199	1200	1201	
		f_{S2}	SD= "0"	ME= "1"	2399	2400	2401	
Transmit Carrier Level		V_{OX}	R1 = R2	DYN = "0"	−11	−9	−7	dBV
				DYN = "1"	−3	−1	+1	
Receive Carrier Input Level		V_{IR}			−32	—	−2	
Bit Error Rate	1200 bps	B_{ER}	Defined at RAIO	8 dB	—	1×10^{-3}	—	—
				10 dB	—	5×10^{-5}	—	
	2400 bps			11 dB	—	1×10^{-3}	—	
				13 dB	—	5×10^{-5}	—	
Number of PLL Lock-in Data Bits *1		V_{IR}	Number of data bits required for the PLL to be locked in within the phase difference of 22.5° or less		—	—	18	bit
			Number of data bits required for the PLL to be locked in within the phase difference of 90° or less		—	—	11	

*1 Receive MSK signal is bit synchronous signal (modulated signal of alternating "0", "1" pattern).

OKI Semiconductor   **MSM7557**

Voice Signal Interfaces

$\left(\begin{array}{l} \text{DYN = "0" : } V_{DD} = 2.7 \text{ V to } 5.5 \text{ V, Ta} = -30°\text{C to } 70°\text{C} \\ \text{DYN = "1" : } V_{DD} = 4.5 \text{ V to } 5.5 \text{ V, Ta} = -30°\text{C to } 70°\text{C} \end{array}\right)$

Parameter		Symbol	Condition		Min.	Typ.	Max.	Unit
RVO Maximum Output Signal Level		V_{OUT}	f_{IN} = 1 kHz BYP = "0" *1	DYN = "0"	—	—	−6	dBV
				DYN = "1"	—	—	+2	
Limiter Clamp Level		V_{LIM}	f_{IN} = 1 kHz LIM = open	DYN = "0"	−10	−9	−8	
				DYN = "1"	−2	−1	0	
Transmit Output Distortion		H_{DT}	f_{IN} = 1 kHz, −12 dBV BYP = "0", EMP = "1"		—	−40	—	dB
Receive Output Distortion		H_{DR}			—	−40	—	
Transmit Gain		G_T	f_{IN} = 1 kHz, BYP = EMP = "1"		−1.5	−0.2	+1	
Receive Gain		G_R	f_{IN} = 1 kHz, BYP = EMP = "1"		−1.5	−0.2	+1	
Transmit Idle Noise		H_{IT}	BYP = "0"		—	−51	—	dBV
Receive Idle Noise		H_{IR}	EMP = "1"		—	−85	—	
Cross Talk	$R_{CV.} \rightarrow T_{ran.}$	C_{TT}	RAIO = −2 dBV	*2	—	−75	−60	
	$T_{ran.} \rightarrow R_{CV.}$	C_{TR}	TVIO = −2 dBV		—	−80	−60	
Transmit Filter Response		FT1	EMP = "1" BYP = "1" RCK2 = "0" Ref. = 1 kHz	100 Hz	—	−28	−23	dB
		FT3		300 Hz	−12.5	−10.5	−8.5	
		FT25		2.5 kHz	+6.5	+8.0	+9.5	
		FT34		3.4 kHz	+8.5	+10.5	+12.5	
		FT60		6 kHz	—	−40	−30	
Receive Filter Response		FR1	EMP = "1" BYP = "1" RCK2 = "0" Ref. = 1 kHz	100 Hz	+1.5	+3.0	+4.5	
		FR3		300 Hz	+8.0	+9.5	+11.0	
		FR25		2.5 kHz	−9.5	−8.0	−6.5	
		FR34		3.4 kHz	−12.5	−10.5	−8.5	
		FR60		6 kHz	—	−40	−30	

*1 S/D ≥ 20 dB

*2 f_{IN} = 1 kHz, BYP = EMP = "1"

OKI Semiconductor   MSM7557

(Continued)

$$\left(\begin{array}{l} \text{DYN = "0" : } V_{DD} = 2.7 \text{ V to } 5.5 \text{ V, Ta} = -30°C \text{ to } 70°C \\ \text{DYN = "1" : } V_{DD} = 4.5 \text{ V to } 5.5 \text{ V, Ta} = -30°C \text{ to } 70°C \end{array} \right)$$

	Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Compressor	Standard Input Level	V_{ICS}	f_{IN} = 1 kHz	DYN = "0"	−16.1	−13.7	−11.3	dBV
				DYN = "1"	−7.1	−5.5	−3.9	
	Maximum Input Level	V_{ICM}		DYN = "0"	—	—	−7	
				DYN = "1"	—	—	+1.0	
	Output Level *3	GC2	f_{IN} = 1 kHz	−20 dB	−10.6	−9.9	−9.2	dB
		GC4		−40 dB	−21.0	−19.8	−18.6	
		GC5		−60 dB	—	−29.5	—	
	Attack Time	T_{AT1}	DYN = "0", C6 = 0.22 μF		—	3.4	—	ms
		T_{AT2}	DYN = "1", C6 = 0.47 μF		—	3.5	—	
	Recovery Time	T_{RE1}	DYN = "0", C6 = 0.22 μF		—	17	—	
		T_{RE2}	DYN = "1", C6 = 0.47 μF		—	16	—	
Expander	Standard Input Level	V_{IES}	f_{IN} = 1 kHz	*4	−12.9	−10.8	−8.7	dBV
				*5	−13.3	−11.2	−9.1	
				*6	−4.7	−3.1	−1.5	
	Maximum Output Level	V_{IEM}		DYN = "0"	—	—	−6	
				DYN = "1"	—	—	+2	
	Output Level	GE1	f_{IN} = 1 kHz *3	−10 dB	−21.5	−20	−18.3	dB
		GE2		−20 dB	−42.2	−40	−37.5	
		GE3		−30 dB	—	−59	—	
	Attack Time	T_{AT3}	DYN = "0", C13 = 0.22 μF		—	3.4	—	ms
		T_{AT4}	DYN = "1", C13 = 0.47 μF		—	3.5	—	
	Recovery Time	T_{RE3}	DYN = "0", C13 = 0.22 μF		—	17	—	
		T_{RE4}	DYN = "1", C13 = 0.47 μF		—	16	—	

*3   0 dB is defined as the input level and the output level when the standard input level is input.

*4 V_{DD} = 3.6 V, DYN = "0"

*5 V_{DD} = 5.0 V, DYN = "0"

*6 V_{DD} = 5.0 V, DYN = "1"

OKI Semiconductor　　　　　　　　　　　　　　　　　　　　　　　　　　　**MSM7557**

Common Characteristics

$\left(\begin{array}{l} \text{DYN = "0" : } V_{DD} = 2.7 \text{ V to } 5.5 \text{ V, Ta} = -30°C \text{ to } 70°C \\ \text{DYN = "1" : } V_{DD} = 4.5 \text{ V to } 5.5 \text{ V, Ta} = -30°C \text{ to } 70°C \end{array} \right)$

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Input Resistance	R_{IA}	TVI, RAI, VR2		—	10	—	MΩ
	R_{IC}	LIM		—	200	—	kΩ
Output Resistance	R_{OX1}	TAO		—	1750	—	Ω
	R_{OX2}	VR1, VR3, RVO		—	600	—	
	R_{OX3}	TVIO, RAIO		—	100	—	
Output Load Resistance	RXL1	S/D ≥ 20 dB	*1	40	—	—	kΩ
	RXL2		TVIO	60	—	—	
Output DC Voltage	V_{SG}	SG		$\dfrac{V_{DD}}{2} - 0.1$	$\dfrac{V_{DD}}{2}$	$\dfrac{V_{DD}}{2} + 0.1$	V
	V_{AO}	TAO, RVO		$\dfrac{V_{DD}}{2} - 0.15$	$\dfrac{V_{DD}}{2}$	$\dfrac{V_{DD}}{2} + 0.15$	

*1　VR1, VR3, TAO, RVO, RAIO

Digital Timing Characteristics

$\left(\begin{array}{l} \text{DYN = "0" : } V_{DD} = 2.7 \text{ V to } 5.5 \text{ V, Ta} = -30°C \text{ to } 70°C \\ \text{DYN = "1" : } V_{DD} = 4.5 \text{ V to } 5.5 \text{ V, Ta} = -30°C \text{ to } 70°C \end{array} \right)$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit Data Set-up Time	t_S	Refer to Fig. 1	1	—	—	μs
Transmit Data Hold Time	t_H		1	—	—	
Receive Data Output Delay	t_D	Refer to Fig. 1	−300	—	300	ns
Sync-signal Output Delay (ME→ST)	t_{MS}	Refer to Fig. 1	0	—	834	μs

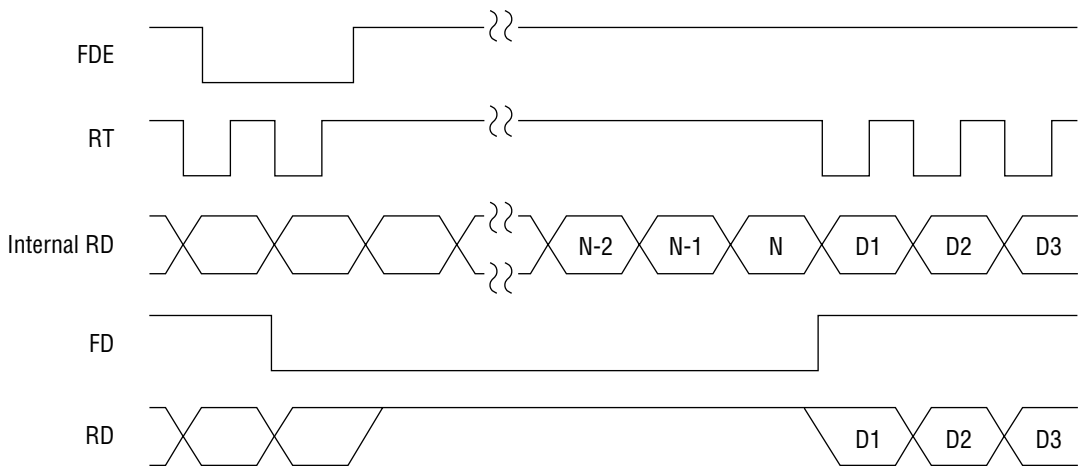## TIMING DIAGRAM
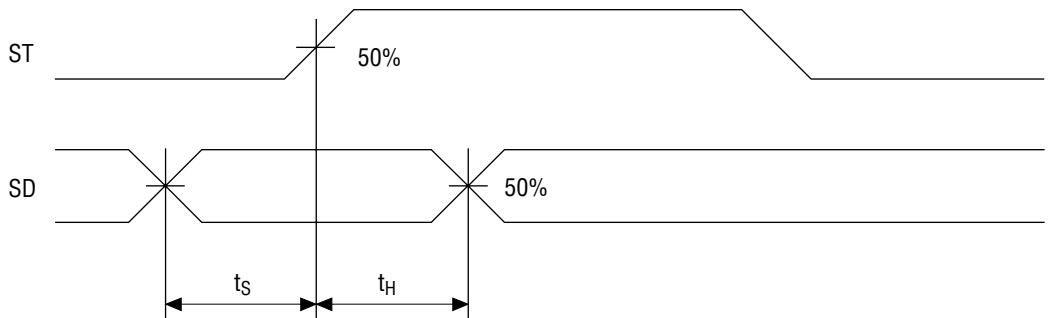
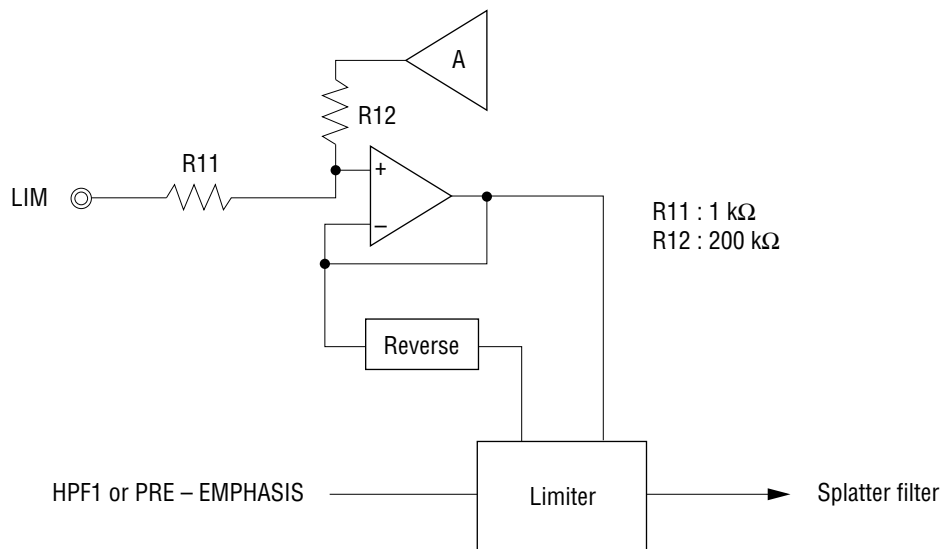**Figure 1 Input Data Timing**
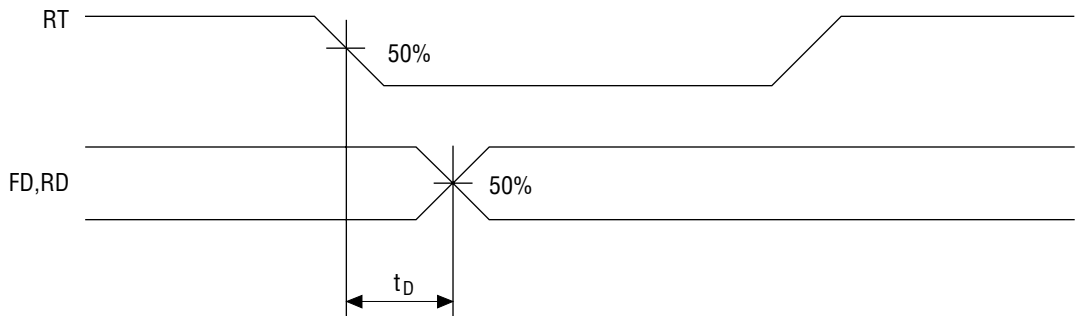
Figure 2 Output Data Timing

N-2, N-1, N : Frame shnchronous signal

Figure 3 Receive Signal Timing

OPERATION DESCRIPTION

Limiter Circuit

R11 : 1 kΩ
R12 : 200 kΩ

DYN = "0"   : Clamp level = VSG ±0.50 V
DYN = "1"   : Clamp level = VSG ±1.26 V

2. In case of using external voltage reference

LIM pin shall be supplied over VSG voltage.

Notes   1) R11 is protection resister from external extra voltage.
             2) Resistor value of R11 and R12 changes 0.7 to 1.3 times from the typical value
                 by lot variation and temperature variation.

OKI Semiconductor   **MSM7557**

Frame Detector

Frame detection pattern is defined by BIT and FPS.

BIT	FPS	Sync-pattern	Receiver	Note
0	0	9336H	S.H.	Frame synchronous
0	1	C4D6H	M.T.	Frame synchronous
1	0	A9336H	S.H.	Bit + Frame synchronous
1	1	AC4D6H	M.T.	Bit + Frame synchronous

M.T. = Master telephone
S.H. = Slave handset

Fig 3 shows detection timing
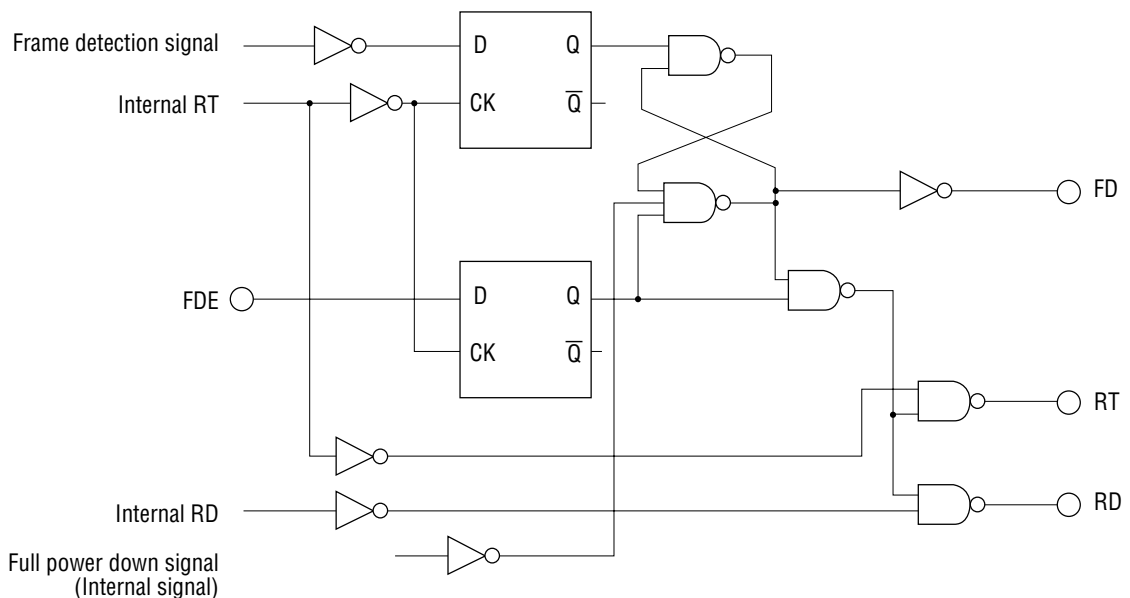First, put digital "0" level to FDE pin more than 1 ms, then FD pin is reset to "0" level.
Next, put digital "1" level to FDE pin, then RT and RD output digital "1" level until frame synchronous signal detected.
When synchronous pattern is detected, FD pin is held to digital "1" level.
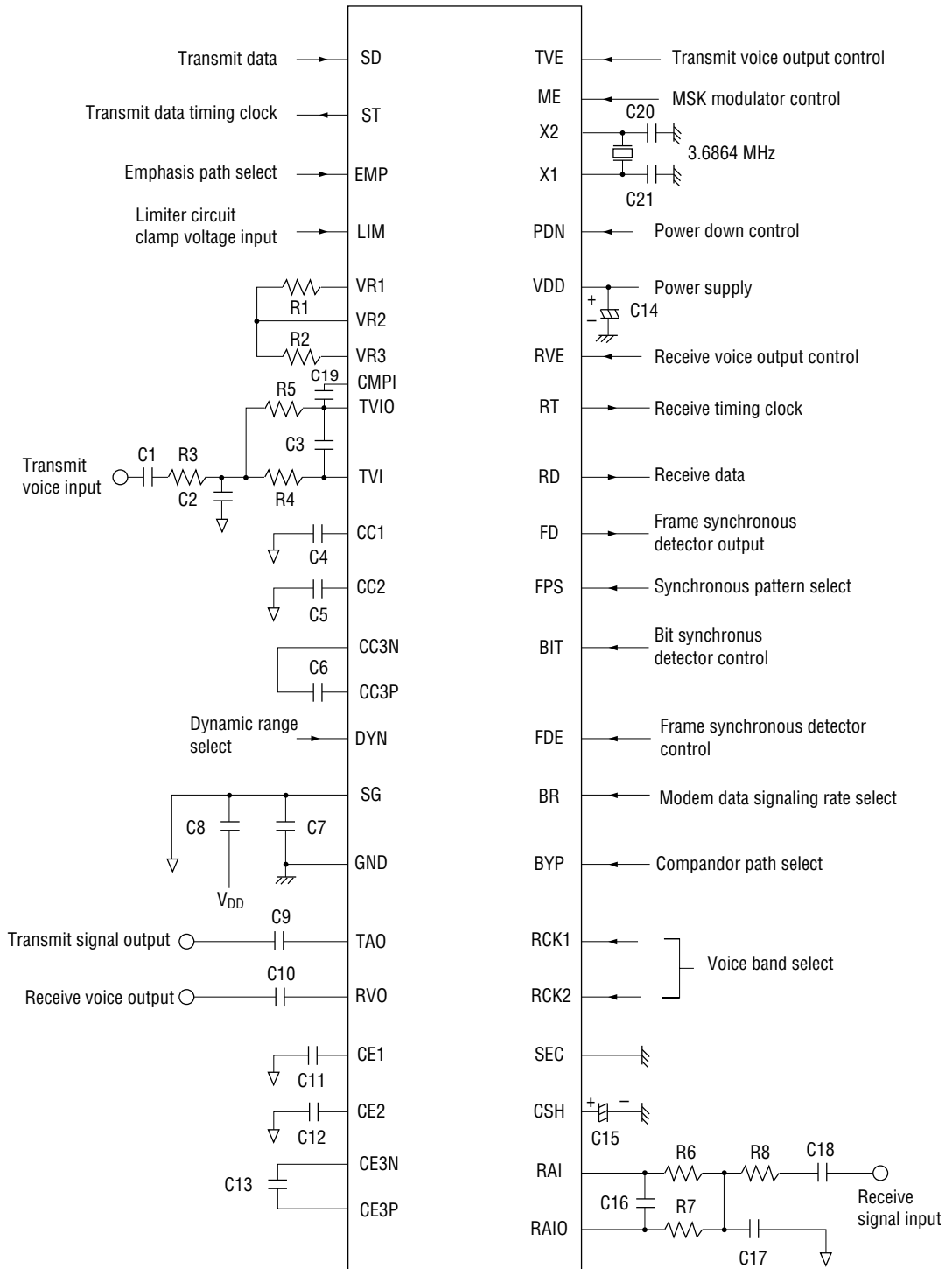At the full power down state (PDN = "1", RVE = "0"), FD pin becomes reset state.
In order to detect frame synchronous signal certainly, receive side PLL should be locked in sufficiently.
When a modem starts data transmittion, the bit-synchronous signal of more than 18 bits should be transmitted before frame pattern of the upper table.

**OKI** Semiconductor   **MSM7557**

Application Circuit

MSM7557GS-2K

Left pins	Right pins
Transmit data → SD	TVE ← Transmit voice output control
Transmit data timing clock ← ST	ME ← MSK modulator control
Emphasis path select → EMP	X2 — C20
	X1 — 3.6864 MHz, C21
Limiter circuit clamp voltage input → LIM	PDN ← Power down control
VR1 R1	VDD — Power supply, C14
VR2 R2	
VR3	RVE ← Receive voice output control
CMPI C19	RT → Receive timing clock
R5 TVIO	
C3	RD → Receive data
Transmit voice input C1 R3 TVI	FD → Frame synchronous detector output
C2 R4	
CC1 C4	FPS → Synchronous pattern select
CC2 C5	BIT → Bit synchronus detector control
CC3N	
C6 CC3P	FDE ← Frame synchronous detector control
Dynamic range select → DYN	BR ← Modem data signaling rate select
SG	BYP ← Compandor path select
C8 C7	
GND	RCK1 ←
V_DD	RCK2 ← Voice band select
Transmit signal output ○ C9 TAO	SEC
Receive voice output ○ C10 RVO	CSH + − C15
CE1 C11	RAI R6 R8 C18
CE2 C12	C16 R7 Receive signal input ○
CE3N	RAIO
C13 CE3P	C17

Note : An arrow mark of (↓) indicates connection to the SG pin.

MSM7557 Filter Characteristics

MSM7557 has wide band filters (0.3 kHz to 3.4 kHz) as follows.

Fig. 4 to Fig. 10 show the filter characteristics when RCK2 is digital "0". When RCK1 is digital "0" and RCK2 is digital "1", the filter characteristics change 0.972 times on the frequency axis. (pass-band becomes narrow) When RCK1 is digital "1" and RCK2 is digital "1", the filter characteristics change 1.029 times on the frequency axis. (pass-band becomes wide)
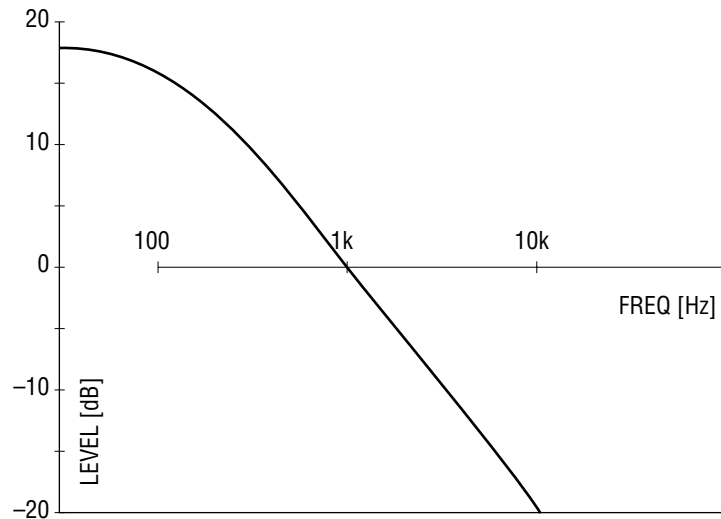
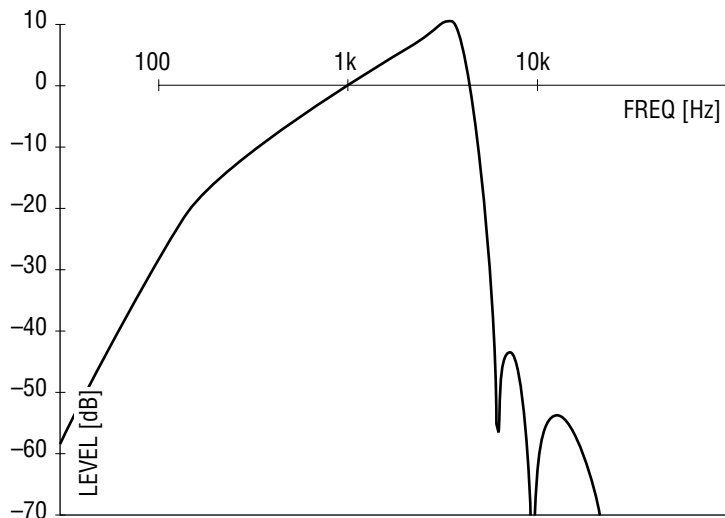**OKI** Semiconductor   **MSM7557**
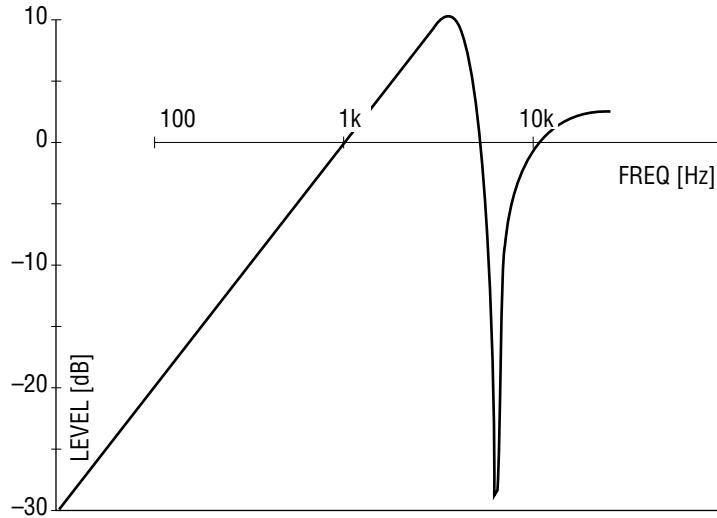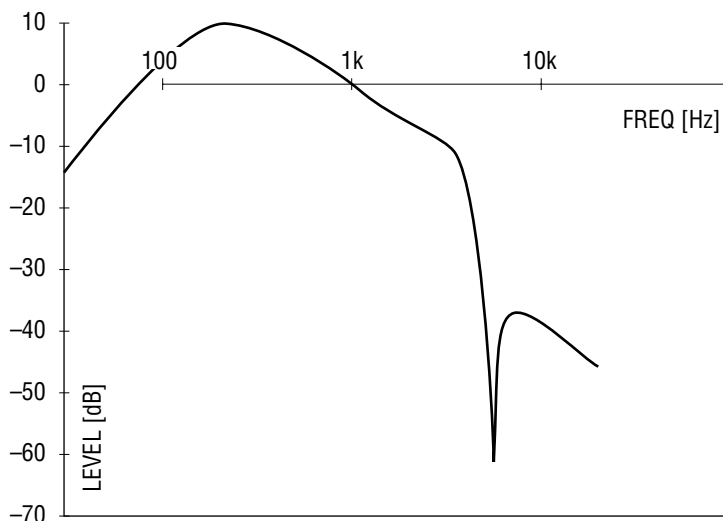

Figure 4 MSM7557 Pre–Emphasis
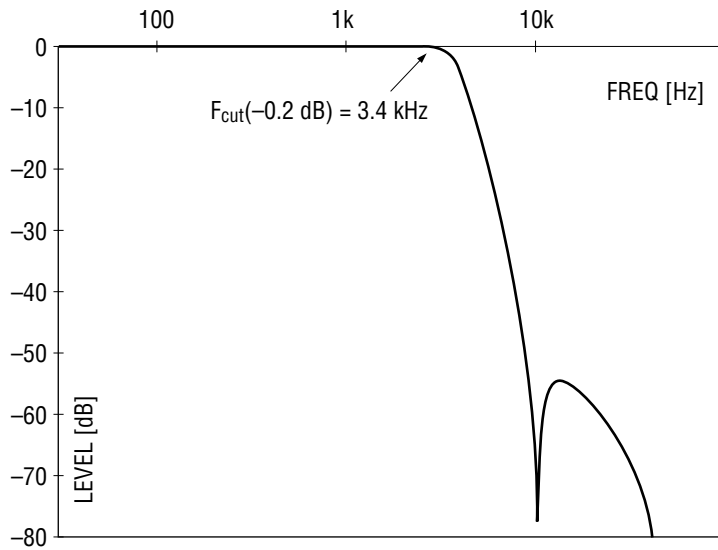
Figure 5 MSM7557 Splatter Filter

OKI Semiconductor   **MSM7557**
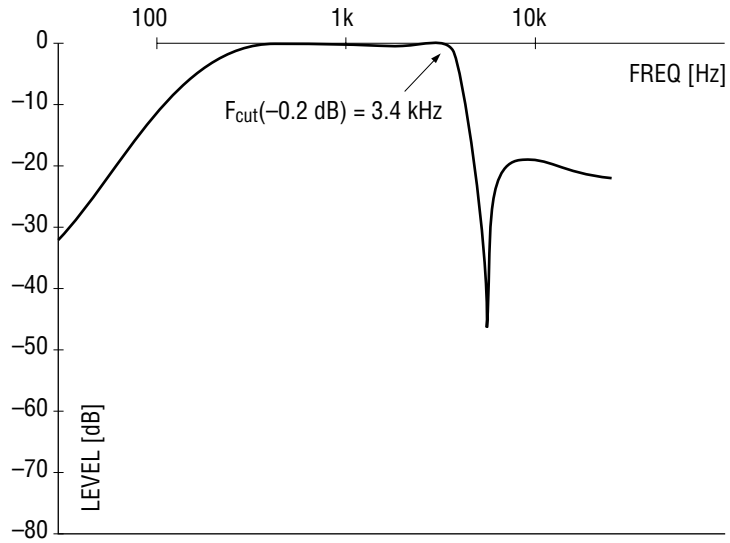
Figure 6 MSM7557 RBPF

Figure 7 MSM7557 De–Emphasis

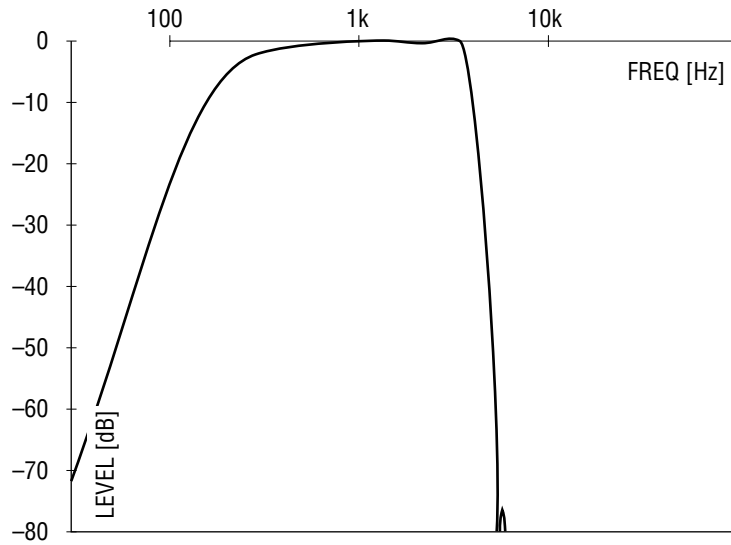**OKI** Semiconductor　　　　　　　　　　　　　　　　　　　　　　　　　　　**MSM7557**

Figure 8 MSM7557 Transmit Total (HPF1 + Pre–Emphasis+Splatter)

Figure 9 MSM7557 Receive Total (RBPF + De–Emphasis)
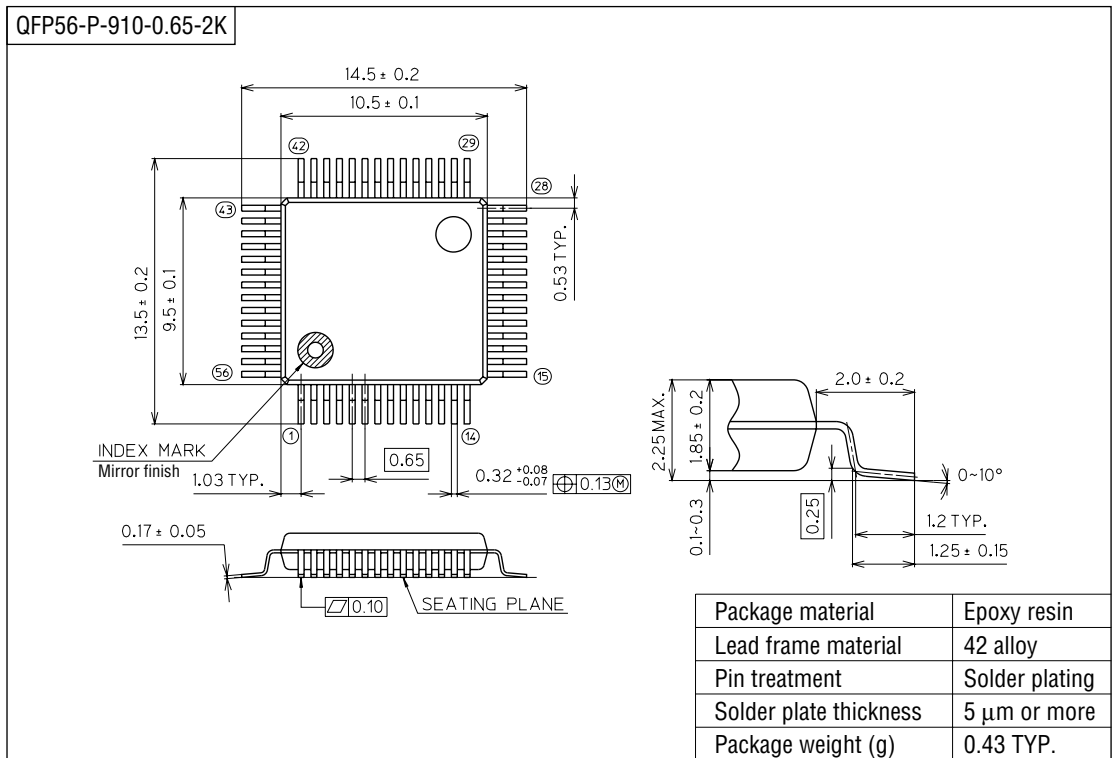
Figure 10 MSM7557 Transmit and Receive Total

OKI Semiconductor　　　　　　　　　　　　　　　　　　　　　　　　　　**MSM7557**

PACKAGE DIMENSIONS

(Unit : mm)

QFP56-P-910-0.65-2K

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.43 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).