

MSM66201/66P201/66207/ 66P207

OLMS-66K Series 16-Bit Microcontroller

GENERAL DESCRIPTION

The MSM66201/66207 is a high performance microcontroller that employs OKI original nX-8/200 CPU core. This chip includes a 16-bit CPU, ROM, RAM, I/O ports, multifunction 16-bit timers, 10-bit A/D converter, serial I/O port, and pulse width modulator (PWM). The MSM66P201/66P207 is the OTP (One-Time Programmable) version of the MSM66201/66207.

FEATURES

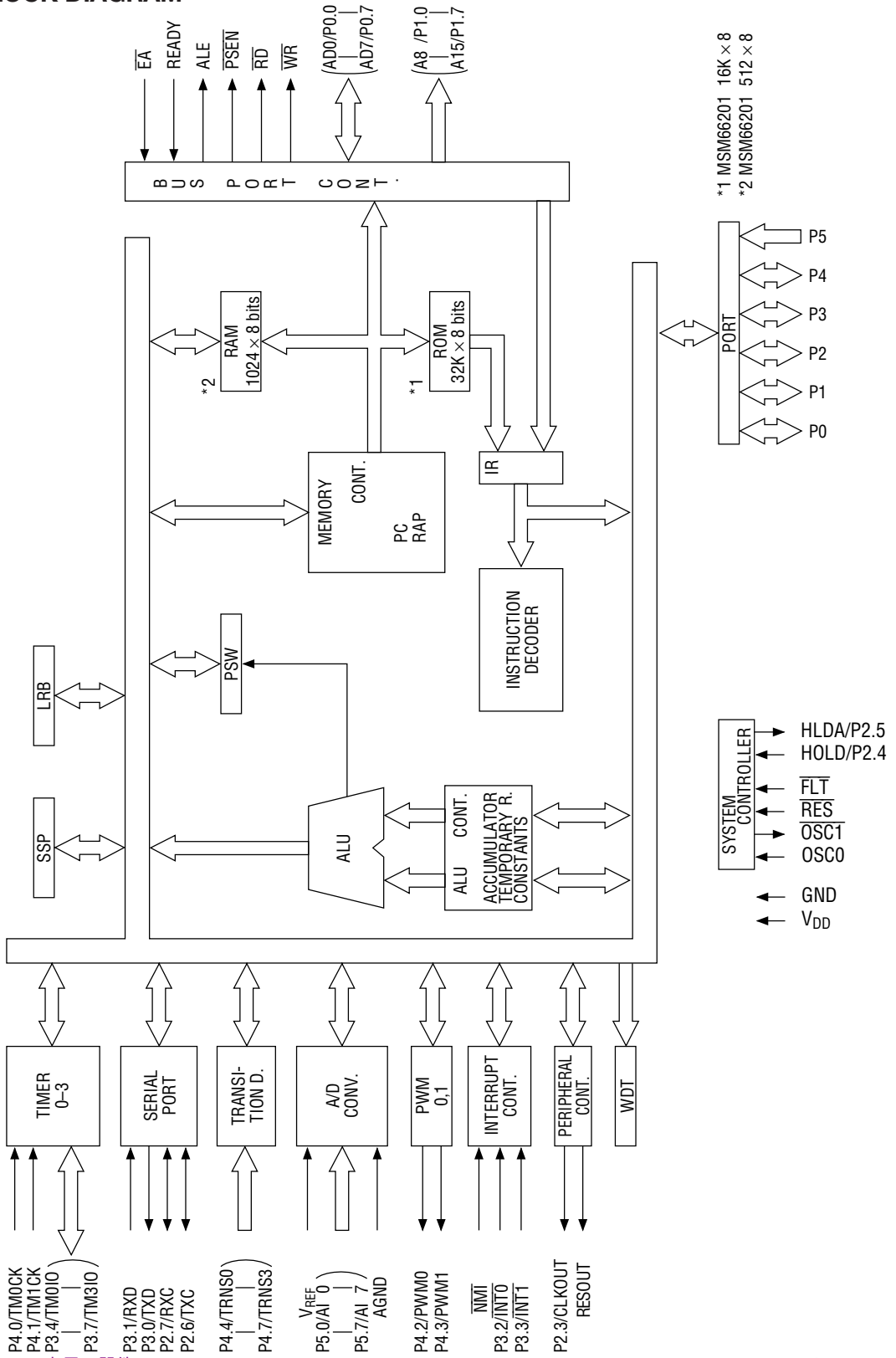
- 64K address space for program memory : Internal ROM : MSM66201 16K bytes
MSM66207 32K bytes
- 64K address space for data memory : Internal RAM : MSM66201 512 bytes
MSM66207 1024 bytes
- High-speed execution : 400ns @ 10MHz
Minimum cycle for instruction
- Powerful instruction set : Instruction set superior in orthogonal matrix
8/16-bit data transfer instructions
8/16-bit arithmetic instructions
Multiplication and division operation instructions
Bit manipulation instructions
Bit logic instructions
ROM table reference instructions
- Abundant addressing modes : Register addressing
Page addressing
Pointing register indirect addressing
Stack addressing
Immediate value addressing
- I/O port : 5 ports × 8 bits
Input-output port (Each bit can be assigned to input or output)
Input port : 1 port × 8 bits
- Built-in multifunctional 16-bit timer : 4
Following 4 modes can be set for each timer : Auto-reload timer mode
Clock output mode
Capture register mode
Real time output mode
- Serial port : 1 channel (Synchronous/UART switchable mode with baud rate generators)
- 16-bit pulse width modulator : 2
- Watchdog timer : 4
- Transition detector : 4
- 10-bit A/D converter : 8 channels
- Interrupts : 1
Nonmaskable : Internal 16/external 2
Maskable
- Stand-by function : Software clock stop mode
STOP mode : Software CPU stop mode
HALT mode : Hardware CPU stop mode
HOLD mode

• Package

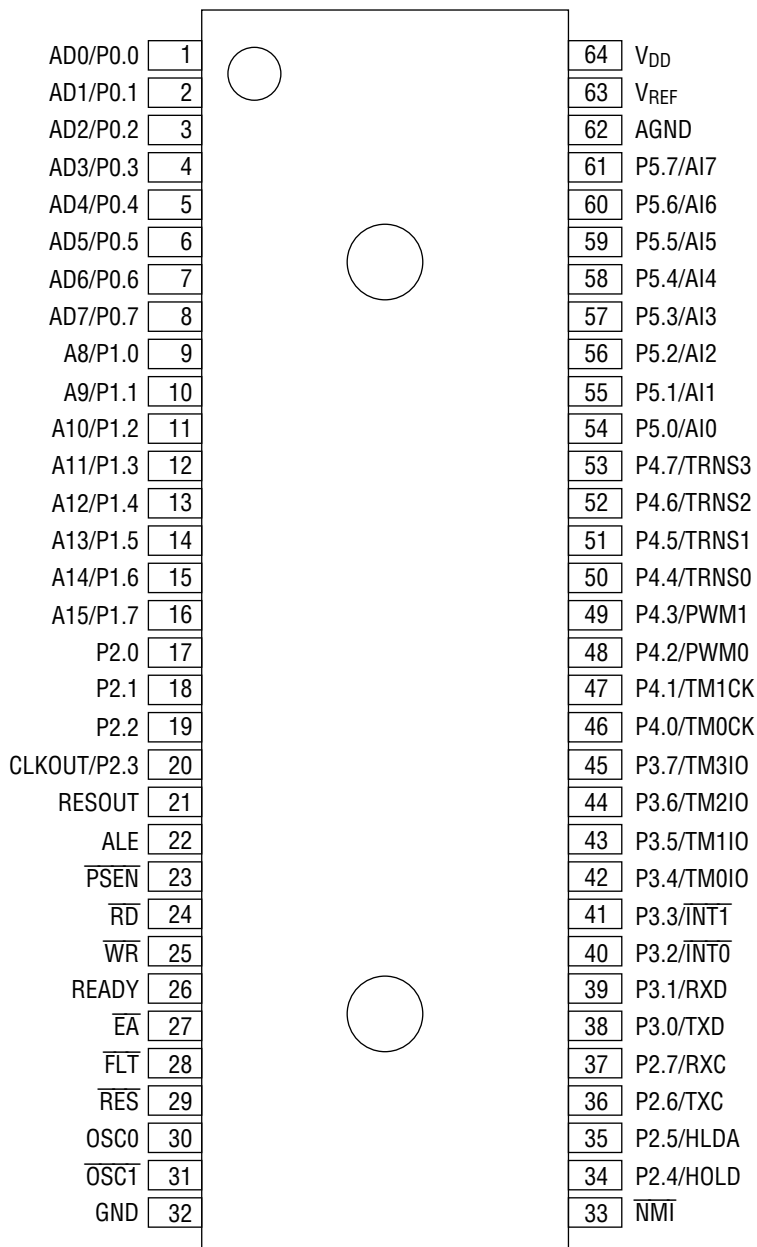
- 64-pin plastic shrink DIP (SDIP64-P-750-1.78) : (MSM66201-xxxSS) (MSM66P201-xxxSS)
(MSM66207-xxxSS) (MSM66P207-xxxSS)
- 64-pin plastic QFP (QFP64-P-1414-0.80-BK) : (MSM66201-xxxGSBK)(MSM66207xxxGS-
BK)
- 68-pin plastic QFJ (PLCC) (QFJ68-P-S950-1.27) : (MSM66201-xxxJS) (MSM66P201-xxxJS)
(MSM66207-xxxJS) (MSM66P207-xxxJS)
- 64-pin ceramic piggyback (ADIP64-C-750-1.78) : (MSM66G207VS)
(xxx indicates the code number.)

* The piggyback type is used only for engineering samples.

BLOCK DIAGRAM

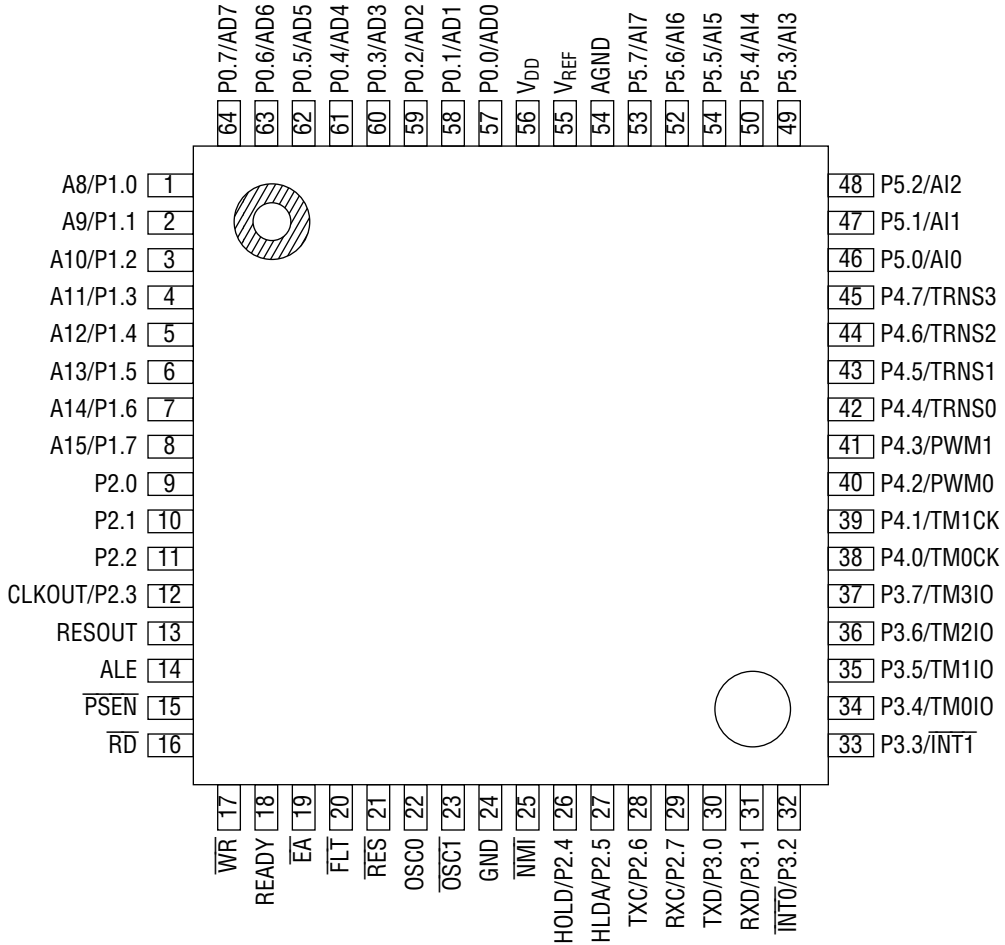


PIN CONFIGURATION (TOP VIEW)



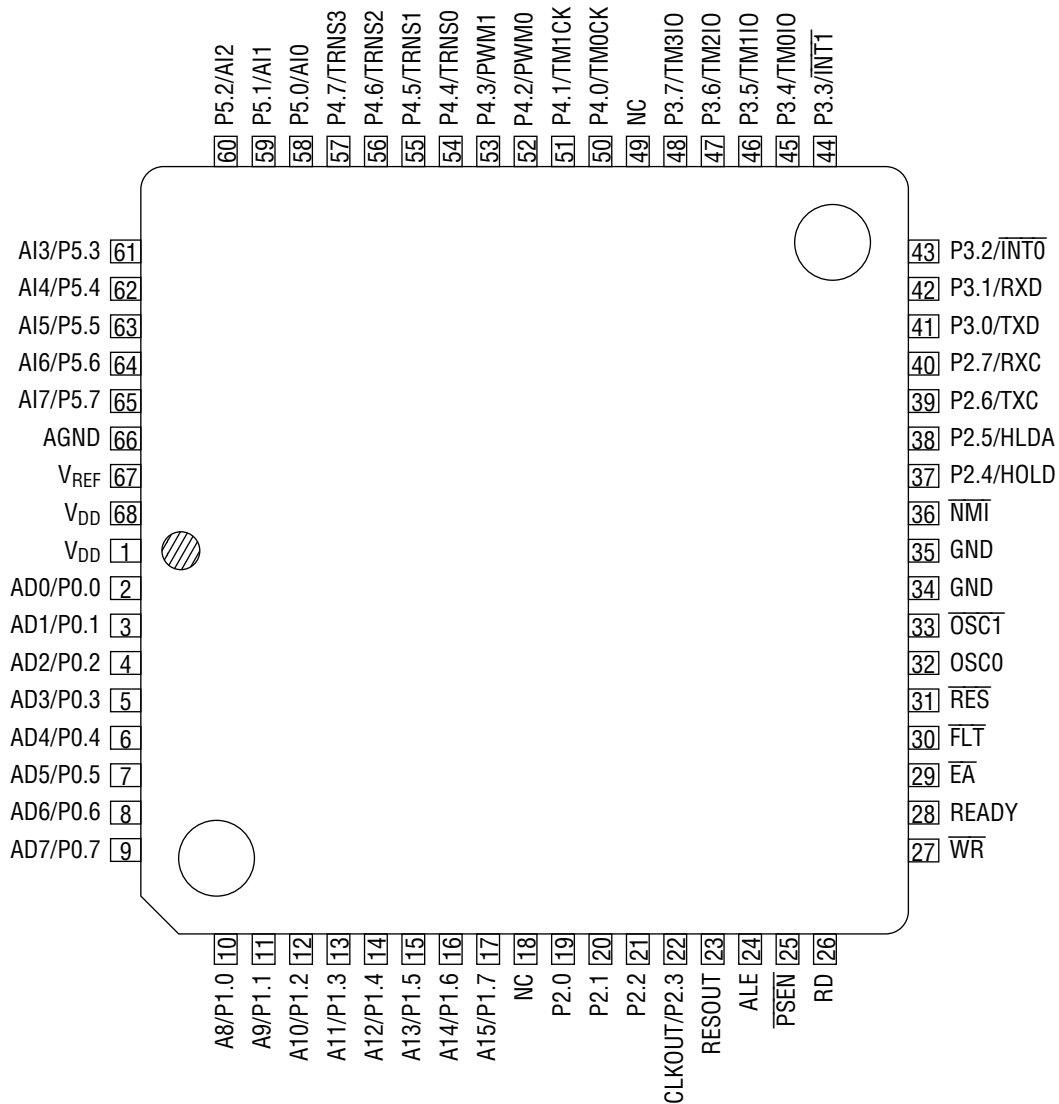
64-Pin Plastic Shrink DIP

PIN CONFIGURATION (TOP VIEW) (Continued)



64-Pin Plastic QFP

PIN CONFIGURATION (TOP VIEW) (Continued)



NC : No-connection pin

68-Pin Plastic QFJ (PLCC)

PIN DESCRIPTION

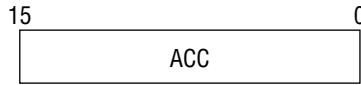
Symbol	Type	Description
P0.0–P0.7/ AD0–AD7	I/O	P0: 8-bit input-output port. Each bit can be assigned to input or output. AD: Outputs the lower 8 bits of program counter during external program memory fetch, and receives the addressed instruction under the control of PSEN. This pin also outputs the address and outputs or inputs data during an external data memory access instruction, under the control of ALE, RD, and WR.
P1.0–P1.7/ A8–A15	I/O	P1: 8-bit input-output port. Each bit can be assigned to input or output. A: Outputs the upper 8 bits of program counter (PC _{8–15}) during external program memory fetch. This pin also outputs the upper 8 bits of address during external data memory access instructions.
P2.0–P2.2 P2.3/CLKOUT P2.4/HOLD P2.5/HLDA P2.6/T _X C P2.7/R _X C	I/O	P2: 8-bit input-output port. Each bit can be assigned to input or output. CLKOUT: Output pin for supplying a clock to peripheral circuits. HOLD: Input pin to request the CPU to enter the hardware power-down state. HLDA: HOLD ACKNOWLEDGE: the HLDA signal appears in response to the HOLD signal and indicates that the CPU has entered the power-down state. T _X C: Transmitter clock input/output pin. R _X C: Receiver clock input/output pin.
P3.0/T _X D P3.1/R _X D P3.2/ $\overline{\text{INT0}}$ P3.3/ $\overline{\text{INT1}}$ P3.4/TM0IO P3.5/TM1IO P3.6/TM2IO P3.7/TM3IO	I/O	P3: 8-bit input-output port. Each bit can be assigned to input or output. T _X D: Transmitter data output pin. R _X D: Receiver data input pin. $\overline{\text{INT}}$: Interrupt request input pin. Falling edge trigger or level trigger is selectable. TM0IO-TM3IO: One of the following signals is output or input. <ul style="list-style-type: none"> • Clock at twice the frequency range of the 16-bit timer overflow • Load trigger signal to the capture register input • Setting value output Whether the signal is input or output depends on the mode.
P4.0/TMOCK P4.1/TM1CK P4.2/PWM0 P4.3/PWM1 P4.4 – P4.7/ TRANS0 – TRANS3	I/O	P4: 8-bit input-output port. Each bit can be assigned to input or output. TMOCK, TM1CK: Clock input pins of timer 0, timer 1. TRANS: Transition detector. The input pins which sense the falling edge and set the flag. PWM: 16-bit pulse-width modulator output pin.
P5.0 – P5.7/ AI0 –AI7	I	P5: 8-bit input port. AI: Analog signal input pin for A/D converter.

PIN DESCRIPTION (Continued)

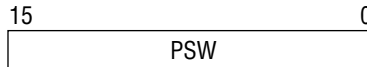
Symbol	Type	Description
RESOUT	0	Outputs "H" level in the case of internal reset. Reset to "L" level by program.
ALE	0	Address Latch Enable: The timing pulse to latch the lower 8 bits of the address output from port 0 when the CPU accesses the external memory.
PSEN	0	Program Strobe Enable: The strobe pulse to fetch to external program memory.
RD	0	Output strobe activated during a bus read cycle. Used to enable data onto the bus from the external data memory.
WR	0	Output strobe during a bus write cycle. Used as write strobe to external data memory.
READY	I	Used when the CPU accesses low-speed peripherals.
EA	I	Normally set to "H" level. If set to "L" level, the CPU fetches the code from external program memory.
FLT	I	If FLT is "H" level, ALE, WR, RD, PSEN are set to "H" level when reset. If FLT is set to "L", ALE, WR, RD, PSEN are set to floating level when reset.
RES	I	RESET input pin.
OSCO	I	Basic clock oscillation pin.
OSC1	0	Basic clock oscillation pin.
NMI	I	Non-maskable interrupt input pin (falling edge).
VREF	—	Reference voltage input pin for A/D converter.
AGND	—	Ground for A/D converter.
VDD	—	System power supply.
GND	—	Ground.

REGISTERS

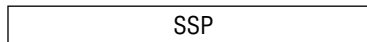
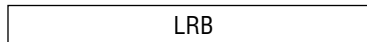
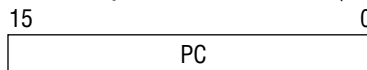
Accumulator



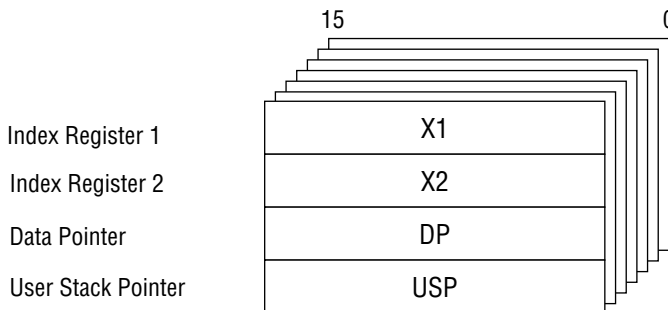
Control Register (CR)



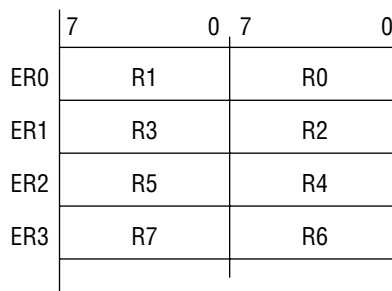
- Bit 15 : Carry flag (CY)
- Bit 14 : Zero flag (ZF)
- Bit 13 : Half carry flag (HC)
- Bit 12 : Data descriptor (DD)
- Bit 8 : Master interrupt priority flag (MIP)
- Bit 9,5,4: User flag (MIP)
- Bit 2-0 : System control base 2-0 (SCB2-0)



Pointing Register (PR)



Local Register



SFR

Address (HEX)	Name	Symbol	R/W	8/16-bit Operation	Reset				
0000	System stack pointer	SSP	R/W	8/16	FFH				
0001		(ASSP)			FFH				
0002	Local register base	LRB			R/W	8/16	undefined		
0003		(ALRB)					undefined		
0004☆	Program status word	PSWL (APSW)					R/W	8/16	C8H
0005☆		PSWH							0CH
0006	Accumulator	ACC							R/W
0007		ACC	00H						
0010☆	Standby control register	SBYCON	W	8					
0011	Watchdog timer	WDT			00H/WDT is stopped				
0012☆	Peripheral control register	PRPHF			R/W	FDH			
0013	Stop code acceptor	STPACP	W	8	"0"				
0018	Interrupt request register	IRQ	R/W	8/16	00H				
0019					00H				
001A	Interrupt enable register	IE			R/W	8/16	00H		
001B							00H		
001C☆	External interrupt control register	EXICON					R/W	8	FCH
0020	Port 0 data register	P0							undefined
0021	Port 0 mode register	P0IO							00H
0022	Port 1 data register	P1	undefined						
0023	Port 1 mode register	P1IO	00H						
0024	Port 2 data register	P2	undefined						
0025	Port 2 mode register	P2IO	00H						
0026☆	Port 2 secondary function control register	P2SF	07H						
0028	Port 3 data register	P3	undefined						
0029	Port 3 mode register	P3IO	00H						
002A	Port 3 secondary function control register	P3SF	00H						
002C	Port 4 data register	P4	undefined						
002D	Port 4 mode register	P4IO	00H						
002E	Port 4 secondary function control register	P4SF	00H						
002F	Port 5	P5	R	—					
0030	Timer 0 counter	TM0	R/W	16	00H				
0031					00H				
0032	Timer 0 register	TMR0			R/W	16	00H		
0033							00H		
0034	Timer 1 counter	TM1					R/W	16	00H
0035									00H
0036	Timer 1 register	TMR1							R/W
0037			00H						

Note: A ☆ mark in the address column indicates that there is a bit that does not exist in the register.
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SFR (Continued)

Address (HEX)	Name	Abbreviated Name	R/W	8/16-bit Operation	Reset	
0038	Timer 2 counter	TM2	R/W	16	00H	
0039					00H	
003A	Timer 2 register	TMR2			00H	
003B					00H	
003C	Timer 3 counter	TM3			00H	
003D					00H	
003E	Timer 3 register	TMR3			00H	
003F					00H	
0040	Timer 0 control register	TCON0		R/W	8	00H
0041	Timer 1 control register	TCON1				00H
0042	Timer 2 control register	TCON2				00H
0043	Timer 3 control register	TCON3				00H
0046☆	Transition detector register	TRANSIT				undefined
0048	Serial port transmission baud rate generator counter	STTM				00H
0049	Serial port transmission baud rate generator register	STTMR				00H
004A☆	Serial port transmission baud rate generator control register	STTMC				0CH
004C	Serial port receiving baud rate generator counter	SRTM	R/W	8	00H	
004D	Serial port receiving baud rate generator register	SRTMR			00H	
004E☆	Serial port receiving baud rate generator control register	SRTMC			0EH	
0050☆	Serial port transmission mode control register	STCON			80H	
0051	Serial port transmission data buffer register	STBUF			W	undefined
0054	Serial port receiving mode control register	SRCON			R/W	00H
0055	Serial port receiving data buffer register	SRBUF			R	undefined
0056☆	Serial port receiving error register	SRSTAT			R/W	FOH
0058☆	A/D scan mode register	ADSCAN	80H			
0059☆	A/D select mode register	ADSEL	A0H			
0060☆	A/D conversion result register 0	ADCRO	R	8/16	undefined	
0061						

Note: A ☆ mark in the address column indicates that there is a bit that does not exist in the register.

SFR (Continued)

Address (HEX)	Name	Abbreviated Name	R/W	8/16-bit operation	Reset
0062☆ 0063	A/D conversion result register 1	ADCR1	R	8/16	undefined
0064☆ 0065	A/D conversion result register 2	ADCR2			
0066☆ 0067	A/D conversion result register 3	ADCR3			
0068☆ 0069	A/D conversion result register 4	ADCR4			
006A☆ 006B	A/D conversion result register 5	ADCR5			
006C☆ 006D	A/D conversion result register 6	ADCR6			
006E☆ 006F	A/D conversion result register 7	ADCR7			
0070 0071	PWM 0 counter	PWMC0	R/W	8	00H
0072 0073	PWM 0 register	PWMR0			00H
0074 0075	PWM 1 counter	PWMC1			00H
0076 0077	PWM 1 register	PWMR1			00H
0078	PWM 0 control register	PWCON0			00H
007A	PWM 1 control register	PWCON1			00H

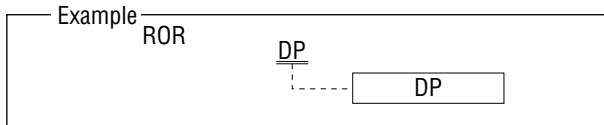
Note: A ☆ mark in the address column indicates that there is a bit that does not exist in the register.

ADDRESSING MODES

The MSM66201/66207 provides independent 64K-byte data and 64K-byte program space with various types of addressing modes. These modes are shown below, for both RAM (for data space) and ROM (for program space).

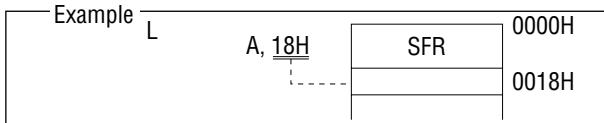
1. RAM Addressing Modes (for data space)

1.1 Register Direct Addressing

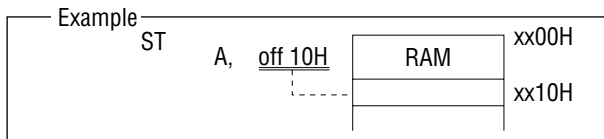


1.2 Displacement Addressing

a) Zero Page

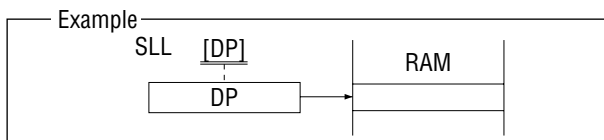


b) Direct Page

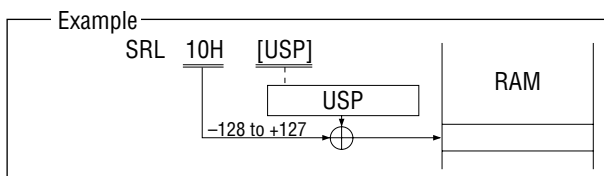


1.3 Pointing Register (PR) Indirect Addressing

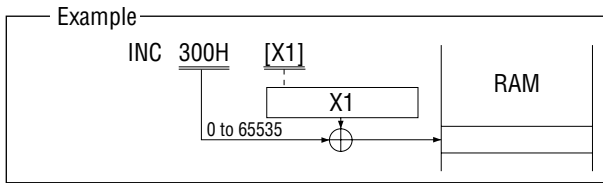
a) Data Point (DP) Indirect



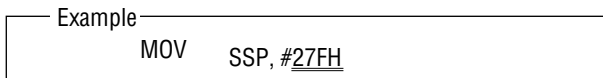
b) User Stack Pointer (USP) Indirect



c) Index Register (X1, X2) Indirect

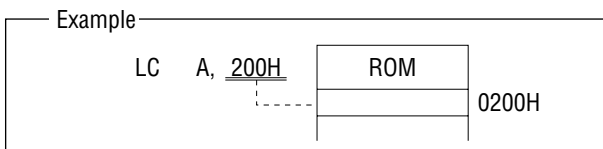


1.4 Immediate Addressing



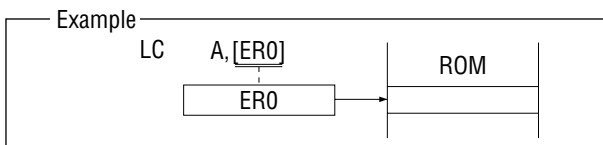
2. ROM Addressing Modes (for program space)

2.1 Direct Addressing



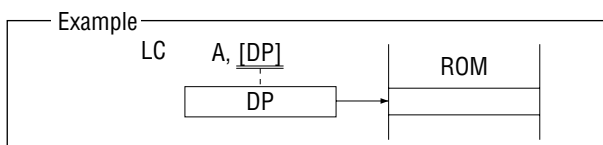
2.2 Simple Indirect Addressing

a) Local Register Indirect

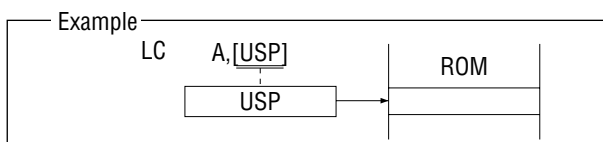


b) Pointing Register Indirect

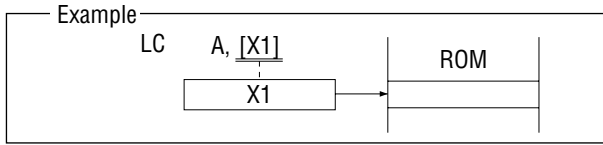
1) Data Pointer (DP) Indirect



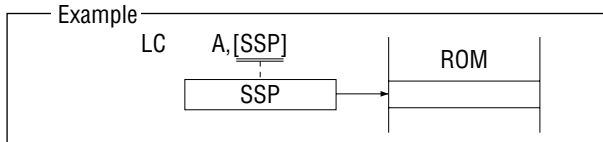
2) User Stack Pointer (USP) Indirect



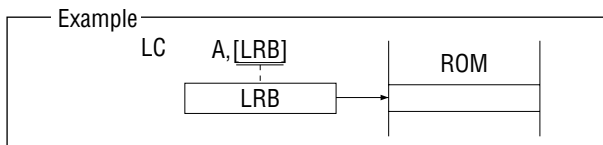
3) Index Register (X1, X2) Indirect



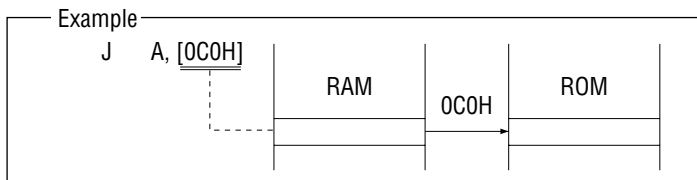
c) System Stack Pointer (SSP) Indirect



d) Local Register Base (LRB) Indirect

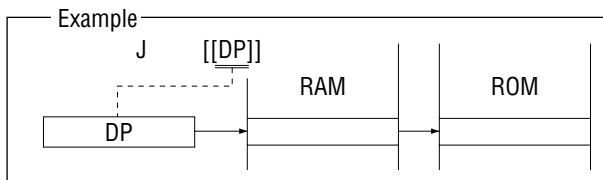


e) RAM Indirect

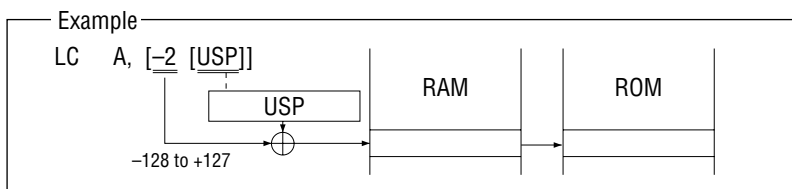


2.3 Double Indirect Addressing

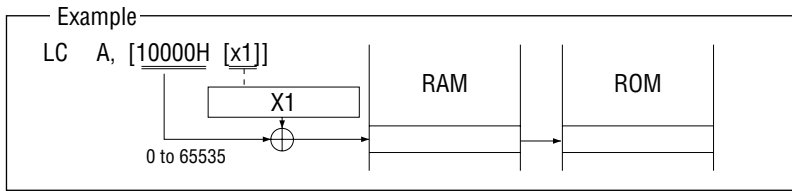
a) Data Pointer (DP) Double Indirect



b) User Stack Pointer (USP) Double Indirect



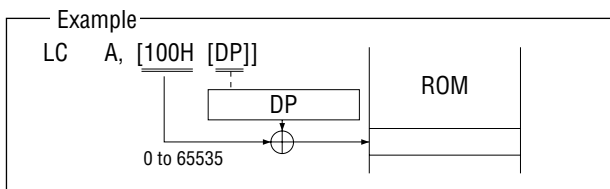
c) Index Register (X1, X2) Double Indirect



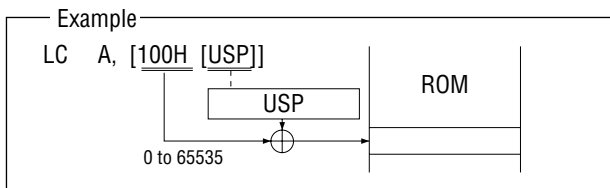
2.4 Indirect Addressing with 16-bit Offset

a) Pointing Register Indirect

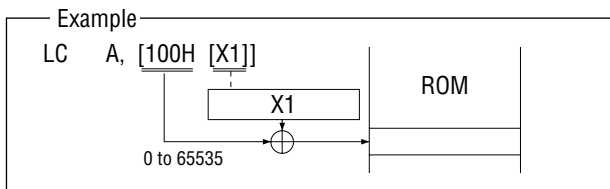
1) Data Pointer (DP) Indirect



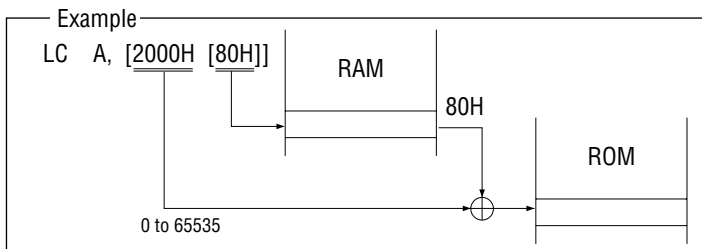
2) User Stack Pointer (USP) Indirect



3) Index Register (X1, X2) Indirect

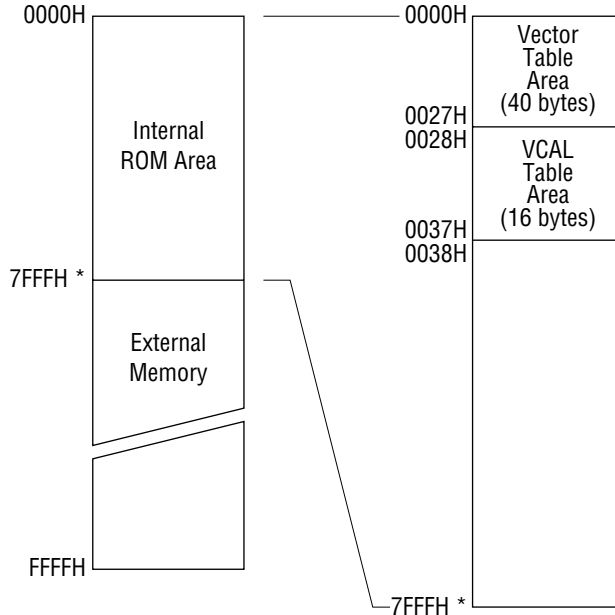


b) RAM Indirect



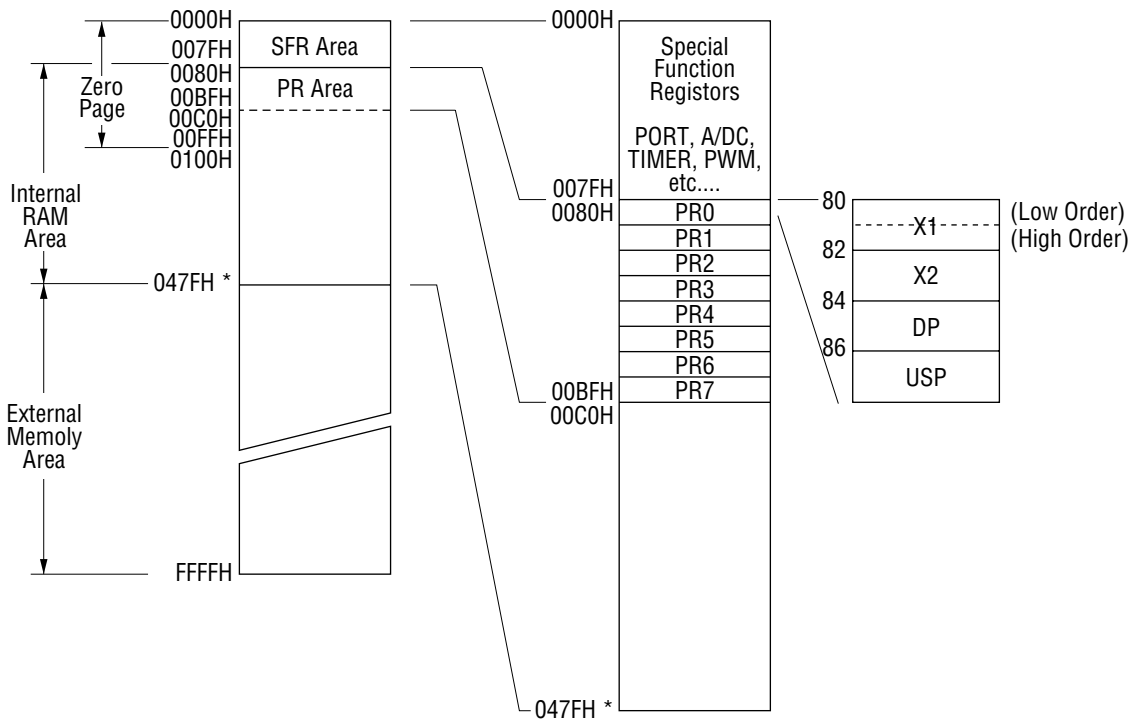
MEMORY MAPS

Program Memory Space



* MSM66201 : 3FFFH

Data Memory Space



ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

Parameter	Symbol	Condition		Rating	Unit
Supply Voltage	V _{DD}	GND=AGND=0V		-0.3 to 7.0	V
Input Voltage	V _I			-0.3 to V _{DD} +0.3	
Output Voltage	V _O			-0.3 to V _{DD} +0.3	
Analog Ref. Voltage	V _{REF}			-0.3 to V _{DD} +0.3	
Analog Input Voltage	V _{AI}			-0.3 to V _{REF}	
Power Dissipation	P _D	Ta=85°C per Package	64-pin shrink DIP	930	mW
			64-pin QFP	565	
			68-pin QFJ	1120	
Storage Temperature	T _{STG}	—		-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit	
Supply Voltage	V _{DD}	f _{OSC} ≤ 10MHz	4.5 to 5.5	V	
Memory Hold Voltage	V _{DDH}	f _{OSC} = 0Hz	2.0 to 5.5		
Operating Frequency	f _{OSC}	V _{DD} = 5V ±10%	0 to 10	MHz	
Ambient Temperature	T _a	—	-40 to +85	°C	
Fan Out	N	MOS load		20	—
		TTL load	P0	2	
			P1, P2, P3, P4	1	

ELECTRICAL CHARACTERISTICS

DC Characteristics

 $(V_{DD} = 5V \pm 10\%, T_a = -40 \text{ to } +85^\circ\text{C})$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage 1, 3, 6	V_{IH}	—	2.4	—	$V_{DD}+0.3$	V
"H" Input Voltage 5, 7			4.0	—	$V_{DD}+0.3$	
"H" Input Voltage 8			4.2	—	$V_{DD}+0.3$	
"H" Input Voltage 2			3.6	—	$V_{DD}+0.3$	
"L" Input Voltage 1, 2, 3, 6	V_{IL}	—	-0.3	—	0.8	V
"L" Input Voltage 5, 7			-0.3	—	0.8	
"L" Input Voltage 8			-0.3	—	0.4	
"H" Output Voltage 1, 4	V_{OH}	$I_O = -400\mu\text{A}$	4.2	—	—	V
"H" Output Voltage 2		$I_O = -200\mu\text{A}$	4.2	—	—	
"L" Output Voltage 1, 4	V_{OL}	$I_O = 3.2\text{mA}$	—	—	0.4	V
"L" Output Voltage 2		$I_O = 1.6\text{mA}$	—	—	0.4	
Input Leakage Current 3, 6, 7	I_{IH}/I_{IL}	$V_I = V_{DD}/0V$	—	—	1/-1	μA
Input Current 5			—	—	1/-20	
Input Current 8			—	—	10/-10	
"H" Output Current 1	I_{OH}	$V_O = 2.4V$	-2	—	—	mA
"H" Output Current 2			-1	—	—	
"L" Output Current 1	I_{OL}		10	—	—	
"L" Output Current 2			5	—	—	
Output Leakage Current 1, 2, 4	I_{LO}	$V_O = V_{DD}/0V$	—	—	± 2	μA
Input Capacitance	C_I	$f = 1\text{MHz}$ $T_a = 25^\circ\text{C}$	—	5	—	pF
Output Capacitance	C_O		—	7	—	
Analog Reference Power Supply Current	I_{REF}	A/D in operation	—	0.3	2	mA
		A/D stopped	—	0.5	10	μA
Current Consumption (during STOP) *	I_{DDS}	$V_{DD} = 2V$	—	0.2	10	μA
		—	—	1	100	
Current Consumption (during HALT)	I_{DDH}	$f_{OSC} = 10\text{MHz}$ No Load	—	6	10	mA
			**—	8	15	
Current Consumption	I_{DD}		—	20	35	
			**—	30	40	

- Note: 1 Applied to P0
2 Applied to P1, P2, P3 and P4
3 Applied to P5
4 Applied to ALE, $\overline{\text{PSEN}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$ and RESOUT
5 Applied to RES and $\overline{\text{NMI}}$
6 Applied to READY and $\overline{\text{EA}}$
7 Applied to FLT
8 Applied to OSC_0

* V_{DD} or GND for ports serving as the input pin. No load for any other.

** Applied to MSM66P201/66P207

AC Characteristics

• External program memory control

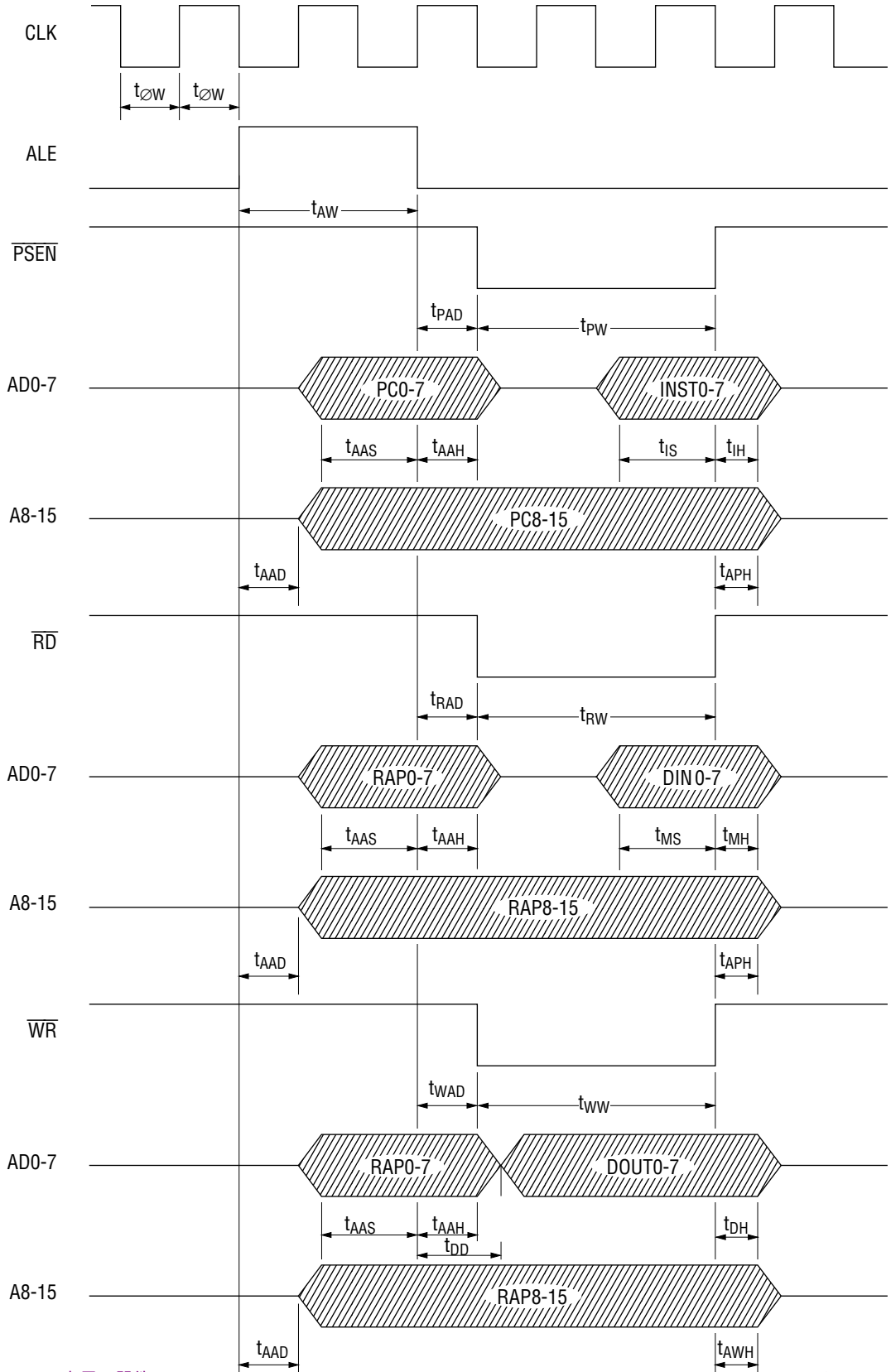
 $(V_{DD}=5V\pm 10\%, T_a=-40 \text{ to } +85^\circ\text{C})$

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock (OSC) Pulse	$t_{\phi W}$	—	50	—	ns
ALE Pulse Width	t_{AW}	$C_L = 50\text{pF}$	$3t_{\phi W}-20$	—	
$\overline{\text{PSEN}}$ Pulse Width	t_{PW}		$4t_{\phi W}-20$	—	
$\overline{\text{PSEN}}$ Pulse Delay Time	t_{PAD}		$t_{\phi W}-20$	$t_{\phi W}+20$	
Low Address Setup time	t_{AAS}		$2t_{\phi W}-35$	$2t_{\phi W}+20$	
Low Address Hold Time	t_{AAH}		$t_{\phi W}-20$	$t_{\phi W}+40$	
High Address Delay Time	t_{AAD}		$t_{\phi W}-20$	$t_{\phi W}+40$	
High Address Hold Time	t_{APH}		$t_{\phi W}-20$	$t_{\phi W}+40$	
Instruction Setup Time	t_{IS}		100	—	
Instruction Hold Time	t_{IH}		0	$t_{\phi W}-20$	

• External data memory control

 $(V_{DD}=5V\pm 10\%, T_a=-40 \text{ to } +85^\circ\text{C})$

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock (OSC) Pulse	$t_{\phi W}$	—	50	—	ns
ALE Pulse Width	t_{AW}	$C_L = 50\text{pF}$	$3t_{\phi W}-20$	—	
$\overline{\text{RD}}$ Pulse Width	t_{RW}		$4t_{\phi W}-20$	—	
$\overline{\text{WR}}$ Pulse Width	t_{WW}		$4t_{\phi W}-20$	—	
$\overline{\text{RD}}$ Pulse Delay Time	t_{RAD}		$t_{\phi W}-20$	$t_{\phi W}+20$	
$\overline{\text{WR}}$ Pulse Delay Time	t_{WAD}		$t_{\phi W}-20$	$t_{\phi W}+20$	
Low Address Setup Time	t_{AAS}		$2t_{\phi W}-35$	$2t_{\phi W}+20$	
Low Address Hold Time	t_{AAH}		$t_{\phi W}-20$	$t_{\phi W}+40$	
High Address Setup Time	t_{AAD}		$t_{\phi W}-20$	$t_{\phi W}+40$	
High Address Hold Time	t_{ARH}		$t_{\phi W}-20$	$t_{\phi W}+40$	
High Address Hold Time	t_{AWH}		$t_{\phi W}-20$	$t_{\phi W}+40$	
Memory Data Setup Time	t_{MS}		100	—	
Memory Data Hold Time	t_{MH}		0	$t_{\phi W}-20$	
Data Delay Time	t_{DD}		$t_{\phi W}-20$	$t_{\phi W}+40$	
Data Hold Time	t_{DH}		$t_{\phi W}-20$	$t_{\phi W}+40$	



- Serial port control

Master mode

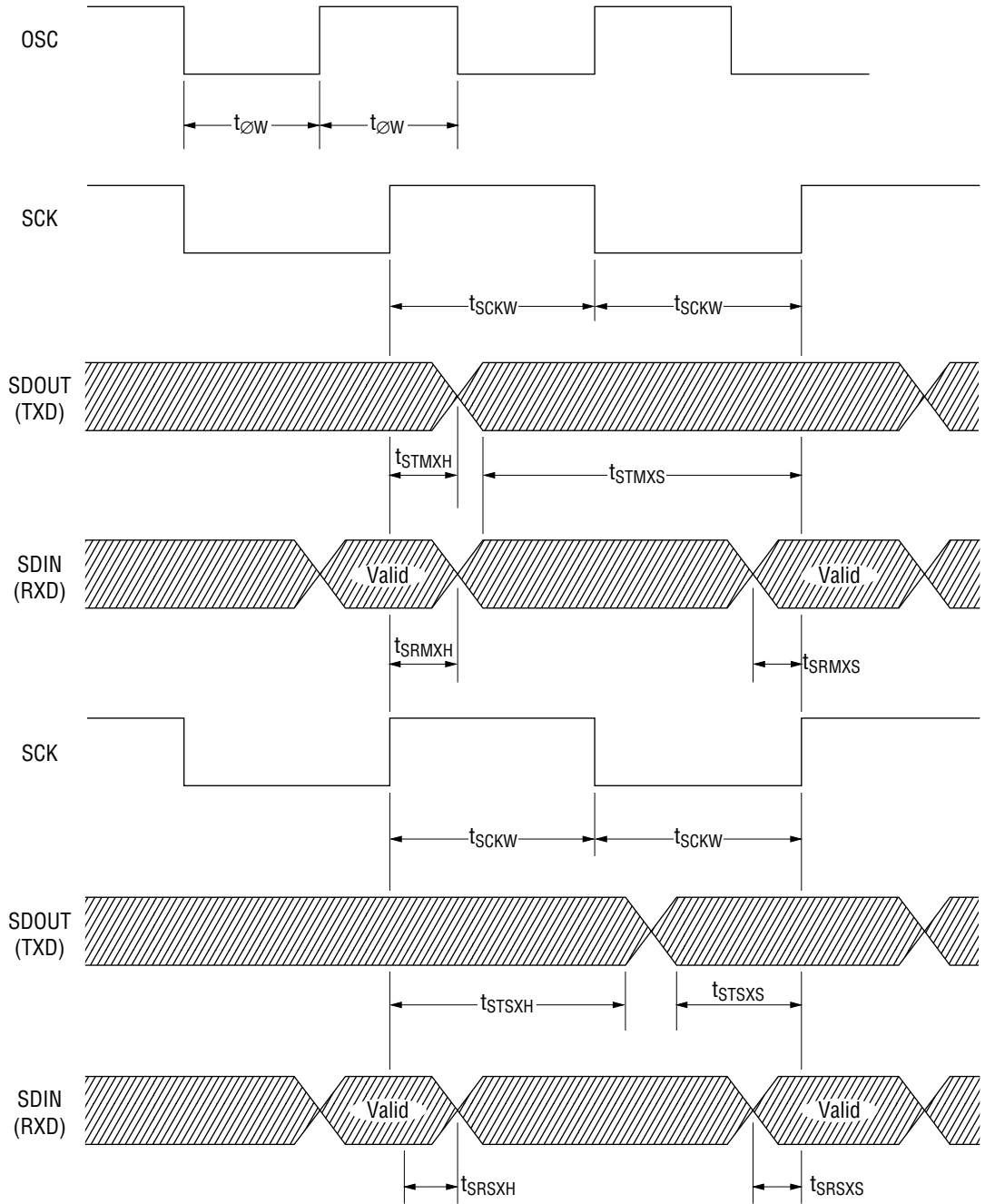
(V_{DD}=5V±10%, Ta=-40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock (OSC) Pulse Width	t _{φW}	—	50	—	ns
Serial Clock Pulse Width	t _{SCKW}	—	8t _{φW}	—	
Output Data Setup Time	t _{STMXS}	C _L =50pF	8t _{φW} +40	—	
Output Data Hold Time	t _{STMXH}		6t _{φW} -20	—	
Input Data Setup Time	t _{SRMXS}		2t _{φW} +10	—	
Input Data Hold Time	t _{SRMXH}		50	—	

Slave mode

(V_{DD}=5V±10%, Ta=-40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock (OSC) Pulse Width	t _{φW}	—	50	—	ns
Serial Clock Pulse Width	t _{SCKW}	—	8t _{φW}	—	
Output Data Setup Time	t _{STSXS}	C _L =50pF	6t _{φW} +40	—	
Output Data Hold Time	t _{STSXH}		6t _{φW} -20	—	
Input Data Setup Time	t _{SRSXS}		100	—	
Input Data Hold Time	t _{SRSXH}		100	—	



A/D Converter Characteristics

• Operating range

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	$f_{OSC} \leq 10\text{MHz}$	4.5	—	5.5	V
Analog Reference Voltage	V_R	$V_{AG} = \text{GND} = 0\text{V}$	4.5	—	V_{DD}	
Analog Input Voltage	V_{AI}		V_{AG}	—	V_R	
Analog Reference Power Voltage Resistance	R_R		—	16	—	k Ω
Operating Temperature	T_{op}	$V_{DD} = 5\text{V} \pm 10\%$	-40	—	+85	$^{\circ}\text{C}$

• A/D Converter accuracy

Normal operation mode

 $(V_{DD}=5\text{V} \pm 10\%, f_{OSC}=10\text{MHz}, T_a=-40 \text{ to } +85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min.		Typ.		Max.		Unit
				*		*		*	
Resolution	n	See the recommended circuit. $V_R = V_{DD}$ $V_{AG} = \text{GND} = 0\text{V}$ Analog input source impedance $\leq 5\text{k}\Omega$ One channel conversion time $t_c = 64\mu\text{s}$	—	—	—	—	10	10	Bit
Absolute Error	E_A		—	—	—	—	+3.0 -3.5	+2.0 -3.5	LSB
Relative Error	E_R		—	—	—	—	± 1.5	± 1.0	
Zero Point Error	E_Z		0	0	—	—	+3.0	+2.0	
Full Scale Error	E_F		-0.5	-1.0	—	—	-3.5	-3.5	
Differential Linearity Error	E_D		—	—	—	—	+3.0	+2.0	
Crosstalk	E_C	—	—	± 0.5	± 0.5	—	—		

* $V_{DD}=5\text{V}, T_a=25^{\circ}\text{C}$

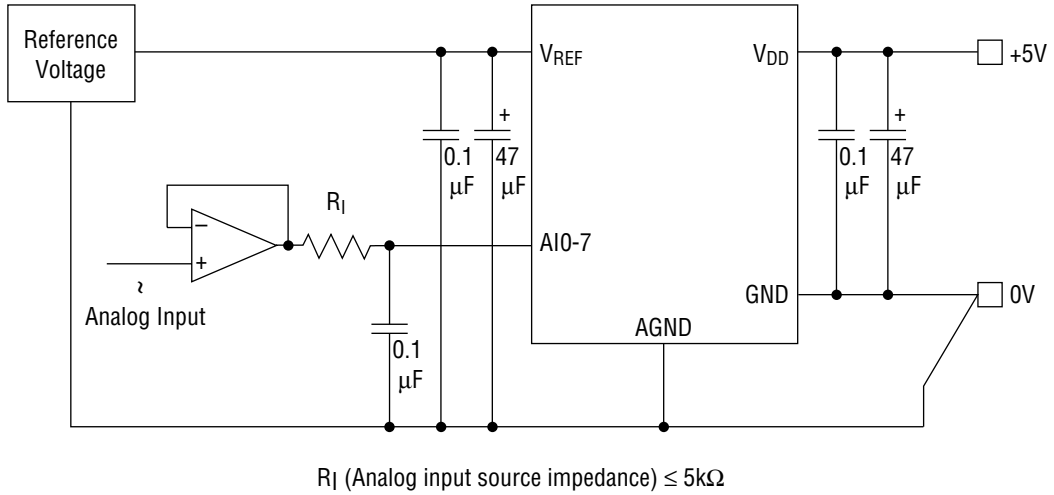
HALT/HOLD operation mode

 $(V_{DD}=5\text{V} \pm 10\%, f_{OSC}=10\text{MHz}, T_a=-40 \text{ to } +85^{\circ}\text{C})$

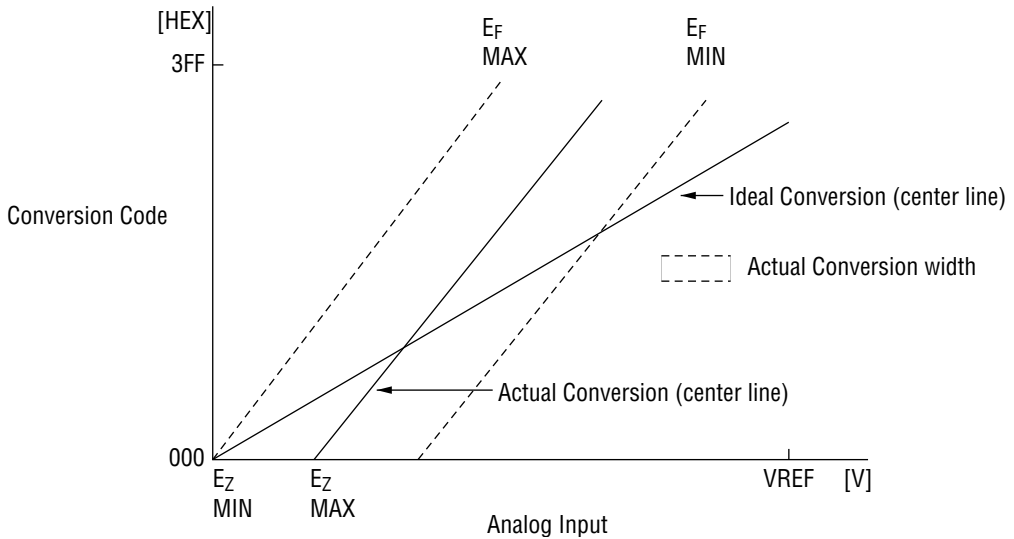
Parameter	Symbol	Condition	Min.		Typ.		Max.		Unit
				*		*		*	
Resolution	n	See the recommended circuit. $V_R = V_{DD}$ $V_{AG} = \text{GND} = 0\text{V}$ Analog input source impedance $\leq 5\text{k}\Omega$ One channel conversion time $t_c = 64\mu\text{s}$	—	—	—	—	10	10	Bit
Absolute Error	E_A		—	—	—	—	+2.0 -3.5	+1.0 -2.0	LSB
Relative Error	E_R		—	—	—	—	± 1.0	± 0.5	
Zero Point Error	E_Z		+0.5	+0.5	—	—	+2.0	+1.0	
Full Scale Error	E_F		-1.0	-1.5	—	—	-3.5	-2.0	
Differential Linearity Error	E_D		—	—	—	—	+2.0	+1.0	
Crosstalk	E_C	—	—	± 0.5	± 0.5	—	—		

* $V_{DD}=5\text{V}, T_a=25^{\circ}\text{C}$

• **Recommended circuit**



• **A/D Converter conversion characteristics 1**



Conversion Characteristics Diagram 1

Absolute error (E_A)

The absolute error indicates a difference between actual conversion and ideal conversion, excluding a quantizing error. The absolute error of the A/D converter gets larger as it approaches the zero point or full scale. (Refer to Conversion Characteristics Diagram 1.)

Relative error (E_R)

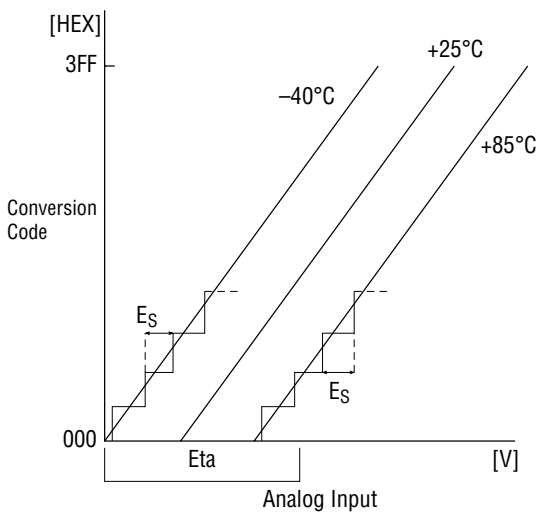
The relative error indicates a deviation from a line which connects the center point of the zero point conversion width with that of the full scale conversion width, excluding a quantizing error.

The relative error of this A/D converter is almost due to a differential linearity error.

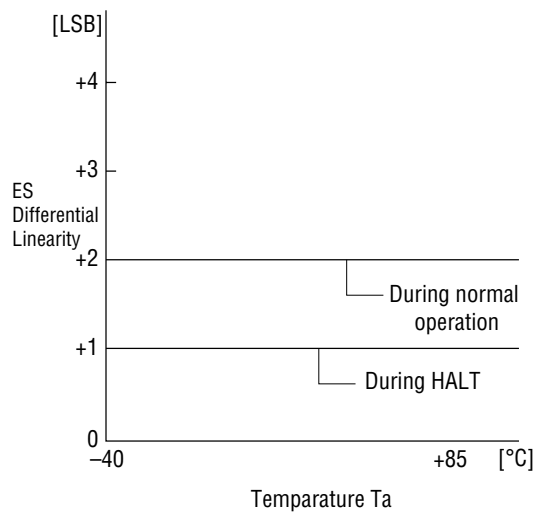
Zero point error (E_z) and full scale error (E_F)

The zero point error and full scale error indicate a difference between actual conversion and ideal conversion at the zero point and full scale, respectively. (Refer to Conversion Characteristics Diagram 1.)

A/D Converter Conversion Characteristics 2 (temperature characteristics)



Conversion Characteristics Diagram 2-1



Conversion Characteristics Diagram 2-2

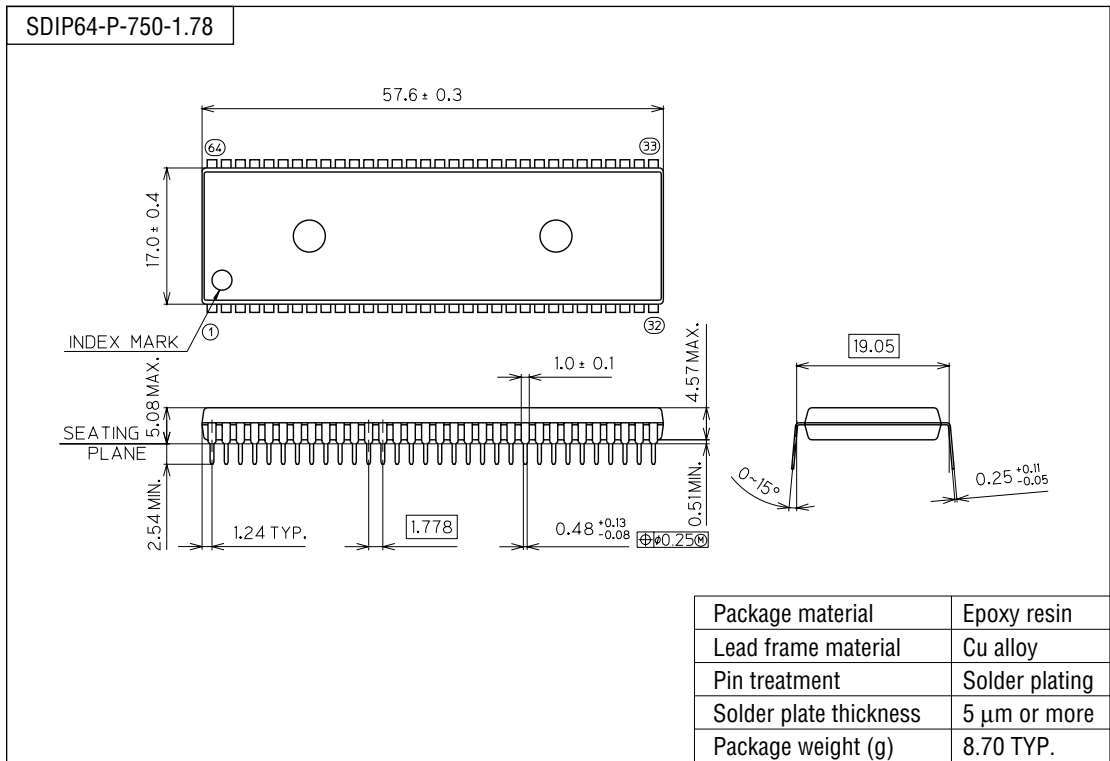
Differential linearity error (E_D)

The differential linearity error indicates a difference between the actual conversion width (actual step width) and ideal value (1LSB).

With this A/D converter, a voltage for actual conversion is shifted and the inclination of a voltage is changed, with changes of temperature (see Conversion Characteristics Diagram 2-1). Specifications described in the foregoing tables are established from Eta shown in Conversion Characteristics Diagram 2-1 ($E_D = \text{Eta} - 1\text{LSB}$). Conversion Characteristics Diagram 2-2 shows temperature characteristics of differential linearity of Es in Conversion Characteristics Diagram 2-1.

PACKAGE DIMENSIONS

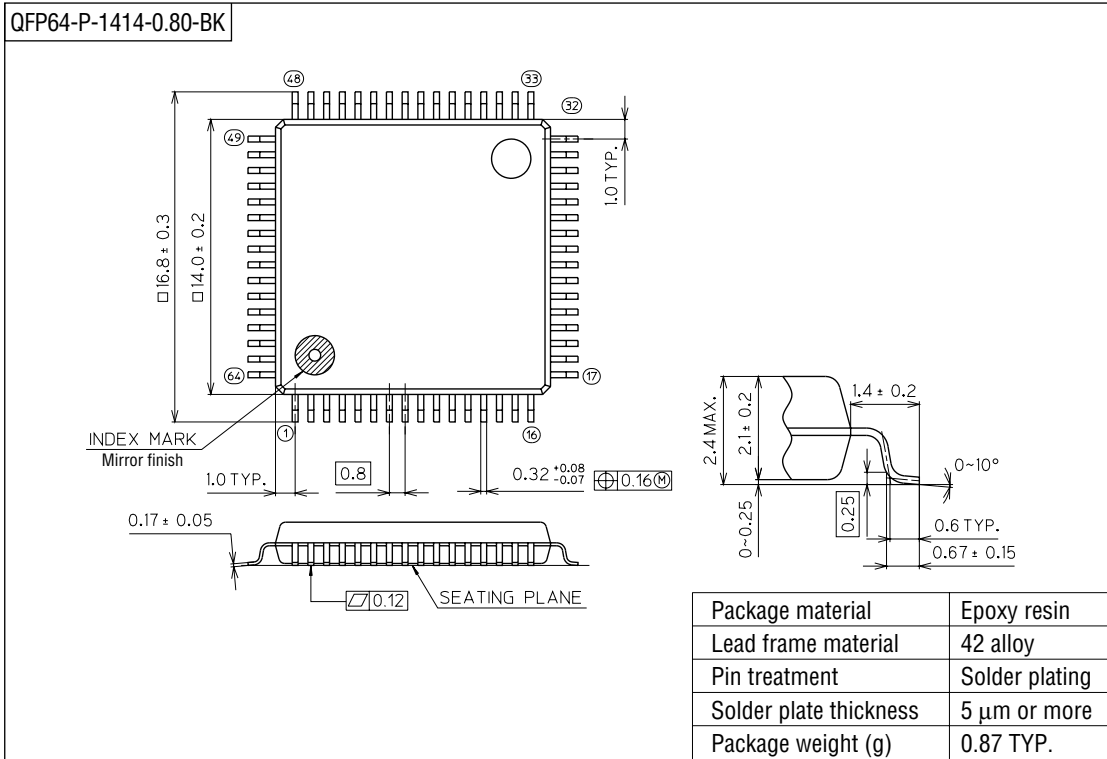
(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

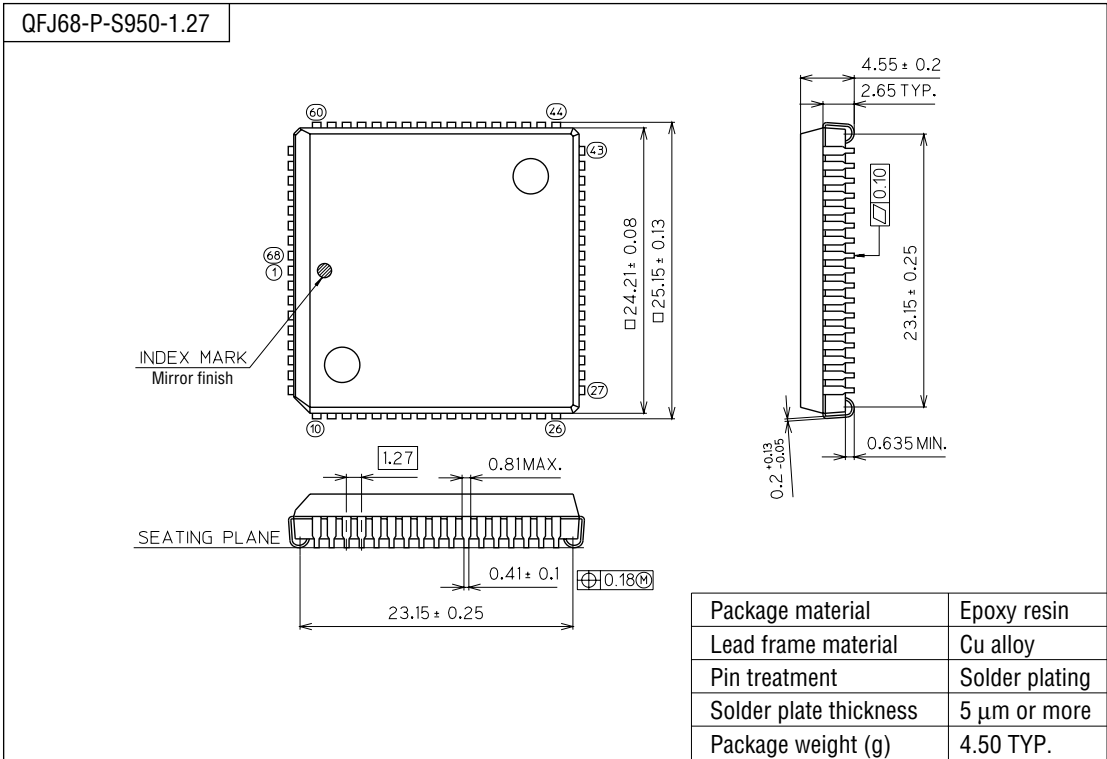
(Unit : mm)



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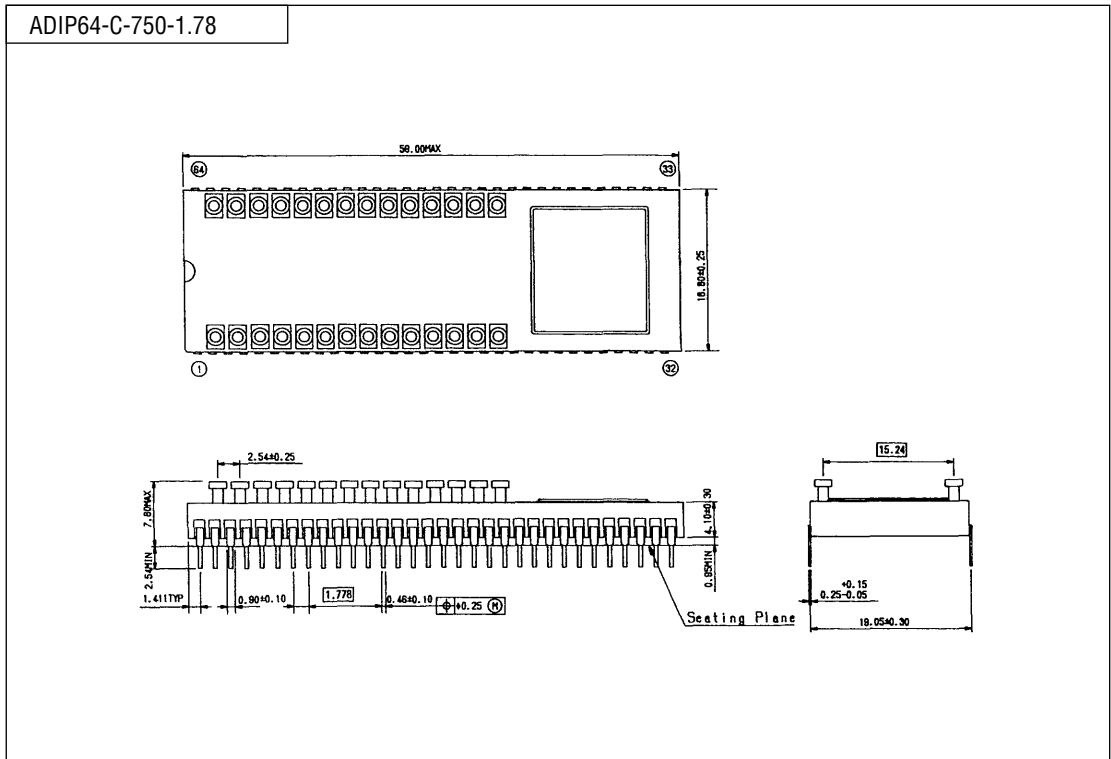
(Unit : mm)



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(Unit : mm)



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