

MSM5267B-15

33-BIT VFD SEGMENT DRIVER

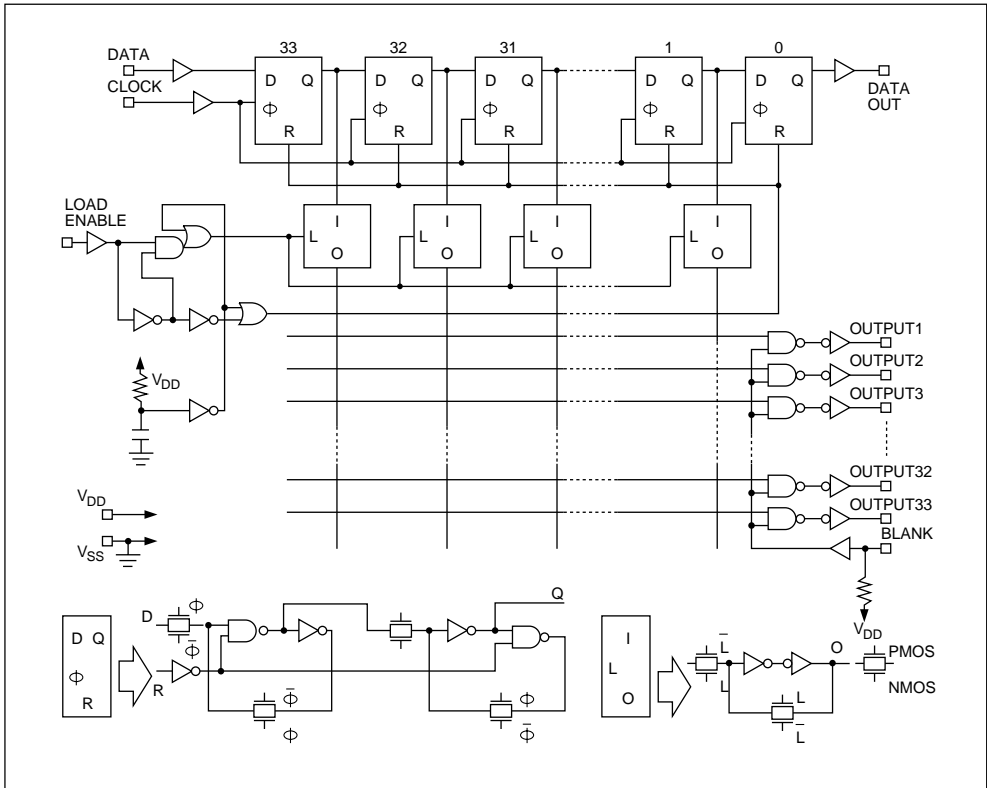
GENERAL DESCRIPTION

The MSM5267B-15 is a CMOS multi-digit display driver and consisting of a 34-bit shift register, a 33-bit latch, and a 33-bit VF tube driver.

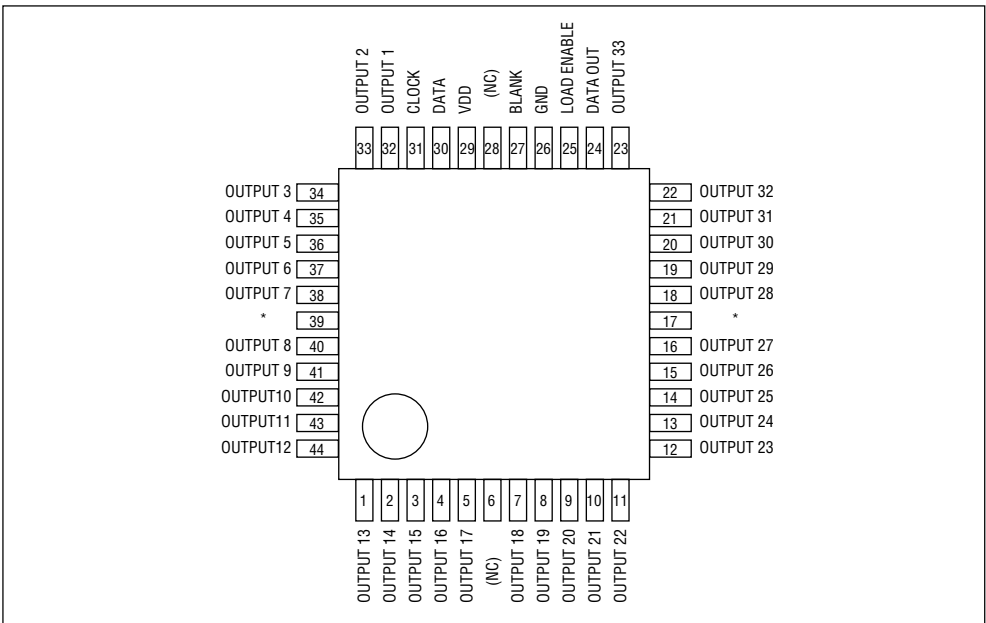
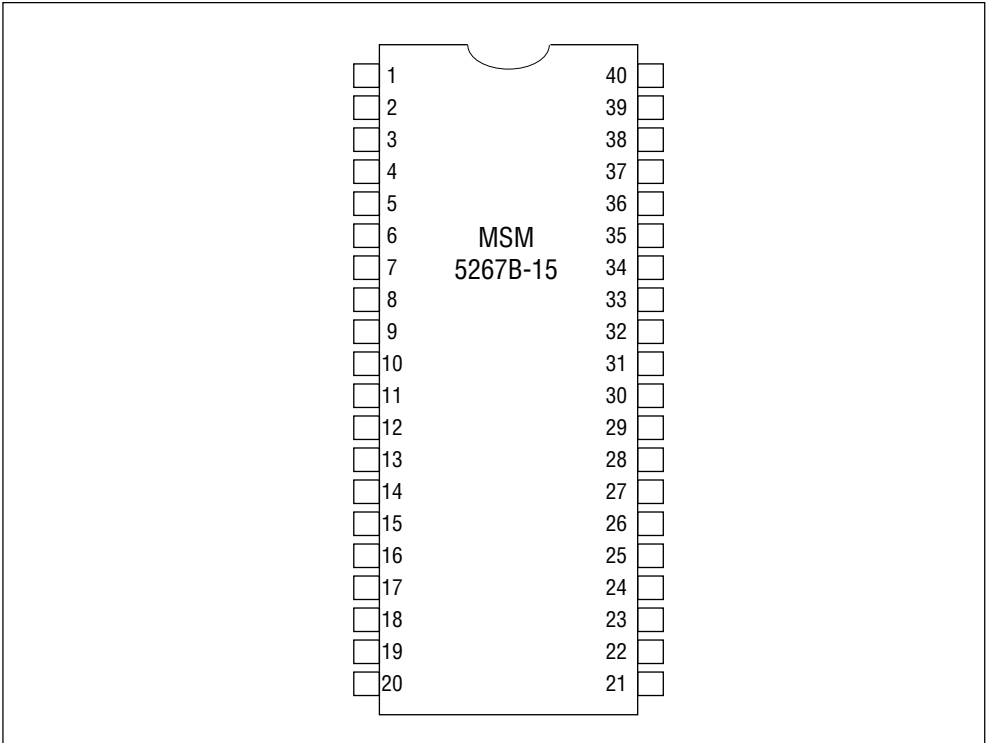
FEATURES

- Complete static operation to ensure stability against noise.
- 3 or 4-signal line connection with microcomputers.
- Direct driver of VF tubes (8 outputs of high-current drive, 25 outputs of low-current drive)
- Capability of self-load mode.
- Low power consumption.
- Signal power supply and operating voltage range of 8V to 18V.
- 40-pin Plastic DIP (DIP40-P-600)
- 44-pin "V" Plastic QFP (QFP44-P-910-VK)
- 44-pin Plastic QFJ (PLCC) (QFJ44-P-S650)

BLOCK DIAGRAM



PIN CONFIGURATION



Note) Pin 17 and Pin 39 are internally connected to VDD. Therefore, those pins can not be connected to any other pin than VDD.

PIN DISCRIPTION

PIN No.	Pin Name	Comments
1	VDD	Input Positive Supply Voltage Terminal
2	Data	Input Data Acquisition Terminal
3	Clock	Input Clock Terminal
4	Output 1	Output Shift Register 32
5	Output 2	Output Shift Register 21
6	Output 3	Output Shift Register 22
7	Output 4	Output Shift Register 23
8	Output 5	Output Shift Register 30
9	Output 6	Output Shift Register 13
10	Output 7	Output Shift Register 14
11	Output 8	Output Shift Register 15
12	Output 9	Output Shift Register 1
13	Output 10	Output Shift Register 33
14	Output 11	Output Shift Register 5
15	Output 12	Output Shift Register 6
16	Output 13	Output Shift Register 7
17	Output 14	Output Shift Register 28
18	Output 15	Output Shift Register 27
19	Output 16	Output Shift Register 31
20	Output 17	Output Shift Register 18
21	Output 18	Output Shift Register 2
22	Output 19	Output Shift Register 10
23	Output 20	Output Shift Register 26
24	Output 21	Output Shift Register 29
25	Output 22	Output Shift Register 3
26	Output 23	Output Shift Register 8
27	Output 24	Output Shift Register 9
28	Output 25	Output Shift Register 4
29	Output 26	Output Shift Register 11
30	Output 27	Output Shift Register 16
31	Output 28	Output Shift Register 17
32	Output 29	Output Shift Register 12
33	Output 30	Output Shift Register 19
34	Output 31	Output Shift Register 24
35	Output 32	Output Shift Register 25
36	Output 33	Output Shift Register 20
37	Data Out	Output Data Shift Register
38	Load Enable	Input for Loading Word into Data Latch from Data Shift Register
39	Vss	Ground Potential Terminal
40	Blank	Input for Turning Output Drivers off

ELECTRICAL CHARACTERISTICS

- Absolute Maximum Ratings

Ta=25°C, Unless otherwise specified

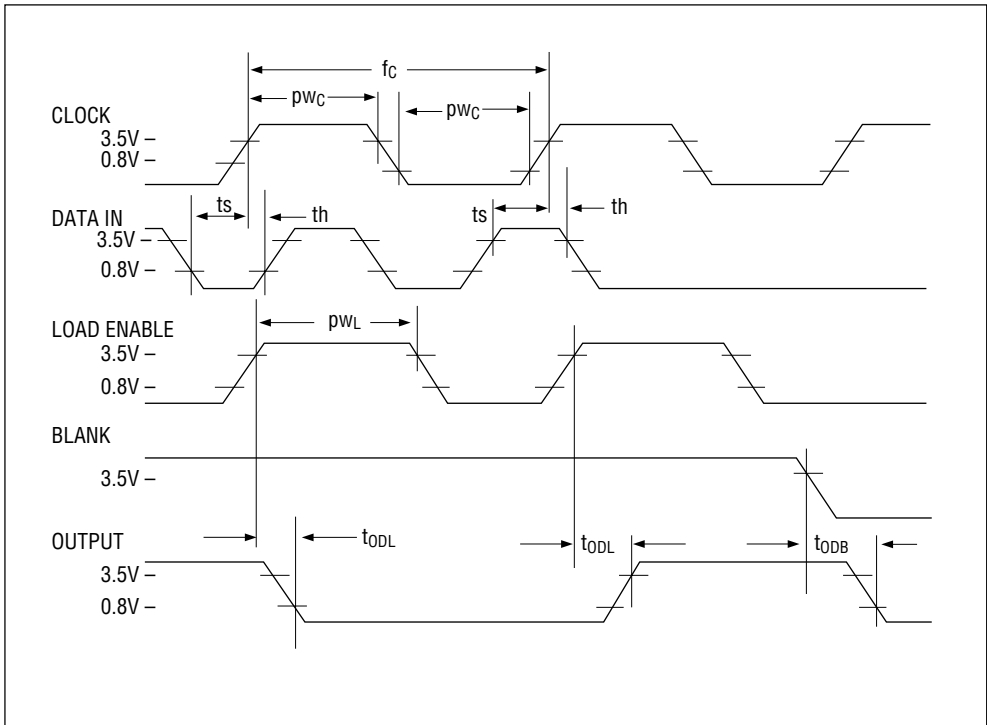
Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	V _{DD}	–	–0.3	20	V
Input voltage	V _I	–	–0.3	V _{DD} + 0.3	V
Operating Temperature	T _a	–	–40	85	°C
Storage Temperature	T _{st}	–	–65	150	°C

AC CHARACTERISTICS

Ta=–40°C to +85°C, VDD=8V to 18V Unless otherwise specified

Characteristics	Symbol	Condition	MIN	MAX	Units
Clock Frequency	F _c	–	–	160	kHz
Clock Pulse Width	PW _c	Either positive or negative	2.5	–	μS
Slew Rate Outputs; (1-33)	t _r	C _L =100pF, t=20% to 80% or 80% to 20% of V _{DD} V _{DD} =8V or V _{DD} =18V	–	5	μS
Data Setup Time	t _s	–	1	–	μS
Data Hold Time	t _H	–	200	–	nS
Output Delay from Blank	t _{ODB}	C _L =100pF V _{DD} =8V	–	7	μS
Output Delay from Load	t _{ODL}	C _L =100pF V _{DD} =8V	–	8	μS
Power on Reset Slew Rate	PRSR	–	0.001	10	V/μS
Load Pulse Width	PW _L	–	1.6	–	μS

• Timing Chart



DC CHARACTERISTICS

Ta= -40 to 85°C Unless otherwise specified

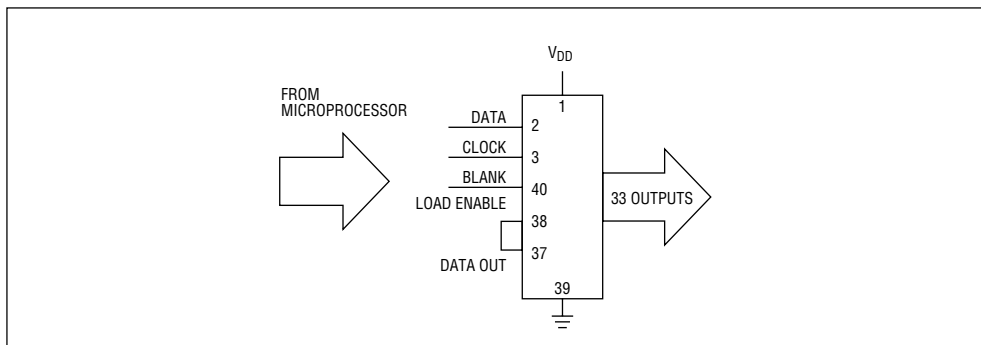
Characteristic	Symbpl	Conditions		MIN	MAX	Unit
High Level input Voltage	V _{IH}	V _{DD} =8 to 18V		3.5	V _{DD} +0.3	V
Low Level Input Voltage	V _{IL}	V _{DD} =8 to 18V		-0.3	0.8	V
High Input Current (PIN 2,3,38)	I _{IH1}	V _{DD} =8 to 18V, V _I =V _{DD}		-	1	μA
Low Input Current (PIN 2,3,38)	I _{IL1}	V _{DD} =8 to 18V, V _I =V _{SS}		-	-1	μA
High Input Current (PIN 40)	I _{IH2}	V _{DD} =8 to 18V, V _I =3.5V		-5	-125	μA
Low Input Current (PIN 40)	I _{IL2}	V _{DD} =8 to 18V, V _I =V _{SS}		-5	-125	μA
Supply Current	I _{DD}	V _{DD} =8 to 16V, All Outputs open Ta= -40°C, 25°C		-	10	mA
		V _{DD} =8 to 16V, All Outputs open Ta=85°C		-	7	mA
Low Current Output Drivers (ON) (PIN4-16, 25-36)	V _{OH1}	V _{DD} =9.5V, I _{OH} = -1.5mA	Ta= 25°C -40°C	V _{DD} -0.3	-	V
			Ta= 85°C	V _{DD} -0.5	-	
High Current Output Drivers (ON)(PIN 17-24)	V _{OH2}	V _{DD} =9.5V, I _{OH} = -6mA	Ta= 25°C -40°C	V _{DD} -0.3	-	V
			Ta= 85°C	V _{DD} -0.5	-	
	V _{OH2}	V _{DD} =9.5V, I _{OH} = -30mA	Ta= 25°C -40°C	V _{DD} -2.0	-	V
			Ta= 85°C	V _{DD} -2.5	-	
Output Drivers (OFF) (PIN 4-36)	V _{OL}	V _{DD} =9.5V, I _{OL} =1μA/500μA		-	V _{SS} + 0.2 / V _{SS} + 5	V
High Voltage Data out (PIN 37)	V _{OHd}	V _{DD} 9.5V, I _{OHd} = -500μA		V _{DD} -5	-	V
Low Voltage Dataout (PIN 37)	V _{OLd}	I _{OLd} =1μA		-	V _{SS} + 0.4	V

FUNCTIONAL DESCRIPTION

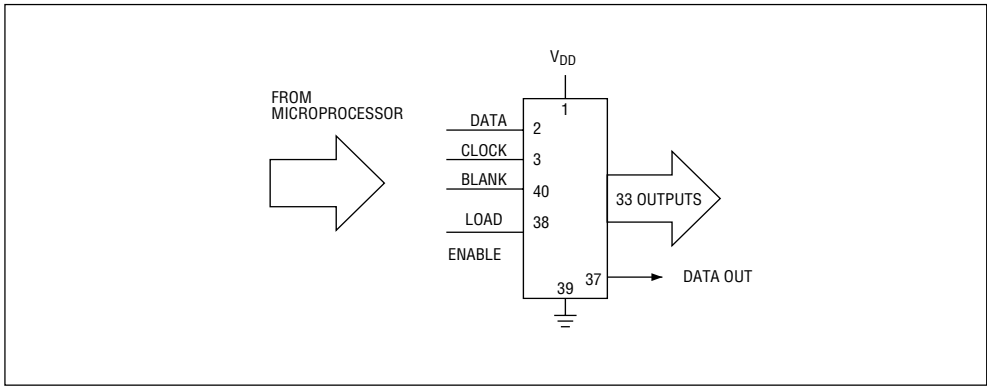
- **Data Input**
The data pattern (33 bits) supplied to the device through this input control the output driver state (On or Off).
 1. A high level turns the output driver on.
 2. A low level turns the output driver off.
- **Clock Input**
A Positive transition of the clock loads and shifts the data. This input also has a Schmitt trigger which provides 0.3 volts of hysteresis.
- **Blanking Input**
A low-level voltage at this pin turns the output drivers off; an internal pull up is provided on this pin.
- **Load Enable**
A high-level at this input transfers the data from the shift register to the data latch, and sets the shift register to zero.

First data bit read-in stored in a shift register #1, the last data bit read-in is stored in a shift register #33. When the shift registers are full, a high voltage level applied to the load enable input will transfer the data from the shift register to the data latch, and then to the output. The device has 34 shift registers and 33 data latches as shown in the functional block diagram.

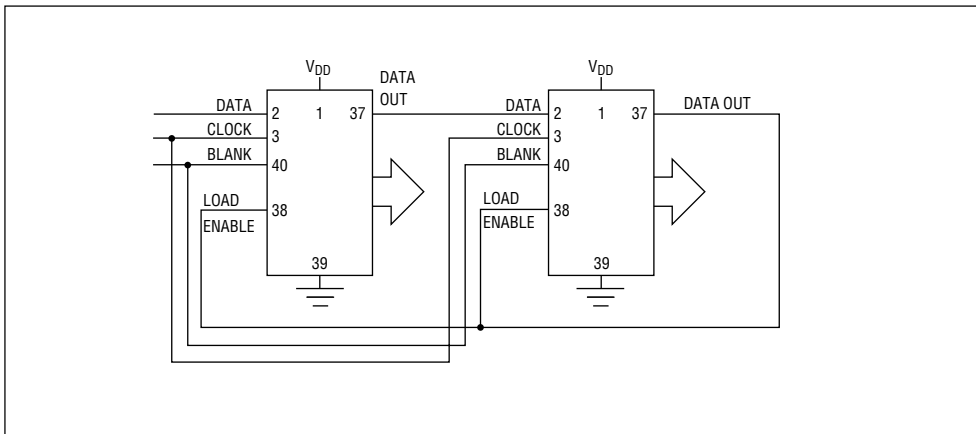
There are two modes of operation:



- **Self-Load Mode**
In this mode Data Out (pin37) is connected to Load Enable (pin38), and the data word is constructed with 33 bits (including the one self-load bit set to logic 1). At the 34th clock pulse, the data is transferred from the shift register to the data latch and the output drivers. Before the next clock pulse, the registers are zeroed.
- **Non-Self-Load Mode**
In this mode, the Data Out and the Load Enable pins are not connected, and the Load Enable input is controlled by an external source. (There are two types of operation in this mode.)
 1. The data word consists of 34 bits (including one self-load bit). To transfer data from the shift registers to the data latch, a high-level voltage is applied to the Load Enable pin before the rise of the clock pulse following the 34th clock pulse.
 2. The data word consists of 33 bits without the self-load bit. To transfer the data, a high voltage level is applied to the Load Enable pin before the rise of the 34th clock pulse.



When the display driver is used in a cascade configuration, a filler bit must be inserted between each group of 33 data bits. The filler bit must be logic 1 when used with the self-loading mode and a logic 0 when used in the non-self-loading mode.



When the cascaded devices are used in self-load mode. The Data Out pin of the last device must be connected to the Load Enable pin of all devices as shown in the above figure.

When two display drivers are cascaded, sufficient on-chip time delays allow the system to operate within the specification of the device and work in a system.

Up to 10 driver inputs may be connected to the Data Out pin (pin37) of the last device.

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