This version: Feb. 1999
Previous version: -------

OKI Semiconductor

MR53V3252J Preliminary

2,097,152-Word X 16-Bit or 4,194,304-Word X 8-Bit

8Word X 16-Bit or 16Word X 8-Bit/Page Mode MASK ROM

DESCRIPTION

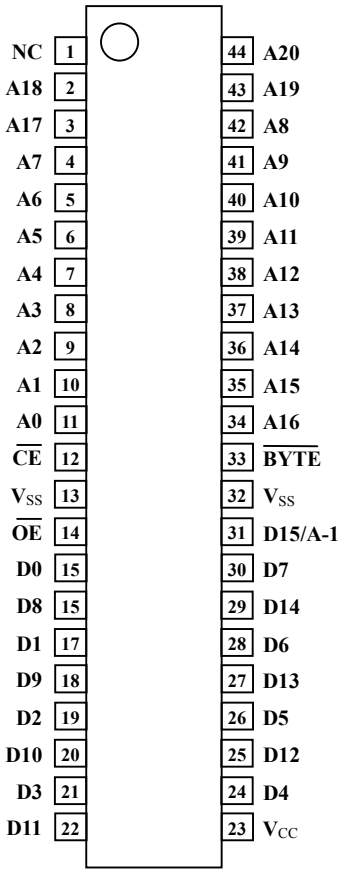
The MR53V3252J is a 32Mbit Read-Only Memory whose configuration can be electrically switched between 2,097,152 word x 16bit and 4,194,304 word x 8bit. The MR53V3252J operates asynchronously, external clocks are not required, making this device easy-to-use. The MR53V3252J is suitable as large-capacity fixed memory for microcomputers and data terminals. It is manufactured using a CMOS silicon gate technology and is offered in 44-pin SOP or 44-pin TSOP packages.

FEATURES

- 2,097,152word x 16bit / 4,194,304 word x 8bit electrically switchable configuration
- 8word x 16-Bit or 16word x 8-bit / Page read mode
- Single +2.7V~3.6V power supply
- Normal Access time 100ns (@Vcc=3.0V~3.6V)
  120ns (@Vcc=2.7V~3.3V)
- Page Access time 30ns (@Vcc=3.0V~3.6V)
  40ns (@Vcc=2.7V~3.3V)
- V_{CC} power supply current 80mA (@Vcc=3.0V~3.6V)
  70mA (@Vcc=2.7V~3.3V)
- V_{CC} standby current 10μA
- Input / Output TTL compatible
- Three-state output
- Packages

44-pin plastic SOP	(SOP44-P-600-1.27-K)	MR53V3252J-XXMA
44-pin plastic TSOP	(TSOPII44-P-400-0.80-K)	MR53V3252J-XXTP

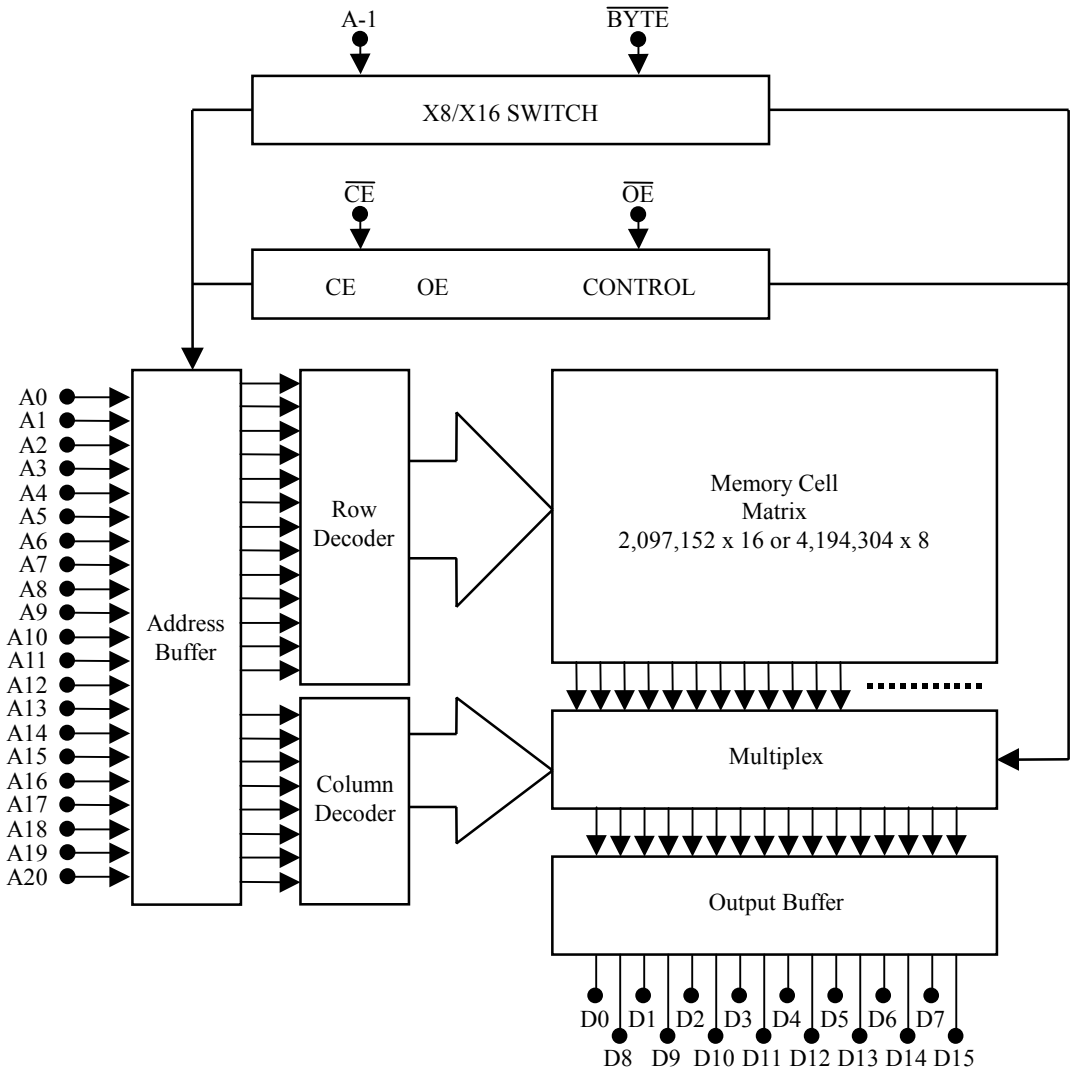
PIN CONFIGURATION (TOP VIEW)



44-Pin SOP
44-Pin TSOPII

PIN NAMES	FUNCTIONS
D15/A-1	Data output / Address input
A0~A20	Address input
D0~D14	Data output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{BYTE}$	Mode switch
V_{CC}	Power supply voltage
V_{SS}	GND
NC	Non connection

BLOCK DIAGRAM



FUNCTION TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	D0~D7	D8~D14	A-1/D15
STAND BY	H	X	X	Hi-Z		
OUTPUT DISABLE	L	H	H			
	L	H	L			L/H
READ(16-BIT)	L	L	H	D_{OUT}		
READ(8-BIT)	L	L	L	D_{OUT}	Hi-Z	L/H

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	T_{OPR}	-	0 ~ 70	`C
Storage temperature	T_{STG}	-	-55 ~ 125	`C
Input voltage	V_I	Relative to V_{SS}	-0.5 ~ V_{CC}+0.5	V
Output voltage	V_O		-0.5 ~ V_{CC}+0.5	V
Power supply voltage	V_{CC}		-0.5 ~ 5	V
Power dissipation per package	P_D	-	1.0	W

RECOMMENDED OPERATING CONDITIONS FOR READ

(Ta=0 ~ 70`C)

Parameter	Symbol	Condition	Min.	Typ.	Min.	Unit
V_{CC} power supply voltage	V_{CC}	V_{CC}=2.7V ~ 3.6V	2.7	-	3.6	`C
Input “H“ level	V_{IH}		2.2	-	V_{CC}+0.5	`C
Input “L“ level	V_{IL}		-0.5	-	0.8	V

Voltage is relative to V_{SS}

PIN Capacitance

(Vcc=3.3V, Ta=25`C, f=1MHz)

Parameter	Symbol	Condition	Min.	Typ.	Min.	Unit
Input	C_{IN}	V_I=0V	-	-	12	pF
Output	C_{OUT}	V_O=0V	-	-	15	pF

ELECTRICAL CHARACTERISTICS

DC Characteristics 1

(Vcc=2.7V~3.3V, Ta=0~70`C)

Parameter	Symbol	Condition	Min.	Typ.	Min.	Unit
Input leakage current	C_{IN}	V_I=0V~V_{CC}	-	-	10	µA
Output leakage current	C_{OUT}	V_O=0V~V_{CC}	-	-	10	µA
V_{CC} power supply current (Standby)	I_{CCSC}	$\overline{CE}$= V_{CC}	-	-	10	µA
	I_{CCST}	$\overline{CE}$= V_{IH}	-	-	1	mA
V_{CC} power supply current (Active)	I_{CCA}	$\overline{CE}$= V_{IL}, $\overline{OE}$= V_{IH} tc= 120ns	-	-	70	mA
Input “H“ level	V_{IH}	-	2.0	-	V_{CC}+0.5	V
Input “L“ level	V_{IL}	-	-0.5	-	0.8	V
Output “H“ level	V_{OH}	I_{OH}=-200 µA	V_{CC}-0.4	-	-	V
Output “L“ level	V_{OL}	I_{OL}=1mA	-	-	0.4	V

Voltage is relative to V_{SS}

DC Characteristics 2

(Vcc=3.0V~3.6V, Ta=0~70`C)

Parameter	Symbol	Condition	Min.	Typ.	Min.	Unit
Input leakage current	C_{IN}	V_I=0V~V_{CC}	-	-	10	µA
Output leakage current	C_{OUT}	V_O=0V~V_{CC}	-	-	10	µA
V_{CC} power supply current (Standby)	I_{CCSC}	$\overline{CE}$= V_{CC}	-	-	10	µA
	I_{CCST}	$\overline{CE}$= V_{IH}	-	-	1	mA
V_{CC} power supply current (Active)	I_{CCA}	$\overline{CE}$= V_{IL}, $\overline{OE}$= V_{IH} tc= 100ns	-	-	80	mA
Input “H“ level	V_{IH}	-	2.0	-	V_{CC}+0.5	V
Input “L“ level	V_{IL}	-	-0.5	-	0.8	V
Output “H“ level	V_{OH}	I_{OH}=-200 µA	V_{CC}-0.4	-	-	V
Output “L“ level	V_{OL}	I_{OL}=1mA	-	-	0.4	V

Voltage is relative to V_{SS}

AC Characteristics 1

(Vcc=2.7V~3.3V, Ta=0~70`C)

Parameter	Symbol	Condition	Min.	Min.	Unit
Address access cycle time	T_C	-	120	-	ns
Address access time	T_{ACC}	$\overline{CE}$=$\overline{OE}$= V_{IL}	-	120	ns
Page set up time	T_{PSET}	NOTE.1	120	-	ns
Page access cycle time	T_{PC}	-	40	-	ns
Page access time	T_{PAC}	-	-	40	ns
$\overline{CE}$ access time	T_{CE}	$\overline{OE}$= V_{IL}	-	120	ns
$\overline{OE}$ access time	T_{OE}	$\overline{CE}$= V_{IL}	-	40	ns
Output disable time	T_{CHZ}	$\overline{OE}$= V_{IL}	0	35	ns
	T_{OHZ}	$\overline{CE}$= V_{IL}	0	30	ns
Output hold time	T_{OH}	$\overline{CE}$=$\overline{OE}$= V_{IL}	0	-	ns

AC Characteristics 2

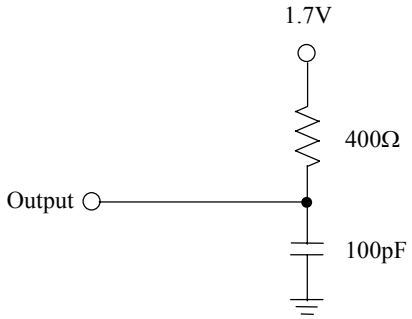
(Vcc=3.0V~3.6V, Ta=0~70`C)

Parameter	Symbol	Condition	Min.	Min.	Unit
Address access cycle time	T_C	-	100	-	ns
Address access time	T_{ACC}	$\overline{CE}$=$\overline{OE}$= V_{IL}	-	100	ns
Page set up time	T_{PSET}	NOTE.1	100	-	ns
Page access cycle time	T_{PC}	-	30	-	ns
Page access time	T_{PAC}	-	-	30	ns
$\overline{CE}$ access time	T_{CE}	$\overline{OE}$= V_{IL}	-	100	ns
$\overline{OE}$ access time	T_{OE}	$\overline{CE}$= V_{IL}	-	30	ns
Output disable time	T_{CHZ}	$\overline{OE}$= V_{IL}	0	30	ns
	T_{OHZ}	$\overline{CE}$= V_{IL}	0	25	ns
Output hold time	T_{OH}	$\overline{CE}$=$\overline{OE}$= V_{IL}	0	-	ns

NOTE.1 T_{PSET} is defined as the end of either $\overline{CE}$ falling edge or address transition in random access term until the first page address transition.

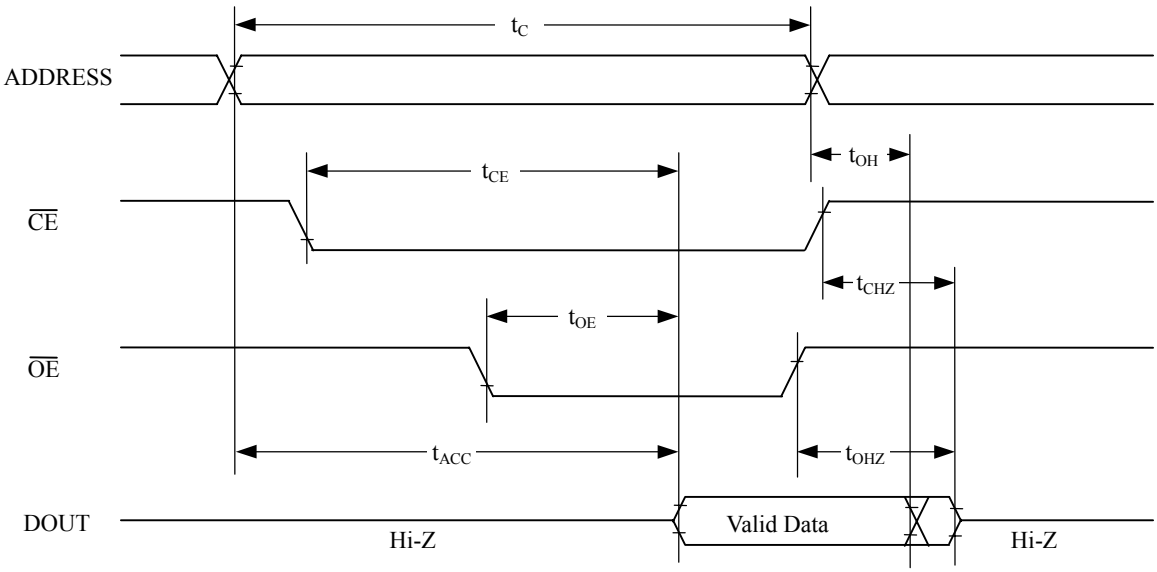
Measurement condition

Input signal level	0V/3V
Input timing reference level	0.8V/2.0V
Output load	100pF
Output timing reference level	0.8V/2.0V

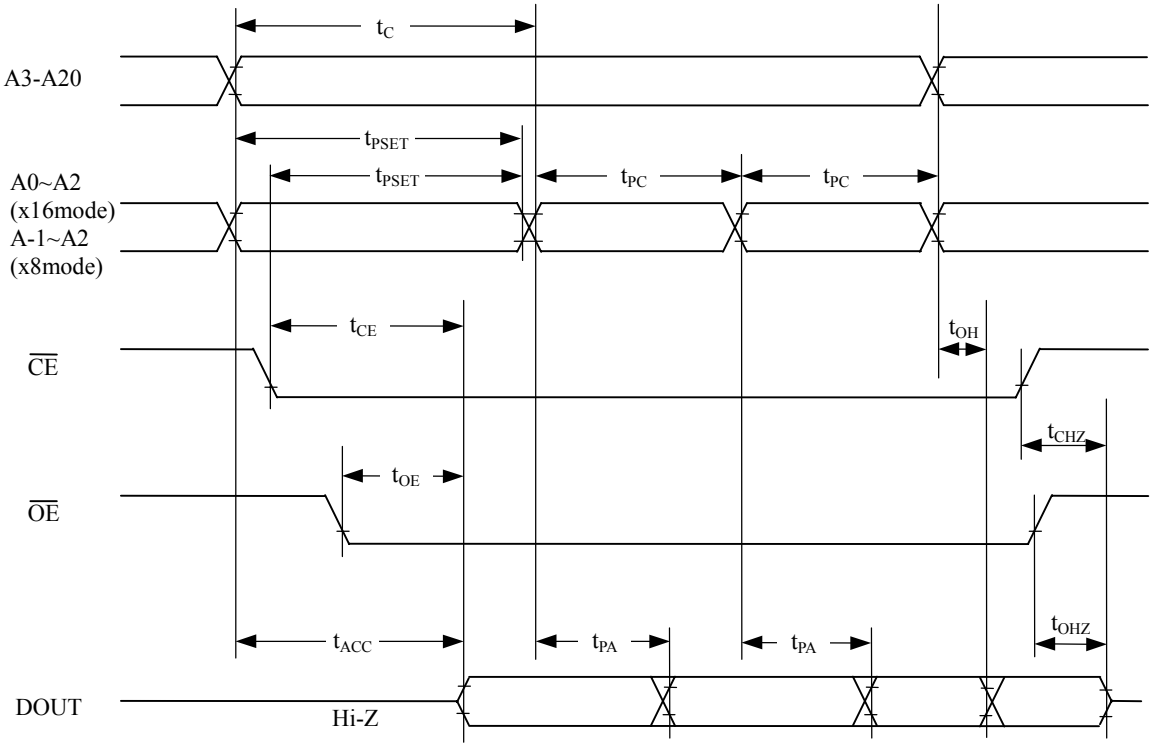


TIMING CHART

NORMAL MODE READ CYCLE



PAGE MODE READ CYCLE



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