PEDL674000-01

OKI Semiconductor

This version: Oct. 2001

ML674000 Preliminary

µPLAT-7B Based Microcontroller

GENERAL DESCRIPTION

This LSI incorporates µPLAT®-7B, employing the CPU core ARM7TDMI™, as the CPU platform and operates at maximum 33 MHz. It contains built-in RAM and peripheral IOs such as Timer, WDT, GPIO, PWM, UART (16550 compatible), AD converter, DMA controller and DRAM controller, etc. and can be used as a microcontroller for configuring various systems.

FEATURES

CPU platform (µPLAT-7B)	CPU core	ARM7TDMI 32-bit instructions (ARM instructions) and 16-bit instructions (Thumb instructions) mixed Execution Possible General register bank: 31 × 32 bits Parallel shifter (continuous processing with ALU) Multiplier: 32 × 8 (Modified Booth's Algorithm)
	Interrupt controller	13 Sources: (internal: 8, external: IRQ (4), FIQ (1))
	External memory controller	ROM (or Flash), SRAM, and IO device interface
	Timer	1 channel: 16-bit auto-reload (for OS)
	Serial interface	1 channel: Xon/Xoff interface
	Power down mechanism	Halt, Stop
	Test controller	AMBA TIC (Test Interface Controller)
	JTAG interface	connectable to ADI (*)/ARM MutiICE.
Internal memory	RAM	8 KB: processor bus connection
CPU peripheral device (AHB device)	Extension interrupt controller	10 Sources (internal)
	DMAC	2 channels: dual address mode, cycle steal.
CPU peripheral device (APB device)	UART	1 channel: with 16-byte FIFO
	Timer	6 channels: 16-bit auto reload
	PWM	2 channels × 16 bits
	PIO	2 channels × 16 bits
	AD converter	8 channels × 10 bits
Input clock	Oscillator input	16 MHz to 33 MHz
	External oscillator input	To 33 MHz
Power supply voltage	Core section	2.25 V to 2.75 V
	IO section	3.0 V to 3.6 V
Operating frequency		33 MHz (Max.)
Operating temperature (ambient temperature)		–40°C to +85°C
Package		128-pin plastic TQFP (TQFP128-P-1414-0.40-K)

(*) ADI: ARM Debug Interface

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µPLAT is Oki's trademark.
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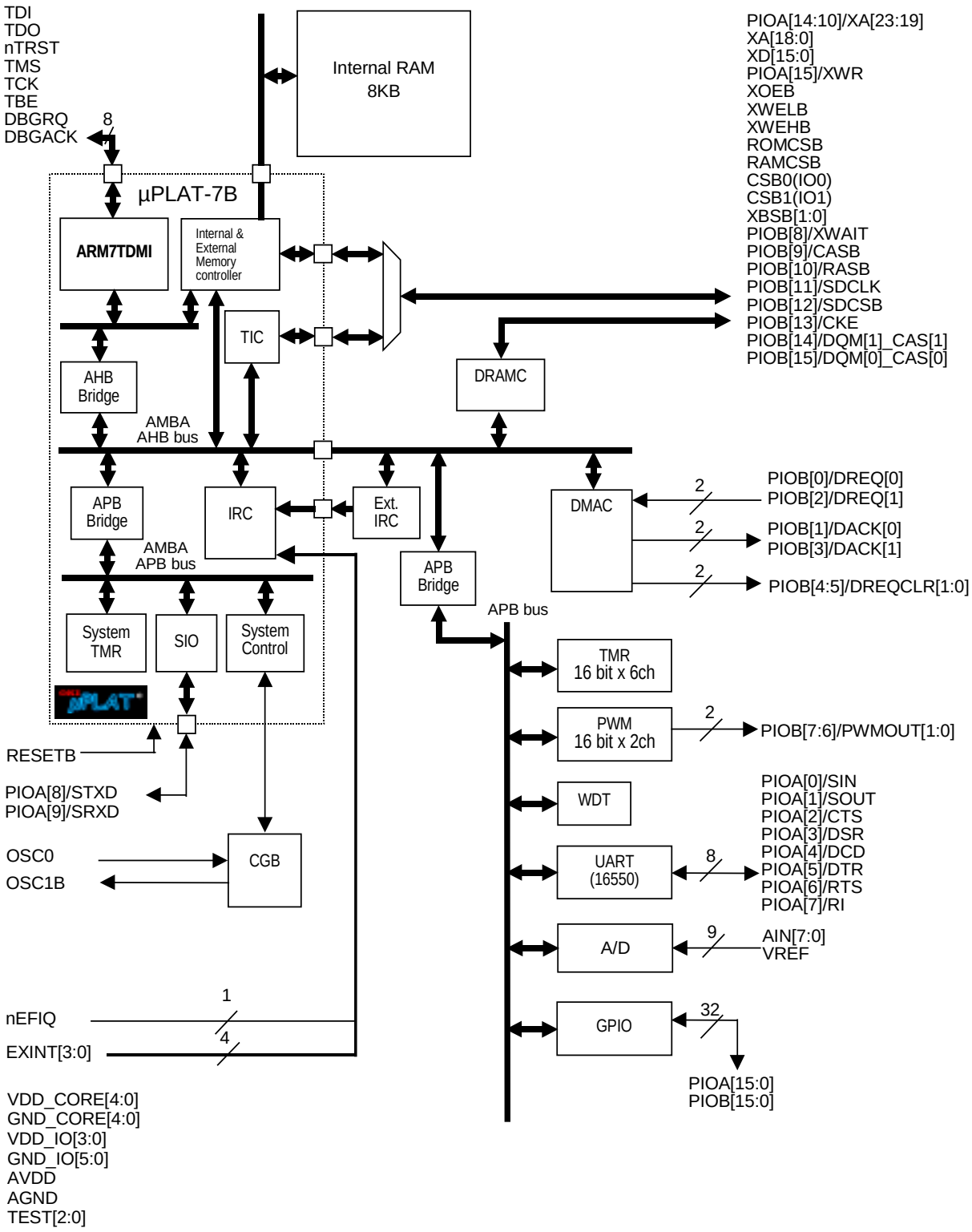
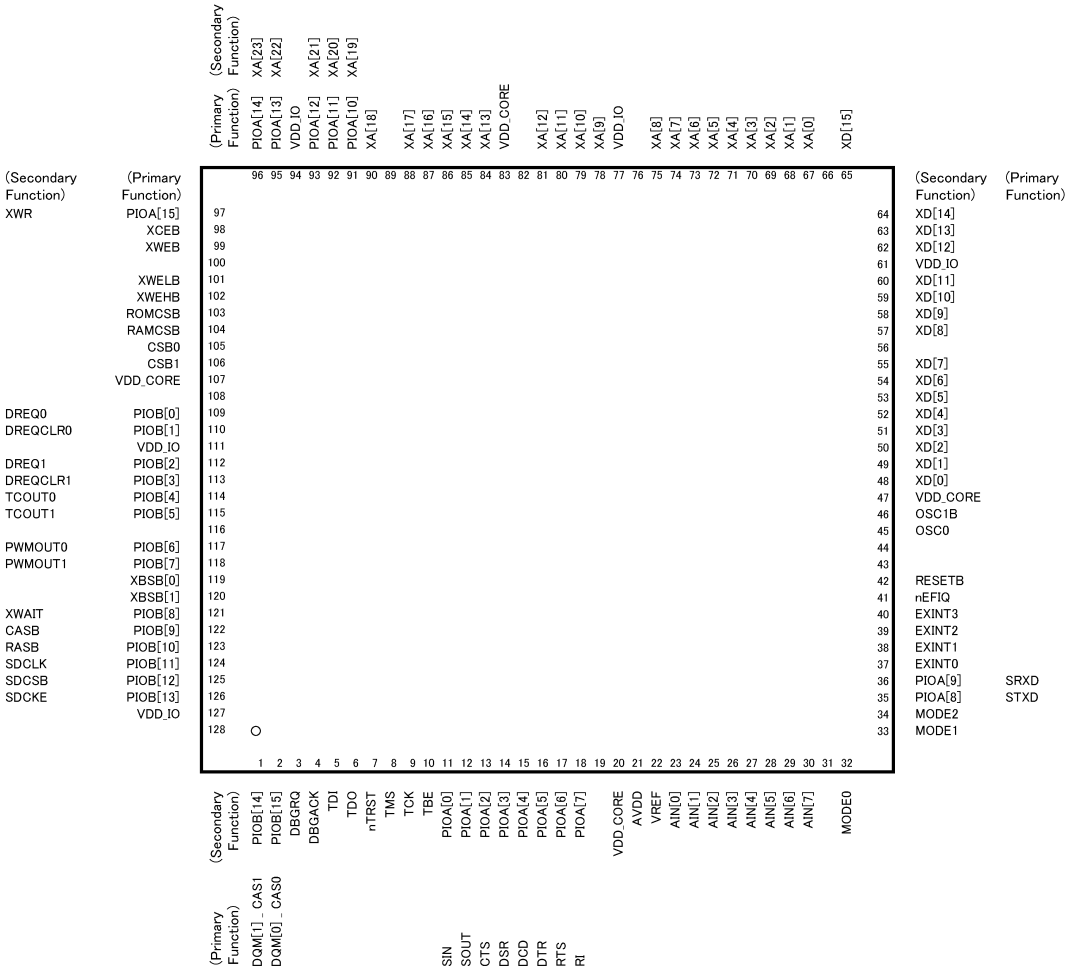
BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



128-Pin Plastic TQFP

LIST OF PINS

Pin	Primary Function			Secondary Function		
	Symbol	Type	Description	Symbol	Type	Description
1	PIOB[14]	I/O	General port (with interrupt function)	DQM[1]_CAS1	O	INPUT/OUTPUT mask/CAS (MSB)
2	PIOB[15]	I/O	General port (with interrupt function)	DQM[0]_CAS0	O	INPUT/OUTPUT mask/CAS (LSB)
3	DBGRQ	I	Input signal for debug	—		
4	DBGACK	O	Output signal for debug	—		
5	TDI	I	JTAG data input	—		
6	TDO	O	JTAG data output	—		
7	nTRST	I	JTAG reset	—		
8	TMS	I	JTAG mode selection	—		
9	TCK	I	JTAG clock	—		
10	TBE	I	Input signal for testing	—		
11	PIOA[0]	I/O	General port (with interrupt function)	SIN	I	UART Serial Data In
12	PIOA[1]	I/O	General port (with interrupt function)	SOUT	O	UART Serial Data Out
13	PIOA[2]	I/O	General port (with interrupt function)	CTS	I	UART Clear To Send
14	PIOA[3]	I/O	General port (with interrupt function)	DSR	I	UART Data Set Ready
15	PIOA[4]	I/O	General port (with interrupt function)	DCD	I	UART Data Carrier Detect
16	PIOA[5]	I/O	General port (with interrupt function)	DTR	O	UART Data Terminal Ready
17	PIOA[6]	I/O	General port (with interrupt function)	RTS	O	UART Request To Send
18	PIOA[7]	I/O	General port (with interrupt function)	RI	I	UART Ring Indicator
19	GND_CORE	GND	GND for CORE	—		
20	VDD_CORE	VDD	Power supply for CORE	—		
21	AVDD	VDD	Power supply for A/D converter	—		
22	VREF	I	Reference voltage for A/D converter	—		
23	AIN[0]	I	A/D converter analog input port	—		
24	AIN[1]	I	A/D converter analog input port	—		
25	AIN[2]	I	A/D converter analog input port	—		
26	AIN[3]	I	A/D converter analog input port	—		
27	AIN[4]	I	A/D converter analog input port	—		
28	AIN[5]	I	A/D converter analog input port	—		
29	AIN[6]	I	A/D converter analog input port	—		
30	AIN[7]	I	A/D converter analog input port	—		
31	AGND	GND	GND for A/D converter	—		
32	MODE0	I	Mode setting	—		
33	MODE1	I	Mode setting	—		
34	MODE2	I	Mode setting	—		
35	PIOA[8]	I/O	General port (with interrupt function)	STXD	O	SIO send data output
36	PIOA[9]	I/O	General port (with interrupt function)	SRXD	I	SIO receive data input
37	EXINT[0]	I	Interrupt input	—	—	—
38	EXINT[1]	I	Interrupt input	—	—	—

Pin	Primary Function			Secondary Function		
	Symbol	Type	Description	Symbol	Type	Description
39	EXINT[2]	I	Interrupt input	—	—	—
40	EXINT[3]	I	Interrupt input	—	—	—
41	nEFIQ	I	FIQ input	—	—	—
42	RESETB	I	Reset	—	—	—
43	GND_IO	GND	GND for I/O	—	—	—
44	GND_CORE	GND	GND for CORE	—	—	—
45	OSC0	I	Oscillation input pin	—		
46	OSC1B	O	Oscillation output pin	—		
47	VDD_CORE	VDD	Power supply for CORE	—		
48	XD[0]	I/O	External memory access data port	—		
49	XD[1]	I/O	External memory access data port	—		
50	XD[2]	I/O	External memory access data port	—		
51	XD[3]	I/O	External memory access data port	—		
52	XD[4]	I/O	External memory access data port	—		
53	XD[5]	I/O	External memory access data port	—		
54	XD[6]	I/O	External memory access data port	—		
55	XD[7]	I/O	External memory access data port	—		
56	GND_IO	GND	GND for I/O	—		
57	XD[8]	I/O	External memory access data port	—		
58	XD[9]	I/O	External memory access data port	—		
59	XD[10]	I/O	External memory access data port	—		
60	XD[11]	I/O	External memory access data port	—		
61	VDD_IO	VDD	Power supply for I/O	—		
62	XD[12]	I/O	External memory access data port	—		
63	XD[13]	I/O	External memory access data port	—		
64	XD[14]	I/O	External memory access data port	—		
65	XD[15]	I/O	External memory access data port	—		
66	GND_IO	GND	GND for I/O	—		
67	XA[0]	O	External memory access address output port	—		
68	XA[1]	O	External memory access address output port	—		
69	XA[2]	O	External memory access address output port	—		
70	XA[3]	O	External memory access address output port	—		
71	XA[4]	O	External memory access address output port	—		
72	XA[5]	O	External memory access address output port	—		
73	XA[6]	O	External memory access address output port	—		
74	XA[7]	O	External memory access address output port	—		
75	XA[8]	O	External memory access address output port	—		
76	GND_IO	GND	GND for I/O	—		
77	VDD_IO	VDD	Power supply for I/O	—		
78	XA[9]	O	External memory access address output port	—		
79	XA[10]	O	External memory access address output port	—		

Pin	Primary Function			Secondary Function		
	Symbol	Type	Description	Symbol	Type	Description
80	XA[11]	O	External memory access address output port	—		
81	XA[12]	O	External memory access address output port	—		
82	GND_CORE	GND	GND for CORE	—		
83	VDD_CORE	VDD	Power supply for CORE	—		
84	XA[13]	O	External memory access address output port	—		
85	XA[14]	O	External memory access address output port	—		
86	XA[15]	O	External memory access address output port	—		
87	XA[16]	O	External memory access address output port	—		
88	XA[17]	O	External memory access address output port	—		
89	GND_IO	O	GND for I/O	—		
90	XA[18]	O	External memory access address output port	—		
91	PIOA[10]	I/O	General port (with interrupt function)	XA[19]	O	External memory access address output port
92	PIOA[11]	I/O	General port (with interrupt function)	XA[20]	O	External memory access address output port
93	PIOA[12]	I/O	General port (with interrupt function)	XA[21]	O	External memory access address output port
94	VDD_IO	VDD	Power supply for I/O			
95	PIOA[13]	I/O	General port (with interrupt function)	XA[22]	O	External memory access address output port
96	PIOA[14]	I/O	General port (with interrupt function)	XA[23]	O	External memory access address output port
97	PIOA[15]	I/O	General port (with interrupt function)	XWR	O	Transfer direction of XBUS
98	XOEB	O	Output enable (excluding SDRAM)	—		
99	XWEB	O	Write enable	—		
100	GND_IO	GND	GND for I/O			
101	XWELB	O	Write enable (LSB)	—		
102	XWEHB	O	Write enable (MSB)	—		
103	ROMCSB	O	External ROM chip select	—		
104	RAMCSB	O	External RAM chip select	—		
105	CSB0	O	IO bank 0 chip select	—		
106	CSB1	O	IO bank 1 chip select	—		
107	GND_CORE	GND	GND for CORE	—		
108	VDD_CORE	VDD	Power supply for CORE	—		
109	PIOB[0]	I/O	General port (with interrupt function)	DREQ0	I	DMA request signal (CH0)
110	PIOB[1]	I/O	General port (with interrupt function)	DREQCLR0	O	DREQ clear signal (CH0)
111	VDD_IO	VDD	Power supply for I/O	—		
112	PIOB[2]	I/O	General port (with interrupt function)	DREQ1	I	DMA request signal (CH1)
113	PIOB[3]	I/O	General port (with interrupt function)	DREQCLR1	O	DREQ clear signal (CH1)
114	PIOB[4]	I/O	General port (with interrupt function)	TCOUT0	O	DMAC Terminal Count (CH0)
115	PIOB[5]	I/O	General port (with interrupt function)	TCOUT1	O	DMAC Terminal Count (CH1)
116	GND_IO	GND	GND for I/O	—		
117	PIOB[6]	I/O	General port (with interrupt function)	PWMOUT[0]	O	PWM output (CH0)
118	PIOB[7]	I/O	General port (with interrupt function)	PWMOUT[1]	O	PWM output (CH1)
119	XBSB[0]	I/O	XBUS byte select (LSB)	—		
120	XBSB[1]	I/O	XBUS byte select (MSB)	—		

Pin	Primary Function			Secondary Function		
	Symbol	Type	Description	Symbol	Type	Description
121	PIOB[8]	I/O	General port (with interrupt function)	XWAIT	O	
122	PIOB[9]	I/O	General port (with interrupt function)	CASB	O	Column address strobe (SDRAM)
123	PIOB[10]	I/O	General port (with interrupt function)	RASB	O	Row address strobe (SDRAM/EDO)
124	PIOB[11]	I/O	General port (with interrupt function)	SDCLK	O	Clock for SDRAM
125	PIOB[12]	I/O	General port (with interrupt function)	SDCSB	O	SDRAM chip select
126	PIOB[13]	I/O	General port (with interrupt function)	SDCKE	O	Clock enable (To SDRAM)
127	VDD_IO	VDD	Power supply for I/O	—		
128	GND_IO	GND	GND for I/O	—		

PIN DESCRIPTION

Pin	Symbol	Type	Description	Primary/ Secondary	Logic
System					
	RESETB	I	Reset	—	Negative
	OSC0	I	Oscillator connecting pin/clock input When connecting crystal oscillator, connect to OSC0 and OSC1B. 16 MHz to 33 MHz oscillator is supported. When less than 16 MHz oscillator is used, clock is directly input to this pin.	—	
	OSC1B	O	Oscillator connecting pin. When connecting crystal oscillator to OSC0 alone, leave this pin open.	—	
	TBE	I	Input pin for testing. In normal operation, connect it to GND.		Negative
Debug support					
	DBGREQ	I	Input pin used to make the CPU enter a debugging state. In normal operation, connect it to GND.		Positive
	DBGACK	O	Output pin used to indicate that the CPU is in a debugging state. In normal operation, leave it open		Positive
	TCK	I	JTAG pin. Used at the time of debugging and ARM test. In normal operation, input low level.		—
	TMS	I	JTAG pin. Used at the time of debugging and ARM test. In normal operation, input high level. The JTAG standard recommends this pin to be pulled up, but this pin is not pulled up in the ML674000.		Positive
	NTRST	I	JTAG pin. Used at the time of debugging and ARM test. In normal operation, input low level.		Negative
	TDI	I	JTAG pin. Used at the time of debugging and ARM test. In normal operation, input high level. The JTAG standard recommends this pin to be pulled up, but this pin is not pulled up in the ML674000.		Positive
	TD0	O	JTAG pin. Used at the time of debugging and ARM test. In normal operation, leave it open.		Positive

(*) OKI ADI board : OKI ARM Debug Interface board
Debugging interface board having the same interface as Multi -ICE of ARM Ltd. Oki Electric is selling it under license from the ARM Ltd.

Pin	Symbol	Type	Description	Primary/ Secondary	Logic
General I/O Port					
	PIOA[15:0]	I/O	General port. For details, refer to the description of PIO. It possesses secondary function, but can not be used as PIO when using secondary function.	Primary	Positive
	PIOB[15:]0	I/O	General port. For details, refer to the description of PIO. It possesses secondary function, but can not be used as PIO when using secondary function. Since PIOB [15:9] gets locked to the secondary function when DRAM controller is activated by means of MODE [2:0], it can not be used as PIO.	Primary	Positive
External Bus					
	XA[23:19]	O	This bus becomes bi-directional when external RAM, external ROM, and external IO connection bus are in address test mode. It is set to primary function PIOA [14:10] immediately after reset.	Secondary	Positive
	XA[18:0]	O	Address bus for external RAM, external ROM, and external IO connection bus. This bus becomes bi-directional in test mode.		Positive
	XD[15:0]	I/O	Data bus for external RAM, external ROM, and external IO connection bus bus.		Positive
External Bus Control Signal					
	ROMCSB	O	ROM bank chip select 1: ROM bank not selected 0: ROM bank selected		Negative
	RAMCSB	O	SRAM bank chip select 1: SRAM bank not selected 0: SRAM bank selected		Negative
	CSB0	O	IO bank 0 chip select 1: IO bank 0 not selected 0: IO bank 0 selected		Negative
	CSB1	O	IO bank 1 chip select 1: IO bank 1 not selected 0: IO bank 1 selected		Negative
	XOEB	O	Output enable/read enable		Negative
	XWEB	O	Write enable. Connect to WE signal of DRAM (used together with XBSB at the time of byte write of RAM bank, ROM bank, IO bank 0/1).		Negative
	XBSB[1:0]	O	Byte select. XBSB [1]: MSB, XBSB [0]: LSB		Negative
	XWELB	O	LSB write enable		Negative
	XWEHB	O	MSB write enable		Negative

Pin	Symbol	Type	Description	Primary / Secondary	Logic
	XWR	O	Indicates data transfer direction of X bus of IO bank. Used to connect to Motorola type IO device. 0: Read 1: Write Since XWR is allocated to secondary function, it is controlled by GPCTL when it is used.	Secondary	—
	XWAIT	I	WAIT signal of IO bank 0. By inputting this signal, it is possible to connect a device slower than register setting. This function can not be used in IO bank 1.	Secondary	Positive
External Bus Control Signal (DRAM)					
	RASB	O	Row address strobe signal Used in both EDO-DRAM and SDRAM	Secondary	Negative
	CASB	O	Column address strobe signal (for SDRAM)	Secondary	Negative
	CLK	O	Clock for SDRAM (has the same frequency as that of internal system clock)	Secondary	—
	CKE	O	Clock enable (for SDRAM)	Secondary	—
	SDCSB	O	Chip select (for SDRAM)	Secondary	Negative
	DQM[1]_ CAS1	O	When connecting to SDRAM: DQM (MSB) When connecting to EDO.- DRAM: Column address strobe signal (MSB)	Secondary	Positive
	DQM[0]_ CAS0	O	When connecting to SDRAM: DQM (LSB) When connecting to EDO.- DRAM: Column address strobe signal (LSB)	Secondary	Positive
DMA Control Signal					
	DREQ0	I	CH0DMA request signal. Valid when set to DREQ type by DMAC.	Secondary	Positive
	DREQCLR0	O	CH0DREQ signal clear request. When this signal is output, the DMA device turns off DREQ. When transferring by cycle steal, the next transfer does not start unless DREQCLR signal is output for every 1 transfer and DREQ is negated. At the time of Burst transfer, it is output when the last transfer starts.	Secondary	Positive
	TCOUT0	O	Indicates that the last transfer has started with regard to CH0DMA device.	Secondary	Positive
	DREQ1	I	CH1DMA request signal. Becomes valid when set to DREQ type by DMAC.	Secondary	Positive

Pin	Symbol	Type	Description	Primary / Secondary	Logic
	DREQCLR1	O	CH1DREQ request signal. When this signal is output, the DMA device turns off DREQ. When transferring by cycle steal , the next transfer does not start unless DREQCLR signal is output for every 1 transfer and DREQ is negated. At the time of Burst transfer, it is output when the last transfer starts.	Secondary	Positive
	TCOUT1	O	Indicates that the last transfer has started with regard to CH1DMA device.	Secondary	Positive
SIO					
	STXD	O	SIO send signal Since it is allocated to secondary function, setting to secondary function by GPCTL is necessary.	Secondary	Positive
	SRXD	I	SIO receive signal Since it is allocated to secondary function, setting to secondary function by GPCTL is necessary.	Secondary	Positive
UART					
	SIN	I	Serial In. Serial data input.	Secondary	Positive
	SOUT	O	Serial Out. Serial data output.	Secondary	Positive
	CTS	I	Clear To Send Indicates that data send / receive preparation is complete on MODEM or data set side. This signal is MODEM status input signal and input status is reflected on bit 4 of MODEM status register.	Secondary	Negative
	DSR	I	Data Set Ready Indicates that MODEM or data set side has completed preparation for establishing communication link with UART. This signal is MODEM status input signal and input status is reflected on bit 5 of MODEM status register.	Secondary	Negative
	DCD	I	Data Carrier Detect Indicates that MODEM or data set side has detected data carrier signal. This signal is modem status input signal and input status is reflected on bit 7 of MODEM status register.	Secondary	Negative
	DTR	O	Data Terminal Ready Indicates that UART has completed preparation for establishing communication link with MODEM or data set side. This signal is MODEM control output signal and the status set in bit 0 of MODEM control register is output to this signal.	Secondary	Negative

Pin	Symbol	Type	Description	Primary / Secondary	Logic
	RTS	O	Request To Send Informs MODEM or data set side of completion of data send/receive preparation on UART side. This signal is modem control output signal and the status set in bit 1 of MODEM control register is output to this signal.	Secondary	Negative
	RI	O	Ring Indicator Indicates that telephone call signal has been received by modem or data set side. This signal is MODEM status input signal and the input status is reflected on bit 6 of MODEM status register.	Secondary	Negative
PWM Signal					
	PWMOUT[0]	O	PWM output of CH0 Since it possesses secondary function, it can not be used as PIO when secondary function is used.	Secondary	Positive
	PWMOUT[1]	O	PWM output of CH1 Since it possesses secondary function, it can not be used as PIO when secondary function is used.	Secondary	Positive
AD					
	AIN[0]	I	Ch0 analog input		
	AIN[1]	I	Ch1 analog input		
	AIN[2]	I	Ch2 analog input		
	AIN[3]	I	Ch3 analog input		
	AIN[4]	I	Ch4 analog input		
	AIN[5]	I	Ch5 analog input		
	AIN[6]	I	Ch6 analog input		
	AIN[7]	I	Ch7 analog input		
	VREF	I	Reference voltage for AD converter		
	AVDD		Power supply for AD converter		
	AGND		Ground for AD converter		
Interrupt Signal					
	EXINT[3:0]	I	External interrupt input signal		Positive/ Negative
	nEFIQ	I	External interrupt input signal. Gets connected to FIQ input of ARM through interrupt control section.		Negative
MODE					
	MODE[2:0]	I	Operating mode signal. For details, refer to (TBD).		

Pin	symbol	Type	Description	Primary / Secondary	Logic
Power supply					
	VDD_CORE		Power supply for core		
	VDD_IO		Power supply for IO		
	GND_CORE		Ground for core		
	GND_IO		Ground for IO		

DESCRIPTION OF FUNCTIONS

CPU

CPU core:	ARM7TDMI
Operating frequency:	1 MHz to 33 MHz
Instructions:	ARM instruction (32-bit length) and Thumb instruction (16-bit length) can be mixed.
General register bank:	31 × 32 bits
Built-in barrel shifter:	ALU and barrel shift operations can be executed by one instruction.
Multiplier:	32 bits × 8 bits (Modified Booth's Algorithm)
Built-in debug function:	JTAG interface, break point register

Built-in Memory

RAM:	8 KB (2K × 32 bits) Connected to processor bus (1 cycle access)

Interrupt Controller

Fast interrupt input (FIQ) and interrupt input (IRQ) are employed as interrupt input signals of ARM core. The interrupt controller controls these interrupt signals going to ARM core.

(1) Interrupt sources of ML674000
FIQ: 1 source, external source (external pin: NEFIQ)
IRQ: 22 sources, internal sources : 18, external sources : 4 (external pins: EXINT [3 : 0])
(2) Interrupt priority level
Priority can be set in 8 levels for each source.
(3) External interrupt pin input
Level sense: Interrupt signal level is selected.
Edge sense: Rise or fall is selected.

Timer

7 channels of 16-bit reload timers are employed. Of these, 1 channel is used as system timer for OS.
The timers of other 6 channels are used in application software.

(1) System timer: 1 channel
16-bit auto reload timer: Used as system timer for OS
(This timer is incorporated in µPLAT-7B.)
(2) Application timer: 6 channels
16-bit auto reload timer
One shot, interval
Clock can be set for each channel

WDT

Possesses the function of interval timer mode in addition to the watch dog timer function.

(1) 16-bit timer
(2) Watch dog timer or interval timer mode can be selected
(3) Interrupt reset generation
(4) Maximum period: 200 msec or longer

PWM

This LSI contains two channels of PWM (Pulse Width Modulation) function which can change the duty in a certain fixed period. The PWM output resolution is 16 bits for each channel.

Serial Interface
This LSI contains two channels of serial interface.

(1) Start-stop synchronous serial interface without FIFO: 1 channel
This serial interface is incorporated in µPLAT-7B.
(2) Start-stop synchronous serial interface with 16-byte FIFO: 1 channel
This is ACE (Asynchronous Communication Element) equivalent in function to 16550A. It has 16-byte FIFO in both sending and receiving.

PIO
This LSI contains two channels 16-bit parallel port.

(1) Input or output can be selected for each bit.
(2) Interrupt can be used for all 16 bits of each channel and interrupt is possible for each channel.
(3) Interrupt mask and interrupt mode (level) can be set for all bits.
(4) Input state immediately after reset.

AD Converter
Successive approximation type AD converter.

(1) 10 bits × 8 channels
(2) Sample hold function
(3) Scan mode and select mode are supported
(4) Interrupt is generated after completion of conversion.
(5) Conversion time: shortest about 5 µs.

DMAC
Two channels of direct memory access controller which transfers data between memory and memory, between I/O and memory and between I/O and I/O.

(1) Number of channels: 2 channels
(2) Channel priority level: Fixed mode
Channel priority level is always fixed (channel 0 > 1).
Roundrobin
Priority level of the channel requested for transfer is kept lowest.
(3) Maximum number of transfers: 65,536 times (64K times)
(4) Data transfer size: Byte (8 bits), half-word (16 bits), word (32 bits)
(5) Bus request system: Cycle steal mode
Bus request signal is asserted for each DMA transfer cycle.
Burst mode:
Bus request signal is asserted until all transfers of transfer cycles are complete.
(6) DMA transfer request: Software request
By setting the software transfer request bit inside DMAC, the CPU starts DMA transfer.
External request
DMA transfer is started by external request allocated to each channel.
(7) Interrupt request: Interrupt request is generated in CPU after the end of DMA transfers for the set number of transfer cycles or after occurrence of error.
Interrupt request signal is output separately for each channel.
Interrupt request signal output can be masked for each channel.

External memory controller
Controls access of externally connected devices such as ROM (FLASH), SRAM, SDRAM (EDO DRAM) and IO devices.

(1) ROM (FLASH) access function
Supports 16-bit device: ROMCSB
Supports FLASH memory: Byte write (can be written only by IF equivalent to SRAM).
Access timing setting
(2) SRAM access function
Supports 16-bit device: RAMCSB
Supports asynchronous SRAM
Access timing setting
(3) DRAM access function
Supports 16-bit device: SDCSB
Supports EDO/SDRAM: Simultaneous connections to EDO-DRAM and SDRAM cannot be made.
Access timing setting
(4) External IO access function
Supports 8-bit/16-bit device: CSB0 / CSB1
Supports 2 banks independently
Supports external wait input: XWAIT (CSB0 only)
Access timing setting (for each bank)

Power Management
HALT and STOP functions are supported as power save functions.

(1) HALT mode
HALT object
CPU, internal RAM, AHB bus control
HALT mode setting: Set by the system control register.
HALT mode cancelling: Reset, interrupt
(2) STOP mode
Stops the clock of entire LSI.
STOP mode setting: Specified by the system control register.
STOP mode cancelling: Reset, external interrupt (other than FIQ)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit	Remark
Power supply voltage	$V_{DD\ core}$	Ta = 25 °C V_{SS} = 0V (Typ.)	–0.3 to +3.6	V	Power supply for internal cell.
	$V_{DD\ io}$		–0.3 to +4.6		Power supply for IO
Input voltage	V_i		–0.3 to V_{DDio} +0.3		
Permissible power dissipation	P_d		TBD	mW	
Storage temperature	T_{stg}		–50 to +150	°C	

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage (core)	$V_{DD\ core}$	—	2.25	2.5	2.75	V
Power supply voltage (I/O, analog)	$V_{DD\ io}$	A single power supply is applied to I/O and analog circuits.	3.0	3.3	3.6	V
“H” level input voltage	V_{ih}	—	2.0	—	V_{DDio} +0.3	V
“L” level input voltage	V_{il}	—	–0.3		0.8	V
Operating temperature	Ta	—	–40	—	85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
“H” level input voltage	V_{oh}	TBD	TBD	TBD	TBD	V
“L” level input voltage	V_{ol}	TBD	TBD	TBD	TBD	V
Input leakage current	I_i	TBD	TBD	TBD	TBD	uA
Output leakage current	I_o	TBD	TBD	TBD	TBD	uA
Power supply current (operating)	I_{ddo}	TBD	TBD	TBD	TBD	uA
Power supply current (standby)	I_{dds}	TBD	TBD	TBD	TBD	uA

AC Characteristics

TBD

DEVELOPMENT ENVIRONMENT

Software Development Toolkit

• SDT 2.51
  ARM Software Development Toolkit (C Compiler, C Linker, Assembler)
• µPLAT-7B SDT (Under Development)
  SDT 2.51
  µPLAT®-7B Instruction Set Simulator

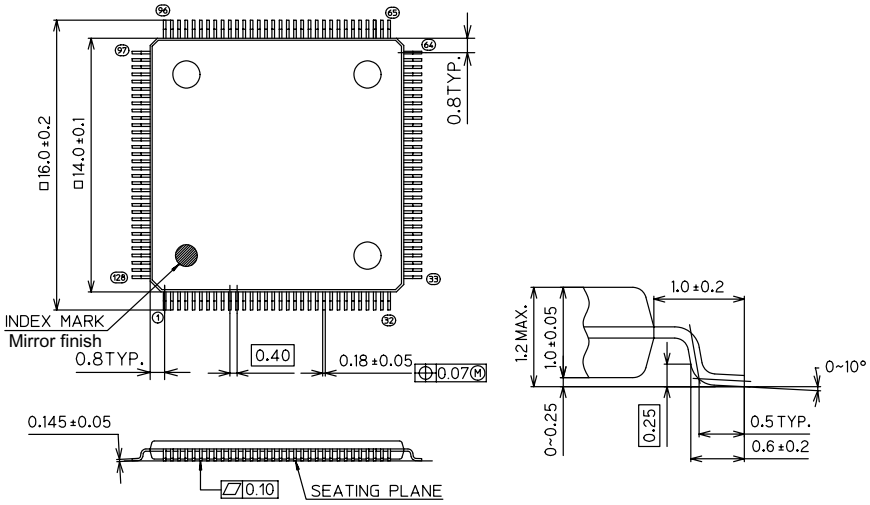
Development Environment

• ML674000 Development Evaluation Kit
  ML674000 CPU evaluation board
  µITRON (under planning)
  Sample software
• µPLAT-7B prototyping Kit
  µPLAT®-7B base LSI development environment
• OKI ADI board
  Interface board for device having the same interface as ARM Multi-ICE.
  Oki Electric is selling it under license from ARM.

PACKAGE DIMENSIONS

(Unit : mm)

TQFP128-P-1414-0.40-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	1/Nov. 18, 1999

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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   Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.

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